MOSPOWER design catalog
including RF

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MOSPOWER Design Catalog January 1983

Product Status and Definitions

DATA SHEET IDENTIFICATION	PRODUCT STATUS	DEFINITION
Preview (Product not available for sampling)	Objective technical specification	Data sheet is a design specification of new products to be announced within 3 months.
Advance Information Marked "Sample"	Sampling available prior to production release for application design cycle.	Data sheet available covering electrical test limits and test conditions. Absolute limits subject to change. Production quantities available within 60 days.
Preliminary Marked "Proto"	First production	Data sheet finalized and limited production quantities available. Initial reliability and characterization curves available. 4–8 weeks typical delivery.
No Identification Noted	Full production	Data sheet finalized and application information available. Sampling and production order subject to product demand and manufacturing availability.

NOTE: Siliconix reserves the right to make changes at any time without notice in order to improve design and supply the best product possible.

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PREFACE

Headquartered in Santa Clara, California, Siliconix is a multinational company with five wholly-owned subsidiaries that manufacture and/or market semiconductors—including MOSPOWER, RF MOSPOWER, ICs, Analog Switches and Small Signal FETs. Manufacturing and marketing operations are located in Santa Clara, Swansea (Wales), Hong Kong and Taiwan. Marketing operations are also located in England, France and West Germany, with a joint sales venture in Japan.

Since pioneering the MOSPOWER technology on October 11, 1975, Siliconix has not only continued to lead the industry in units shipped, but has introduced the first RF MOSPOWER line, introduced the first Quad MOSPOWER devices, and introduced the world's only 200°C rated device. Siliconix' continual commitment to high reliability has motivated development of nitride passivation, unique field termination and the most rugged device now available.

Fabricated by the double-diffused MOS process, the MOSPOWER devices offer the advantages of speed and simple drive requirements characteristic of MOS transistors. Unlike bipolar transistors, MOSPOWER devices do not require protective circuitry to prevent damage from secondary breakdown and, because of their high input impedance, they can be driven and controlled by a single IC. The advantages of MOSPOWER devices over bipolar transistors have stimulated new higher performance designs which take advantage of the extremely fast switching speeds, better voltage control and temperature stability.

Siliconix offers the most extensive range of MOSPOWER electrical ratings and package options from any single source. Single MOSPOWER transistors are offered with drain-to-source breakdown voltages from 30V to 500V, drain currents from 0.15A to 40A and "ON" resistance ratings from 0.055Ω to 10Ω. N- and P-Channel Quads in both plastic and side braze with breakdown voltages up to 90V are also offered.

Continuing support of military and high-reliability needs, Siliconix offers optional /750, /883, and JANTXV equivalent process flows for all hermetic packages. Siliconix will continue to lead the industry with the most high-rel units shipped in 1982.

Siliconix' vast sales network has made state-of-the-art technology readily available today. With continuing advancements in design and packaging techniques, higher voltage, higher current and more complex devices will soon be available to make designers' jobs even easier.

Tony Grant

TONY GRANT
MOSPOWER PRODUCT MARKETING MANAGER

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MOSPOWER

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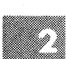
N-/P-Channel 
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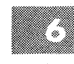
Application Notes 
Other Siliconix Products
Worldwide Sales Offices

How to Use the MOSPOWER Selector Guides

SHORT FORM MOSPOWER SELECTOR GUIDE (PRIME PRODUCTS):

This selector guide is designed to quickly identify the appropriate product family (data sheet) by separating the MOSPOWER product line by package type, breakdown voltage and current handling capability. This selector guide only shows prime products. For more cost effective selections, refer to the full line selector guide or the appropriate data sheet.

MOSPOWER SELECTOR GUIDE (FULL LINE):

This selector guide lists the complete MOSPOWER product line by package type, breakdown voltage, $R_{DS(on)}$, $I_{D(continuous)}$, power dissipation, and part number. For complete electrical characteristics and power ratings, refer to the appropriate data sheet listed in the Table of Contents.

MOSPOWER Prime Product Selector Guide

* 200°C RATING

Packages:								
BV_{DSS} (Volts)	TO-3	TO-220	TO-39	TO-237	TO-92	TO-202	Quad Side Braze	Quad Plastic
450-500	IRF450 13A, 0.4Ω	IRF840 8A, 0.85Ω						
	IRF440 8A, 0.85Ω	VN5001D/IRF830 5.5A, 1.5Ω						
	VNP002A* 6.5A, 1.5Ω	IRF820 2.5A, 3Ω						
	VN5001A/IRF430 4.5A, 1.5Ω							
350-400	IRF350 15A, 0.3Ω	IRF740 10A, 0.55Ω						
	IRF340 10A, 0.55Ω	VN4000D/IRF730 5.5A, 1.0Ω						
	VNM001A* 8A, 1.0Ω	IRF720 3A, 1.8Ω						
	VN4000A/IRF330 5.5A, 1.0Ω							
150-240	IRF250 30A, 0.085Ω	IRF640 18A, 0.18Ω	VN2406B 0.8A, 6Ω	VN2406M 0.3A, 6Ω	VN2406L 0.21A, 6Ω			
	IRF240 18A, 0.18Ω	IRF630 9A, 0.4Ω		VN2410M 0.25A, 10Ω	VN2410L 0.16A, 10Ω			
	IRF230 9A, 0.4Ω	IRF620 5A, 0.8Ω						
	IRF220 5A, 0.8Ω	VN2406D 1.4A, 6Ω						

MOSPOWER Prime Product Selector Guide

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P-CHANNEL

Packages:								
BV$_{DSS}$ (Volts)	**TO-3**	**TO-220**	**TO-39**	**TO-237**	**TO-92**	**TO-202**	**Quad Side Braze**	**Quad Plastic**
100–120	IRF150 40A, 0.055Ω	IRF540 27A, 0.085Ω	IRFF120 6A, 0.30Ω	VN1206M 0.3A, 6Ω	VN1206L 0.21A, 6Ω			
	IRF140 27A, 0.085Ω	VN1200D/IRF530 14A, 0.18Ω	IRFF122 5A, 0.40Ω	VN1210M 0.25A, 10Ω	VN1210L 0.16A, 10Ω			
	VN1200A/IRF130 14A, 0.18Ω	IRF520 8A, 0.30Ω	VN1206B 0.8A, 6Ω	VP1008M 0.37A, 5Ω	VP1008L 0.23A, 5Ω			
	IRF120 8A, 0.3Ω	VN1206D 1.4A, 6Ω	VP1008B 0.9A, 5Ω					
80–90	VN0800A 14A, 0.18Ω	VN0800D 14A, 0.18Ω	2N6661 0.9A, 4Ω	VN0808M 0.35A, 4Ω	VP0808L 0.23A, 5Ω	VN88AF 1.5A, 4Ω	VQ1006P 0.40A, 4.5Ω	VQ1006J 0.40A, 4.5Ω
	2N6658 1.9A, 4Ω	VN88AD 1.7A, 4Ω	VP0808B 0.9A, 5Ω	VP0808M 0.37A, 5Ω		VN80AF 1.3A, 5Ω	VQ2006P 0.41A, 5Ω	VQ2006J 0.41A, 5Ω
60	IRF151 40A, 0.055Ω	IRF541 27A, 0.085Ω	IRFF121 6A, 0.30Ω	VN0606M 0.4, 3Ω	VN0610L 0.2A, 5Ω	VN66AF 1.7A, 3Ω	VQ1004P 0.46A, 3.5Ω	VQ1004J 0.46A, 3.5Ω
	IRF141 27A, 0.085Ω	VN0600D 18A, 0.12Ω	IRFF123 5A, 0.40Ω	VN10KM 0.3A, 5Ω	VN2222L 0.15A, 7.5Ω	VN67AF 1.6A, 3.5Ω	VQ1000P 0.225A, 5.5Ω	VQ1000J 0.225A, 5.5Ω
	VN0600A 18A, 0.12Ω	IRF531 14A, 0.18Ω	2N6660 1.1A, 3Ω	VN2222KM 0.25A, 7.5Ω			VQ2004P 0.41A, 5Ω	VQ2004J 0.41A, 5Ω
	IRF131 14A, 0.18Ω	IRF521 8A, 0.30Ω	VN67AB 1A, 3.5Ω					
	2N6657 2A, 3Ω	VN66AD 1.9A, 3Ω						
30–40	VN0400A 18A, 0.12Ω	VN0400D 18A, 0.12Ω	2N6659 1.4A, 1.8Ω	VN0300M 0.7A, 1.2Ω		VN46AF 1.6A, 3Ω	VQ1001P 0.85A, 1.0Ω	VQ1001J 0.85A, 1.0Ω
	2N6656 2A, 1.8Ω	VN0300D 2.5A, 1.2Ω	VP0300B 1.3A, 2.5Ω	VP0300M 0.48A, 2.5Ω		VN40AF 1.3A, 5Ω	VQ2001P 0.6A, 2Ω	VQ2001J 0.6A, 2Ω
Specialty Products (N- and P-Channel Quad Arrays)							VQ3001P 30V, 3Ω Total	VQ3001J 30V, 3Ω Total
							VQ7254P 20V, 3Ω Total	VQ7254J 20V, 3Ω Total

MOSPOWER Selector Guide

Siliconix

N-Channel MOSPOWER

Device	Breakdown Voltage (Volts)	$r_{DS(on)}$ (Ohms)	I_D Continuous (Amps)	Power Dissipation (Watts)	Part Number
	500	0.4	13.0	150	IRF450
	500	0.5	12.0	150	IRF452
	500	0.85	8.0	125	IRF440
	500	1.10	7.0	125	IRF442
	500	1.5	6.5	175	VNP002A*
	500	1.5	4.5	100	VN5001A
	500	1.5	4.5	75	IRF430
	500	2.0	4.0	100	VN5002A
	500	2.0	4.0	75	IRF432
	500	3.0	2.5	40	IRF420
	500	4.0	2.0	40	IRF422
	450	0.4	13.0	150	IRF451
	450	0.5	12.0	150	IRF453
	450	0.85	8.0	125	IRF441
	450	1.10	7.0	125	IRF443
	450	1.5	6.5	175	VNN002A*
	450	1.5	4.5	100	VN4501A
	450	1.5	4.5	75	IRF431
	450	2.0	4.0	100	VN4502A
	450	2.0	4.0	75	IRF433
	450	3.0	2.5	40	IRF421
	450	4.0	2.0	40	IRF423
	400	0.3	15.0	150	IRF350
	400	0.4	13.0	150	IRF352
	400	0.55	10.0	125	IRF340
	400	0.80	8.0	125	IRF342
	400	1.0	8.0	175	VNM001A*
	400	1.0	6.0	125	VN4000A
	400	1.0	5.5	75	IRF330
	400	1.5	5.0	125	VN4001A
	400	1.5	4.5	75	IRF332
	400	1.8	3.0	40	IRF320
	400	2.5	2.5	40	IRF322
TO-3	350	0.3	15.0	150	IRF351
	350	0.4	13.0	150	IRF353
	350	0.55	10.0	125	IRF341
	350	0.80	8.0	125	IRF343
	350	1.0	8.0	175	VNL001A*
	350	1.0	6.0	125	VN3500A
	350	1.0	5.5	75	IRF331
	350	1.5	5.0	125	VN3501A
	350	1.5	4.5	75	IRF333
	350	1.8	3.0	40	IRF321
	350	2.5	2.5	40	IRF323
	200	0.085	30.0	150	IRF250
	200	0.12	25.0	150	IRF252
	200	0.18	18.0	125	IRF240
	200	0.22	16.0	125	IRF242
	200	0.4	9.0	75	IRF230
	200	0.6	8.0	75	IRF232
	200	0.8	5.0	40	IRF220
	200	1.2	4.0	40	IRF222
	150	0.085	30.0	150	IRF251
	150	0.12	25.0	150	IRF253
	150	0.18	18.0	125	IRF241
	150	0.22	16.0	125	IRF243
	150	0.4	9.0	75	IRF231
	150	0.6	8.0	75	IRF233
	150	0.8	5.0	40	IRF221
	150	1.2	4.0	40	IRF223
	120	0.18	14.0	75	VN1200A
	120	0.25	12.0	100	VN1201A

*200°C Rating

MOSPOWER Selector Guide (Continued)

N-Channel MOSPOWER (Continued)

Device	Breakdown Voltage (Volts)	$r_{DS(on)}$ (Ohms)	I_D Continuous (Amps)	Power Dissipation (Watts)	Part Number
TO-3	100	0.055	40.0	150	IRF150
	100	0.08	33.0	150	IRF152
	100	0.085	27.0	125	IRF140
	100	0.11	24.0	125	IRF142
	100	0.18	14.0	100	VN1000A
	100	0.18	14.0	75	IRF130
	100	0.25	12.0	100	VN1001A
	100	0.25	12.0	75	IRF132
	100	0.3	8.0	40	IRF120
	100	0.4	7.0	40	IRF122
	90	4.0	1.9	25	2N6658
	90	4.5	1.8	25	VN99AA
	90	5.0	1.7	25	VN90AA
	80	0.18	14.0	100	VN0800A
	80	0.25	12.0	100	VN0801A
	60	0.055	40.0	150	IRF151
	60	0.08	33.0	150	IRF153
	60	0.085	27.0	125	IRF141
	60	0.11	24.0	125	IRF143
	60	0.12	18.0	100	VN0600A
	60	0.15	16.0	100	VN0601A
	60	0.18	14.0	75	IRF131
	60	0.25	12.0	75	IRF133
	60	0.3	8.0	40	IRF121
	60	0.4	10.0	80	VN64GA
	60	0.4	7.0	40	IRF123
	60	3.0	2.0	25	2N6657
	60	3.5	2.0	25	VN67AA
	40	0.12	18.0	100	VN0400A
	40	0.15	16.0	100	VN0401A
	35	1.8	2.0	25	2N6656
	35	2.5	2.0	25	VN35AA
TO-220AB	500	0.85	8.0	125	IRF840
	500	1.10	7.0	125	IRF842
	500	1.5	4.5	75	VN5001D
	500	1.5	4.5	75	IRF830
	500	2.0	4.0	75	VN5002D
	500	2.0	4.0	75	IRF832
	500	3.0	2.5	40	IRF820
	500	4.0	2.0	40	IRF822
	450	0.85	8.0	125	IRF841
	450	1.10	7.0	125	IRF843
	450	1.5	4.5	75	VN4501D
	450	1.5	4.5	75	IRF831
	450	2.0	4.0	75	VN4502D
	450	2.0	4.0	75	IRF833
	450	3.0	2.5	40	IRF821
	450	4.0	2.0	40	IRF823
	400	0.55	10.0	125	IRF740
	400	0.80	8.0	125	IRF742
	400	1.0	6.0	75	VN4000D
	400	1.0	5.5	75	IRF730
	400	1.5	5.0	75	VN4001D
	400	1.5	4.5	75	IRF732
	400	1.8	3.0	40	IRF720
	400	2.5	2.5	40	IRF722
	350	0.55	10.0	125	IRF741
	350	0.80	8.0	125	IRF743
	350	1.0	6.0	75	VN3500D
	350	1.0	5.5	75	IRF731
	350	1.5	5.0	75	VN3501D
	350	1.5	4.5	75	IRF733
	350	1.8	3.0	40	IRF721
	350	2.5	2.5	40	IRF723
	240	6.0	1.4	20	VN2406D

MOSPOWER Selector Guide (Continued)

N-Channel MOSPOWER (Continued)

Device	Breakdown Voltage (Volts)	$r_{DS(on)}$ (Ohms)	I_D Continuous (Amps)	Power Dissipation (Watts)	Part Number
TO-220AB	200	0.18	18.0	125	IRF640
	200	0.22	16.0	125	IRF642
	200	0.4	9.0	75	IRF630
	200	0.6	8.0	75	IRF632
	200	0.8	5.0	40	IRF620
	200	1.2	4.0	40	IRF622
	170	6.0	1.4	20	VN1706D
	150	0.18	18.0	125	IRF641
	150	0.22	16.0	125	IRF643
	150	0.4	9.0	75	IRF631
	150	0.6	8.0	75	IRF633
	150	0.8	5.0	40	IRF621
	150	1.2	4.0	40	IRF623
	120	0.18	14.0	75	VN1200D
	120	0.25	12.0	75	VN1201D
	120	6.0	1.4	20	VN1206D
	100	0.085	27.0	125	IRF540
	100	0.11	24.0	125	IRF542
	100	0.18	14.0	75	VN1000D
	100	0.18	14.0	75	IRF530
	100	0.25	12.0	75	VN1001D
	100	0.25	12.0	75	IRF532
	100	0.30	8.0	40	IRF520
	100	0.40	7.0	40	IRF522
	80	0.18	14.0	75	VN0800D
	80	0.25	12.0	75	VN0801D
	80	4.0	1.7	20	VN88AD
	80	4.5	1.6	20	VN89AD
	60	0.085	27.0	125	IRF541
	60	0.11	24.0	125	IRF543
	60	0.12	18.0	75	VN0600D
	60	0.15	16.0	75	VN0601D
	60	0.18	14.0	75	IRF531
	60	0.25	12.0	75	IRF533
	60	0.30	8.0	40	IRF521
	60	0.40	7.0	40	IRF523
	60	3.0	1.9	20	VN66AD
	60	3.5	1.8	20	VN67AD
	40	0.12	18.0	75	VN0400D
	40	0.15	16.0	75	VN0401D
	40	3.0	1.9	20	VN46AD
	40	5.0	1.5	20	VN40AD
	30	1.2	2.5	20	VN0300D
TO-202AA	80	4.0	1.5	15	VN88AF
	80	4.5	1.4	15	VN89AF
	80	5.0	1.3	15	VN80AF
	60	3.0	1.7	15	VN66AF
	60	3.5	1.6	15	VN67AF
	40	3.0	1.6	15	VN46AF
	40	5.0	1.3	15	VN40AF
TO-39	240	6.0	0.8	6.25	VN2406B
	170	6.0	0.8	6.25	VN1706B
	120	6.0	0.8	6.25	VN1206B
	100	0.3	6.0	20	IRFF120
	100	0.4	5.0	20	IRFF122
	90	4.0	0.9	6.25	2N6661
	90	4.5	0.9	6.25	VN99AB
	90	5.0	0.8	6.25	VN90AB
	60	0.3	6.0	20	IRFF121
	60	0.4	5.0	20	IRFF123
	60	3.0	1.1	6.25	2N6660
	60	3.5	1.0	6.25	VN67AB
	35	1.8	1.4	6.25	2N6659
	35	2.5	1.2	6.25	VN35AB

MOSPOWER Selector Guide (Continued)

N-Channel MOSPOWER (Continued)

Device	Breakdown Voltage (Volts)	$r_{DS(on)}$ (Ohms)	I_D Continuous (Amps)	Power Dissipation (Watts)	Part Number
TO-52	60	5.0	0.2	0.315	VN10KE
	60	5.0	0.2	0.315	VN10LE
TO-237	240	6.0	0.3	1.0	VN2406M
	240	10.0	0.25	1.0	VN2410M
	170	6.0	0.3	1.0	VN1706M
	170	10.0	0.25	1.0	VN1710M
	120	6.0	0.3	1.0	VN1206M
	120	10.0	0.25	1.0	VN1210M
	80	4.0	0.35	1.0	VN0808M
	60	3.0	0.4	1.0	VN0606M
	60	5.0	0.3	1.0	VN10KM
	60	5.0	0.3	1.0	VN10LM
	60	7.5	0.25	1.0	VN2222KM
	60	7.5	0.25	1.0	VN2222LM
	30	1.2	0.7	1.0	VN0300M
TO-92	240	6.0	0.21	0.4	VN2406L
	240	10.0	0.16	0.4	VN2410L
	170	6.0	0.21	0.4	VN1706L
	170	10.0	0.16	0.4	VN1710L
	120	6.0	0.21	0.4	VN1206L
	120	10.0	0.16	0.4	VN1210L
	60	5.0	0.2	0.4	VN0610L
	60	7.5	0.15	0.4	VN2222L
14-Pin Dual-In-Line (Side Braze)	90	4.5	0.40	1.3	VQ1006P
	60	3.5	0.46	1.3	VQ1004P
	60	5.5	0.225	0.5	VQ1000P
	30	1.0	0.85	1.3	VQ1001P
14-Pin Dual-In-Line (Plastic)	90	4.5	0.40	1.3	VQ1006J
	60	3.5	0.46	1.3	VQ1004J
	60	5.5	0.225	0.5	VQ1000J
	30	1.0	0.85	1.3	VQ1001J

MOSPOWER Selector Guide (Continued)

P-Channel MOSPOWER

Device	Breakdown Voltage (Volts)	$r_{DS(on)}$ (Ohms)	I_D Continuous (Amps)	Power Dissipation (Watts)	Part Number
TO-39	−100	5.0	0.9	6.25	VP1008B
	−80	5.0	0.9	6.25	VP0808B
	−30	2.5	1.3	6.25	VP0300B
TO-237	−100	5.0	0.37	1.0	VP1008M
	−80	5.0	0.37	1.0	VP0808M
	−30	2.5	0.48	1.0	VP0300M
TO-92	−100	5.0	0.23	0.4	VP1008L
	−80	5.0	0.23	0.4	VP0808L
14-Pin Dual-In-Line (Side Braze)	−90	5.0	0.41	1.3	VQ2006P
	−60	5.0	0.41	1.3	VQ2004P
	−30	2.0	0.60	1.3	VQ2001P
14-Pin Dual-In-Line (Plastic)	−90	5.0	0.41	1.3	VQ2006J
	−60	5.0	0.41	1.3	VQ2004J
	−30	2.0	0.60	1.3	VQ2001J

N- and P-Channel Quad MOSPOWER

Device	Breakdown Voltage (Volts)	$r_{DS(on)}$ (Ohms)	I_D Continuous (Amps)	Power Dissipation (Watts)	Part Number
14-Pin Dual-In-Line (Side Braze)	30	3.0**	N- 0.60 P- 0.85	1.3	VQ3001P
	20	3.0**	N- 0.60 P- 0.85	1.3	VQ7254P
14-Pin Dual-In-Line (Plastic)	30	3.0**	N-0.60 P- 0.85	1.3	VQ3001J
	20	3.0**	N-0.60 P- 0.85	1.3	VQ7254J

**Total (N + P)

MOSPOWER Process Flows

STANDARD PRODUCT FLOW:

Standard MOSPOWER process flow combines preseal visual with MIL-STD environmental procedures to assure the highest quality commercial grade products available.

BURN-IN (LEVEL 4)*:

Optional processing including standard product flow with 100% 96-hour MIL-STD HTRB burn-in at 150°C.

SILICONIX/750*:

The /750 includes full MIL-STD 19500/750 environmentals with burn-ins at 150°C. This optional process flow provides readily available high reliability products similar to MIL-STD 19500 JANTX at low cost.

SILICONIX/883*:

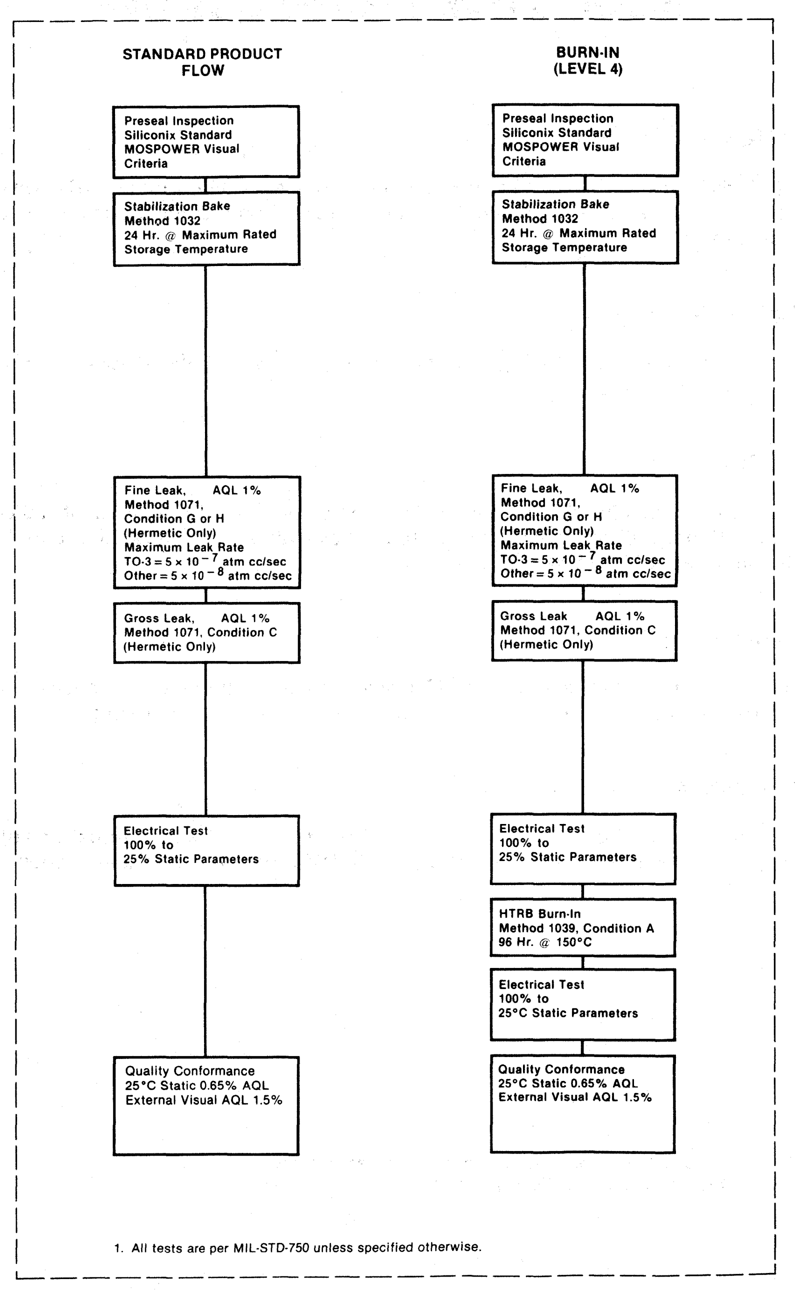
Siliconix's multi-chip version of the /750 flow for dual-in-line side braze packages. The /883 includes full MIL-STD-883B environmental and burn-in testing.

JAN, JANTX, JANTXV EQUIVALENT*:

Siliconix is receiving MIL-STD 19500 JAN, JANTX and JANTXV qualifications on the popular 2N6660 and 2N6661. More MIL-STD devices will be available soon.

*For price and delivery information on optional processing flows contact the local Siliconix Sales Representative.

MOSPOWER
Commercial/Industrial Process Flow[1]



1. All tests are per MIL-STD-750 unless specified otherwise.

MOSPOWER Military/Hi-Rel Process Flows[3]

Standard Military/Hi-Rel Flows

SILICONIX /750

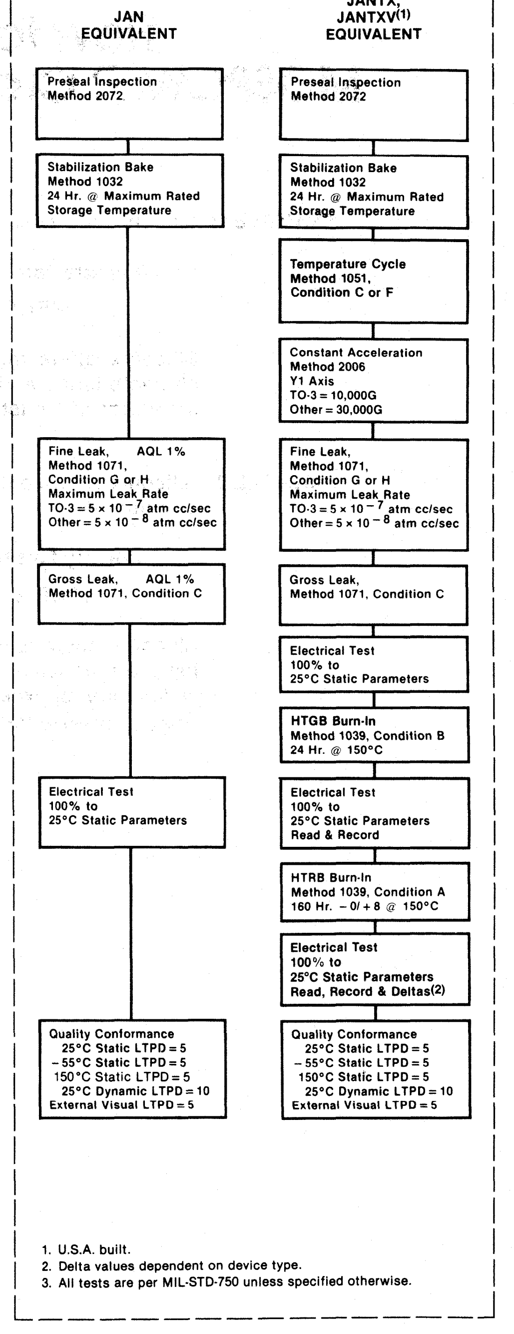
- Preseal Inspection
  Method 2072
- Stabilization Bake
  Method 1032
  24 Hr. @ Maximum Rated Storage Temperature
- Temperature Cycle
  Method 1051,
  Condition C or F
- Constant Acceleration
  Method 2006
  Y1 Axis
  TO-3 = 10,000G
  Other = 30,000G
- Fine Leak,
  Method 1071,
  Condition G or H
  Maximum Leak Rate
  TO-3 = 5×10^{-7} atm cc/sec
  Other = 5×10^{-8} atm cc/sec
- Gross Leak,
  Method 1071, Condition C
- Electrical Test
  100% to
  25°C Static Parameters
- HTGB Burn-In
  Method 1039, Condition B
  24 Hr. @ 150°C
- Electrical Test
  100% to
  25°C Static Parameters
- HTRB Burn-In
  Method 1039, Condition A
  160 Hr. −0/+8 @ 150°C
- Electrical Test
  100% to
  25°C Static Parameters
- Quality Conformance
  25°C Static 0.65% AQL
  External Visual AQL 1.5%

SILICONIX /883 (MULTICHIP SIDEBRAZE)

- Preseal Inspection
  Method 2017
  Condition B — /883
- Stabilization Bake
  Method 1008, Condition C
  150°C, 24 Hours — /883
- Temperature Cycle
  Method 1010, Condition C — /883
- Centrifuge
  Method 2001, Condition E
  30,000G Y1 Axis — /883
- Hermeticity (Fine Leak)
  Method 1014, Condition A or B
  <5×10^{-8} cc/sec — /883
- Hermeticity (Gross Leak)
  Method 1014, Condition C — /883
- Electrical Test
  100% to
  25% Static Parameters
- Burn-In
  Method 1015
  125°C, 160 Hours — /883
- Electrical Test
  100% to
  25°C Static Parameters
- Quality Conformance
  Group A*
  Method 5005 — /883
- External Visual
  Method 2009**
  100% — /883

*Group B and C tests done to customer order on /883 parts
**Physical Dimensions Excluded
The latest revision of MIL-STD-883 is applicable

19500 MIL-STD Optional Flows



How to Use the MOSPOWER Cross Reference List

EXAMPLE 1: Siliconix equivalent is identical to industry part number.

Industry Part Number	Siliconix Equivalent
IRF120	IRF120

Siliconix offers the exact replacement with electrical characteristics and ratings which meet or exceed the standards of industry part number.

EXAMPLE 2: Siliconix equivalent which is not identical to the industry part number.

Industry Part Number	Siliconix Equivalent
HPWR-6501	IRF441

Siliconix equivalents referenced in the cross reference list are functional equivalents in similar package types which meet or exceed the critical device ratings (BV_{DSS}, $R_{DS(on)}$, $I_{D(on)}$) of the industry part number.

MOSPOWER Cross Reference List

HEWLETT-PACKARD

Industry Part No.	BV_{DSS} (Volts)	$r_{DS(on)}$ (Ohms)	Package	Siliconix Equivalent	BV_{DSS} (Volts)	$r_{DS(on)}$ (Ohms)
HPWR-6501	450	0.85	TO-3	IRF441	450	0.85
HPWR-6502	400	0.74	TO-3	IRF340	400	0.55
HPWR-6503	450	1.0	TO-3	IRF441	450	0.85
HPWR-6504	400	1.0	TO-3	VN4001A	400	1.0

HITACHI

Industry Part No.	BV_{DSS} (Volts)	$r_{DS(on)}$ (Ohms)	Package	Siliconix Equivalent	BV_{DSS} (Volts)	$r_{DS(on)}$ (Ohms)
2SK132	100	1.71	TO-3	IRF122	100	0.4
2SK133	120	1.71	TO-3	IRF223	150	1.2
2SK134	140	1.71	TO-3	IRF223	150	1.2
2SK135	160	1.71	TO-3	IRF222	200	1.2
2SK175	180	1.71	TO-3	IRF222	200	1.2
2SK176	200	1.71	TO-3	IRF222	200	1.2
2SK220	160	—	TO-3	—	—	—
2SK221	200	—	TO-3	—	—	—
2SK259	350	3.0	TO-3	IRF323	350	2.5
2SK260	400	3.0	TO-3	IRF322	400	2.5
2SJ47	−100	1.71	TO-3	—	—	—
2SJ48	−120	1.71	TO-3	—	—	—
2SJ49	−140	1.71	TO-3	—	—	—
2SJ50	−160	1.71	TO-3	—	—	—

INTERNATIONAL RECTIFIER

Industry Part No.	BV_{DSS} (Volts)	$r_{DS(on)}$ (Ohms)	Package	Siliconix Equivalent	BV_{DSS} (Volts)	$r_{DS(on)}$ (Ohms)
IRF120	100	0.30	TO-3	IRF120	—	—
IRF121	60	0.30	TO-3	IRF121	—	—
IRF122	100	0.40	TO-3	IRF122	—	—
IRF123	60	0.40	TO-3	IRF123	—	—
IRF130	100	0.18	TO-3	IRF130	—	—
IRF131	60	0.18	TO-3	IRF131	—	—
IRF132	100	0.25	TO-3	IRF132	—	—
IRF133	60	0.25	TO-3	IRF133	—	—
IRF140	100	0.085	TO-3	IRF140	—	—
IRF141	60	0.085	TO-3	IRF141	—	—
IRF142	100	0.11	TO-3	IRF142	—	—
IRF143	60	0.11	TO-3	IRF143	—	—
IRF150	100	0.055	TO-3	IRF150	—	—
IRF151	60	0.055	TO-3	IRF151	—	—
IRF152	100	0.08	TO-3	IRF152	—	—
IRF153	60	0.08	TO-3	IRF153	—	—
IRF220	200	0.8	TO-3	IRF220	—	—
IRF221	150	0.8	TO-3	IRF221	—	—
IRF222	200	1.2	TO-3	IRF222	—	—
IRF223	150	1.2	TO-3	IRF223	—	—
IRF230	200	0.4	TO-3	IRF230	—	—
IRF231	150	0.4	TO-3	IRF231	—	—
IRF232	200	0.6	TO-3	IRF232	—	—
IRF233	150	0.6	TO-3	IRF233	—	—
IRF240	200	0.18	TO-3	IRF240	—	—
IRF241	150	0.18	TO-3	IRF241	—	—
IRF242	200	0.22	TO-3	IRF242	—	—
IRF243	150	0.22	TO-3	IRF243	—	—
IRF250	200	0.085	TO-3	IRF250	—	—
IRF251	150	0.085	TO-3	IRF251	—	—
IRF252	200	0.120	TO-3	IRF252	—	—
IRF253	150	0.120	TO-3	IRF253	—	—
IRF320	400	1.8	TO-3	IRF320	—	—
IRF321	350	1.8	TO-3	IRF321	—	—
IRF322	400	2.5	TO-3	IRF322	—	—
IRF323	350	2.5	TO-3	IRF323	—	—
IRF330	400	1.0	TO-3	IRF330	—	—
IRF331	350	1.0	TO-3	IRF331	—	—
IRF332	400	1.5	TO-3	IRF332	—	—
IRF333	350	1.5	TO-3	IRF333	—	—
IRF340	400	0.55	TO-3	IRF340	—	—
IRF341	350	0.55	TO-3	IRF341	—	—
IRF342	400	0.80	TO-3	IRF342	—	—
IRF343	350	0.80	TO-3	IRF343	—	—
IRF350	400	0.3	TO-3	IRF350	—	—
IRF351	350	0.3	TO-3	IRF351	—	—
IRF352	400	0.4	TO-3	IRF352	—	—
IRF353	350	0.4	TO-3	IRF353	—	—

MOSPOWER Cross Reference List (Cont'd)

INTERNATIONAL RECTIFIER (Cont'd)

Industry Part No.	BV_{DSS} (Volts)	$r_{DS(on)}$ (Ohms)	Package	Siliconix Equivalent	BV_{DSS} (Volts)	$r_{DS(on)}$ (Ohms)
IRF420	500	3.0	TO-3	IRF420	—	—
IRF421	450	3.0	TO-3	IRF421	—	—
IRF422	500	4.0	TO-3	IRF422	—	—
IRF423	450	4.0	TO-3	IRF423	—	—
IRF430	500	1.5	TO-3	IRF430	—	—
IRF431	450	1.5	TO-3	IRF431	—	—
IRF432	500	2.0	TO-3	IRF432	—	—
IRF433	450	2.0	TO-3	IRF433	—	—
IRF440	500	0.85	TO-3	IRF440	—	—
IRF441	450	0.85	TO-3	IRF441	—	—
IRF442	500	1.10	TO-3	IRF442	—	—
IRF443	450	1.10	TO-3	IRF443	—	—
IRF450	500	0.4	TO-3	IRF450	—	—
IRF451	450	0.4	TO-3	IRF451	—	—
IRF452	500	0.5	TO-3	IRF452	—	—
IRF453	450	0.5	TO-3	IRF453	—	—
IRF510	100	0.6	TO-220	—	—	—
IRF511	60	0.6	TO-220	—	—	—
IRF512	100	0.8	TO-220	—	—	—
IRF513	60	0.8	TO-220	—	—	—
IRF520	100	0.3	TO-220	IRF520	—	—
IRF521	60	0.3	TO-220	IRF521	—	—
IRF522	100	0.4	TO-220	IRF522	—	—
IRF523	60	0.4	TO-220	IRF523	—	—
IRF530	100	0.18	TO-220	IRF530	—	—
IRF531	100	0.25	TO-220	IRF531	—	—
IRF532	60	0.18	TO-220	IRF532	—	—
IRF533	60	0.25	TO-220	IRF533	—	—
IRF540	100	0.085	TO-220	IRF540	—	—
IRF541	60	0.085	TO-220	IRF541	—	—
IRF542	100	0.11	TO-220	IRF542	—	—
IRF543	60	0.11	TO-220	IRF543	—	—
IRF610	100	1.6	TO-220	—	—	—
IRF611	60	1.6	TO-220	—	—	—
IRF612	100	2.4	TO-220	—	—	—
IRF613	60	2.4	TO-220	—	—	—
IRF620	200	0.8	TO-220	IRF620	—	—
IRF621	150	0.8	TO-220	IRF621	—	—
IRF622	200	1.2	TO-220	IRF622	—	—
IRF623	150	1.2	TO-220	IRF623	—	—
IRF630	200	0.4	TO-220	IRF630	—	—
IRF631	150	0.4	TO-220	IRF631	—	—
IRF632	200	0.6	TO-220	IRF632	—	—
IRF633	150	0.6	TO-220	IRF633	—	—
IRF640	200	0.18	TO-220	IRF640	—	—
IRF641	150	0.18	TO-220	IRF641	—	—
IRF642	200	0.22	TO-220	IRF642	—	—
IRF643	150	0.22	TO-220	IRF643	—	—
IRF710	100	3.6	TO-220	—	—	—
IRF711	60	3.6	TO-220	—	—	—
IRF712	100	5.0	TO-220	—	—	—
IRF713	60	5.0	TO-220	—	—	—
IRF720	400	1.8	TO-220	IRF720	—	—
IRF721	350	1.8	TO-220	IRF721	—	—
IRF722	400	2.5	TO-220	IRF722	—	—
IRF723	350	2.5	TO-220	IRF723	—	—
IRF730	400	1.0	TO-220	IRF730	—	—
IRF731	350	1.0	TO-220	IRF731	—	—
IRF732	400	1.5	TO-220	IRF732	—	—
IRF733	350	1.5	TO-220	IRF733	—	—
IRF820	500	3.0	TO-220	IRF820	—	—
IRF821	450	3.0	TO-220	IRF821	—	—
IRF822	500	4.0	TO-220	IRF822	—	—
IRF823	450	4.0	TO-220	IRF823	—	—
IRF830	500	1.5	TO-220	IRF830	—	—
IRF831	450	1.5	TO-220	IRF831	—	—
IRF832	500	2.0	TO-220	IRF832	—	—
IRF833	450	2.0	TO-220	IRF833	—	—
IRF840	500	0.85	TO-220	IRF840	—	—
IRF841	450	0.85	TO-220	IRF841	—	—
IRF842	500	1.1	TO-220	IRF842	—	—
IRF843	450	1.1	TO-220	IRF843	—	—

MOSPOWER Cross Reference List (Cont'd)

INTERNATIONAL RECTIFIER (Cont'd)

Industry Part No.	BV_{DSS} (Volts)	$r_{DS(on)}$ (Ohms)	Package	Siliconix Equivalent	BV_{DSS} (Volts)	$r_{DS(on)}$ (Ohms)
IRF9130	100	0.3	TO-3	IRF9130*	—	—
IRF9131	60	0.3	TO-3	IRF9131	—	—
IRF9132	100	0.4	TO-3	IRF9132	—	—
IRF9133	60	0.4	TO-3	IRF9133	—	—
IRF9230	200	0.8	TO-3	—	—	—
IRF9231	150	0.8	TO-3	—	—	—
IRF9232	200	1.2	TO-3	—	—	—
IRF9233	150	1.2	TO-3	—	—	—
IRF9520	100	0.6	TO-220	IRF9520*	—	—
IRF9521	60	0.6	TO-220	IRF9521	—	—
IRF9522	100	0.8	TO-220	IRF9522	—	—
IRF9523	60	0.8	TO-220	IRF9523	—	—
IRF9530	100	0.3	TO-220	IRF9530*	—	—
IRF9531	60	0.3	TO-220	IRF9531	—	—
IRF9532	100	0.4	TO-220	IRF9532	—	—
IRF9533	60	0.4	TO-220	IRF9533	—	—
IRF9610	200	3.0	TO-220	—	—	—
IRF9611	150	3.0	TO-220	—	—	—
IRF9612	200	4.5	TO-220	—	—	—
IRF9613	150	4.5	TO-220	—	—	—
IRF9620	200	1.5	TO-220	—	—	—
IRF9621	150	1.5	TO-220	—	—	—
IRF9622	200	2.4	TO-220	—	—	—
IRF9623	150	2.4	TO-220	—	—	—
IRF9630	200	0.8	TO-220	—	—	—
IRF9631	150	0.8	TO-220	—	—	—
IRF9632	200	1.2	TO-220	—	—	—
IRF9633	150	1.2	TO-220	—	—	—
IRFF110	100	0.6	TO-39	—	—	—
IRFF111	60	0.6	TO-39	—	—	—
IRFF112	100	0.8	TO-39	—	—	—
IRFF113	60	0.8	TO-39	—	—	—
IRFF120	100	0.30	TO-39	IRFF120	—	—
IRFF121	60	0.30	TO-39	IRFF121	—	—
IRFF122	100	0.40	TO-39	IRFF122	—	—
IRFF123	60	0.40	TO-39	IRFF123	—	—
IRFF130	100	0.18	TO-39	—	—	—
IRFF131	60	0.18	TO-39	—	—	—
IRFF132	100	0.25	TO-39	—	—	—
IRFF133	60	0.25	TO-39	—	—	—
2N6755	60	0.25	TO-3	IRF131	—	—
2N6756	100	0.18	TO-3	IRF130	—	—
2N6757	150	0.6	TO-3	—	—	—
2N6758	200	0.4	TO-3	—	—	—
2N6759	350	1.5	TO-3	IRF333	—	—
2N6760	400	1.0	TO-3	IRF330	—	—
2N6761	450	2.0	TO-3	IRF433	—	—
2N6762	500	1.5	TO-3	IRF430	—	—
2N6763	60	0.08	TO-3	—	—	—
2N6764	100	0.055	TO-3	—	—	—
2N6765	150	0.120	TO-3	—	—	—
2N6766	200	0.085	TO-3	—	—	—
2N6767	350	0.4	TO-3	—	—	—
2N6768	400	0.3	TO-3	—	—	—
2N6769	450	0.5	TO-3	—	—	—
2N6770	500	0.4	TO-3	—	—	—
2N6781	60	0.6	TO-39	—	—	—
2N6782	100	0.6	TO-39	—	—	—
2N6783	150	1.5	TO-39	—	—	—
2N6784	200	1.5	TO-39	—	—	—
2N6785	350	3.6	TO-39	—	—	—
2N6786	400	3.6	TO-39	—	—	—
2N6787	60	0.3	TO-39	—	—	—
2N6788	100	0.3	TO-39	—	—	—
2N6789	150	0.8	TO-39	—	—	—
2N6790	200	0.8	TO-39	—	—	—
2N6791	350	1.8	TO-39	—	—	—
2N6792	400	1.8	TO-39	—	—	—
2N6793	450	3.0	TO-39	—	—	—
2N6794	500	3.0	TO-39	—	—	—
2N6795	60	0.18	TO-39	—	—	—

*Product family available by March 1983

MOSPOWER Cross Reference List (Cont'd)

INTERNATIONAL RECTIFIER (Cont'd)

Industry Part No.	BV_{DSS} (Volts)	$r_{DS(on)}$ (Ohms)	Package	Siliconix Equivalent	BV_{DSS} (Volts)	$r_{DS(on)}$ (Ohms)
2N6796	100	0.18	TO-39	—	—	—
2N6797	150	0.4	TO-39	—	—	—
2N6798	200	0.4	TO-39	—	—	—
2N6799	350	1.0	TO-39	—	—	—
2N6800	400	1.0	TO-39	—	—	—
2N6801	450	1.5	TO-39	—	—	—
2N6802	500	1.5	TO-39	—	—	—

INTERSIL

Industry Part No.	BV_{DSS} (Volts)	$r_{DS(on)}$ (Ohms)	Package	Siliconix Equivalent	BV_{DSS} (Volts)	$r_{DS(on)}$ (Ohms)
IVN5000AND	40	2.5	TO-237	—	—	—
IVN5000ANE	60	2.5	TO-237	—	—	—
IVN5000ANF	80	2.5	TO-237	—	—	—
IVN5000ANH	100	2.5	TO-237	—	—	—
IVN5000SND	40	2.5	TO-52	—	—	—
IVN5000SNE	60	2.5	TO-52	—	—	—
IVN5000SNF	80	2.5	TO-52	—	—	—
IVN5000SNH	100	2.5	TO-52	—	—	—
IVN5000TND	40	2.5	TO-39	—	—	—
IVN5000TNE	60	2.5	TO-39	—	—	—
IVN5000TNF	80	2.5	TO-39	—	—	—
IVN5000TNH	100	2.5	TO-39	—	—	—
IVN5001AND	40	2.5	TO-237	—	—	—
IVN5001ANE	60	2.5	TO-237	—	—	—
IVN5001ANF	80	2.5	TO-237	—	—	—
IVN5001ANH	100	2.5	TO-237	—	—	—
IVN5001SND	40	2.5	TO-52	—	—	—
IVN5001SNE	60	2.5	TO-52	—	—	—
IVN5001SNF	80	2.5	TO-52	—	—	—
IVN5001SNH	100	2.5	TO-52	—	—	—
IVN5001TND	40	2.5	TO-39	—	—	—
IVN5001TNE	60	2.5	TO-39	—	—	—
IVN5001TNF	80	2.5	TO-39	—	—	—
IVN5001TNH	100	2.5	TO-39	—	—	—
IVN5200HND	40	0.5	TO-66	—	—	—
IVN5200HNE	60	0.5	TO-66	—	—	—
IVN5200HNF	80	0.5	TO-66	—	—	—
IVN5200HNH	100	0.5	TO-66	—	—	—
IVN5200KND	40	0.5	TO-3	IRF123	60	0.4
IVN5200KNE	60	0.5	TO-3	IRF123	60	0.4
IVN5200KNF	80	0.5	TO-3	IRF122	100	0.4
IVN5200KNH	100	0.5	TO-3	IRF122	100	0.4
IVN5200TND	40	0.5	TO-39	IRFF123	60	0.4
IVN5200TNE	60	0.5	TO-39	IRFF123	60	0.4
IVN5200TNF	80	0.5	TO-39	IRFF122	100	0.4
IVN5200TNH	100	0.5	TO-39	IRFF122	100	0.4
IVN5201CND	40	0.5	TO-220	IRF523	60	0.4
IVN5201CNE	60	0.5	TO-220	IRF523	60	0.4
IVN5201CNF	80	0.5	TO-220	IRF522	100	0.4
IVN5201CNH	100	0.5	TO-220	IRF522	100	0.4
IVN5201HND	40	0.5	TO-66	—	—	—
IVN5201HNE	60	0.5	TO-66	—	—	—
IVN5201HNF	80	0.5	TO-66	—	—	—
IVN5201HNH	100	0.5	TO-66	—	—	—
IVN5201KND	40	0.5	TO-3	IRF123	60	0.4
IVN5201KNE	60	0.5	TO-3	IRF123	60	0.4
IVN5201KNF	80	0.5	TO-3	IRF122	100	0.4
IVN5201KNH	100	0.5	TO-3	IRF122	100	0.4
IVN5201TND	40	0.5	TO-39	IRF123	60	0.4
IVN5201TNE	60	0.5	TO-39	IRF123	60	0.4
IVN5201TNF	80	0.5	TO-39	IRF122	100	0.4
IVN5201TNH	100	0.5	TO-39	IRF122	100	0.4
IVN6000CNS	400	3.5	TO-220	IRF722	400	2.5
IVN6000CNT	450	3.5	TO-220	IRF821	450	3.0
IVN6000CNU	500	4.0	TO-220	IRF822	500	4.0
IVN6000KNR	350	3.0	TO-3	IRF323	350	2.5
IVN6000KNS	400	3.0	TO-3	IRF322	400	2.5
IVN6000KNT	450	3.0	TO-3	IRF421	450	3.0
IVN6000KNU	500	4.0	TO-3	IRF422	500	4.0
IVN6100TNS	400	15.0	TO-39	—	—	—
IVN6100TNT	450	15.0	TO-39	—	—	—

MOSPOWER Cross Reference List (Cont'd)

INTERSIL (Cont'd)

Industry Part No.	BV_{DSS} (Volts)	$r_{DS(on)}$ (Ohms)	Package	Siliconix Equivalent	BV_{DSS} (Volts)	$r_{DS(on)}$ (Ohms)
IVN6100TNU	500	15.0	TO-39	—	—	—
IVN6200CND	40	0.35	TO-220	VN0401D	40	0.15
IVN6200CNE	60	0.25	TO-220	IRF533	60	0.25
IVN6200CNF	80	0.25	TO-220	VN0801D	80	0.25
IVN6200CNH	100	0.25	TO-220	VN1001D	100	0.25
IVN6200CNM	200	0.5	TO-220	IRF630	200	0.4
IVN6200CNP	250	0.5	TO-220	—	—	—
IVN6200CNR	395	2.5	TO-220	VN4001D	400	1.5
IVN6200CNS	400	1.5	TO-220	VN4001D	400	1.5
IVN6200CNT	450	1.5	TO-220	VN4501D	450	1.5
IVN6200CNU	500	2.0	TO-220	VN5001D	500	1.5
IVN6200KND	40	0.25	TO-3	VN0401A	40	0.15
IVN6200KNE	60	0.25	TO-3	IRF133	60	0.25
IVN6200KNF	80	0.25	TO-3	VN0801A	80	0.25
IVN6200KNH	100	0.25	TO-3	VN1001A	100	0.25
IVN6200KNM	200	0.5	TO-3	IRF230	200	0.4
IVN6200KNP	250	0.5	TO-3	—	—	—
IVN6200KNS	400	1.5	TO-3	VN4001A	400	1.5
IVN6200KNT	450	1.5	TO-3	VN4501A	450	1.5
IVN6200KNU	500	2.0	TO-3	VN5000A	500	1.5
IVN6300ANE	60	7.5	TO-237	VN2222LM	60	7.5
IVN6300ANF	80	7.5	TO-237	—	—	—
IVN6300ANH	100	7.5	TO-237	—	—	—
IVN6300ANM	200	25.0	TO-237	VN2410M	240	10.0
IVN6300ANP	250	25.0	TO-237	VN2410M	240	10.0
IVN6300ANS	400	75.0	TO-237	—	—	—
IVN6300ANT	450	75.0	TO-237	—	—	—
IVN6300ANU	500	75.0	TO-237	—	—	—
IVN6300SNE	60	7.5	TO-52	VN10LE	60	5.0
IVN6300SNF	80	7.5	TO-52	—	—	—
IVN6300SNH	100	7.5	TO-52	—	—	—
IVN6300SNM	200	25.0	TO-52	—	—	—
IVN6300SNP	250	25.0	TO-52	—	—	—
IVN6300SNS	400	75.0	TO-52	—	—	—
IVN6300SNT	450	75.0	TO-52	—	—	—
IVN6300SNU	500	75.0	TO-52	—	—	—

MOTOROLA

Industry Part No.	BV_{DSS} (Volts)	$r_{DS(on)}$ (Ohms)	Package	Siliconix Equivalent	BV_{DSS} (Volts)	$r_{DS(on)}$ (Ohms)
MTM1N95	950	10.0	TO-3	—	—	—
MTM1N100	1000	10.0	TO-3	—	—	—
MTM2N45	450	4.0	TO-3	IRF423	450	4.0
MTM2N50	500	4.0	TO-3	IRF422	500	4.0
MTM2N85	850	8.0	TO-3	—	—	—
MTM2N90	900	8.0	TO-3	—	—	—
MTM3N35	350	3.3	TO-3	IRF323	350	2.5
MTM3N40	400	3.3	TO-3	IRF322	400	2.5
MTM3N55	550	2.5	TO-3	—	—	—
MTM3N60	600	2.5	TO-3	—	—	—
MTM4N45	450	2.0	TO-3	VN4502A	450	2.0
MTM4N50	500	2.0	TO-3	VN5002A	500	2.0
MTM5N35	350	1.5	TO-3	VN3501A	350	1.5
MTM5N40	400	1.5	TO-3	VN4001A	400	1.5
MTM6N55	550	1.5	TO-3	—	—	—
MTM6N60	600	1.5	TO-3	—	—	—
MTM7N45	450	1.2	TO-3	IRF443	450	1.1
MTM7N50	500	1.2	TO-3	IRF442	500	1.1
MTM8N12	120	0.5	TO-3	—	—	—
MTM8N15	150	0.5	TO-3	—	—	—
MTM8N18	180	0.4	TO-3	—	—	—
MTM8N20	200	0.4	TO-3	—	—	—
MTM8N35	350	0.8	TO-3	IRF343	350	0.8
MTM8N40	400	0.8	TO-3	IRF342	400	0.8
MTM10N08	80	0.33	TO-3	IRF120	100	0.3
MTM10N10	100	0.33	TO-3	IRF120	100	0.3
MTM10N12	120	0.3	TO-3	—	—	—
MTM10N15	150	0.3	TO-3	—	—	—
MTM12N05	50	0.2	TO-3	VN0601A	60	0.15
MTM12N06	60	0.2	TO-3	VN0601A	60	0.15
MTM12N08	80	0.25	TO-3	VN0801A	80	0.25
MTM12N10	100	0.25	TO-3	VN1001A	100	0.25

MOSPOWER Cross Reference List (Cont'd)

MOTOROLA (Cont'd)

Industry Part No.	BV_{DSS} (Volts)	$r_{DS(on)}$ (Ohms)	Package	Siliconix Equivalent	BV_{DSS} (Volts)	$r_{DS(on)}$ (Ohms)
MTM15N05	50	0.16	TO-3	VN0601A	60	0.15
MTM15N06	60	0.16	TO-3	VN0601A	60	0.15
MTM15N35	350	0.4	TO-3	IRF353	350	0.4
MTM15N40	400	0.4	TO-3	IRF352	400	0.4
MTM15N45	450	0.5	TO-3	IRF453	450	0.5
MTM15N50	500	0.5	TO-3	IRF452	500	0.5
MTM2P45	450	6.0	TO-3	—	—	—
MTM2P50	500	6.0	TO-3	—	—	—
MTM814	80	0.4	TO-3	—	—	—
MTM815	100	0.4	TO-3	—	—	—
MTP1N95	950	10.0	TO-220	—	—	—
MTP1N100	1000	10.0	TO-220	—	—	—
MTP2N45	450	4.0	TO-220	IRF823	450	4.0
MTP2N50	500	4.0	TO-220	IRF822	500	4.0
MTP2N85	850	8.0	TO-220	—	—	—
MTP2N90	900	8.0	TO-220	—	—	—
MTP3N35	350	3.3	TO-220	IRF723	350	2.5
MTP3N40	400	3.3	TO-220	IRF722	400	2.5
MTP3N55	550	2.5	TO-220	—	—	—
MTP3N60	600	2.5	TO-220	—	—	—
MTP4N45	450	2.0	TO-220	VN4502D	450	2.0
MTP4N50	500	2.0	TO-220	VN5002D	500	2.0
MTP5N35	350	1.5	TO-220	VN3501D	350	1.5
MTP5N40	400	1.5	TO-220	VN4001D	400	1.5
MTP6N55	550	1.5	TO-220	—	—	—
MTP6N60	600	1.5	TO-220	—	—	—
MTP7N45	450	1.2	TO-220	IRF843	450	1.1
MTP7N50	500	1.2	TO-220	IRF842	500	1.1
MTP8N12	120	0.5	TO-220	—	—	—
MTP8N15	150	0.5	TO-220	—	—	—
MTP8N18	180	0.4	TO-220	—	—	—
MTP8N20	200	0.4	TO-220	—	—	—
MTP8N35	350	0.8	TO-220	IRF743	350	0.8
MTP8N40	400	0.8	TO-220	IRF742	400	0.8
MTP10N08	80	0.33	TO-220	IRF520	100	0.3
MTP10N10	100	0.33	TO-220	IRF520	100	0.3
MTP10N12	120	0.3	TO-220	—	—	—
MTP10N15	150	0.3	TO-220	—	—	—
MTP12N05	50	0.2	TO-220	VN0601D	60	0.15
MTP12N06	60	0.2	TO-220	VN0601D	60	0.15
MTP12N08	80	0.25	TO-220	VN0801D	80	0.25
MTP12N10	100	0.25	TO-220	VN1001D	100	0.25
MTP15N05	50	0.16	TO-220	VN0601D	60	0.15
MTP15N06	60	0.16	TO-220	VN0601D	60	0.15
MTP2P45	450	6.0	TO-220	—	—	—
MTP2P50	500	6.0	TO-220	—	—	—
MTP814	80	0.4	TO-220	—	—	—
MTP815	100	0.4	TO-220	—	—	—

RCA

Industry Part No.	BV_{DSS} (Volts)	$r_{DS(on)}$ (Ohms)	Package	Siliconix Equivalent	BV_{DSS} (Volts)	$r_{DS(on)}$ (Ohms)
RCA-9213A	100	2.5	TO-220	—	—	—
RCA-9213B	150	2.5	TO-220	—	—	—
RCA-9196A	100	2.5	TO-39	—	—	—
RCA-9196B	150	2.5	TO-39	—	—	—
RCA-9212A	100	0.3	TO-220	IRF520	100	0.3
RCA-9212B	150	0.3	TO-220	—	—	—
RCA-9192A	100	0.3	TO-3	IRF120	100	0.3
RCA-9192B	150	0.3	TO-3	—	—	—
RCA-9230A	100	0.15	TO-220	IRF542	100	0.11
RCA-9230B	150	0.15	TO-220	—	—	—
RCA-9195A	100	0.15	TO-3	IRF142	100	0.11
RCA-9195B	150	0.15	TO-3	—	—	—

SIEMENS

Industry Part No.	BV_{DSS} (Volts)	$r_{DS(on)}$ (Ohms)	Package	Siliconix Equivalent	BV_{DSS} (Volts)	$r_{DS(on)}$ (Ohms)
BUZ 10	50	0.10	TO-220	IRF541	60	0.085
BUZ 11	50	0.04	TO-220	—	—	—

MOSPOWER Cross Reference List (Cont'd)

SIEMENS (Cont'd)

Industry Part No.	BV_{DSS} (Volts)	$r_{DS(on)}$ (Ohms)	Package	Siliconix Equivalent	BV_{DSS} (Volts)	$r_{DS(on)}$ (Ohms)
BUZ 14	50	0.04	TO-3	—	—	—
BUZ 15	50	0.03	TO-3	—	—	—
BUZ 20	100	0.20	TO-220	VN1000D	100	0.18
BUZ 21	100	0.10	TO-220	IRF522	100	0.4
BUZ 23	100	0.20	TO-3	VN1000A	100	0.18
BUZ 24	100	0.06	TO-3	—	—	—
BUZ 25	100	0.10	TO-3	IRF540	100	0.085
BUZ 30	200	0.75	TO-220	IRF632	200	0.6
BUZ 31	200	0.20	TO-220	IRF640	200	0.18
BUZ 33	200	0.75	TO-3	IRF232	200	0.6
BUZ 34	200	0.20	TO-3	IRF240	200	0.18
BUZ 40	500	4.5	TO-220	IRF822	500	4.0
BUZ 41	500	1.1	TO-220	IRF842	500	1.1
BUZ 43	500	4.5	TO-3	IRF422	500	4.0
BUZ 44	500	1.1	TO-3	IRF442	500	1.1
BUZ 45	500	0.6	TO-3	IRF452	500	0.5
BUZ 50	1000	3.5	TO-220	—	—	—
BUZ 53	1000	3.5	TO-3	—	—	—
BUZ 54	1000	2.0	TO-3	—	—	—
BUZ 80	800	2.6	TO-220	—	—	—
BUZ 83	800	2.6	TO-3	—	—	—
BUZ 84	800	1.3	TO-3	—	—	—

SONY

Industry Part No.	BV_{DSS} (Volts)	$r_{DS(on)}$ (Ohms)	Package	Siliconix Equivalent	BV_{DSS} (Volts)	$r_{DS(on)}$ (Ohms)
2SJ54	−210	1.0	TO-220	—	—	—
2SK173	210	1.0	TO-220	IRF232	200V	0.6

SUPERTEX

Industry Part No.	BV_{DSS} (Volts)	$r_{DS(on)}$ (Ohms)	Package	Siliconix Equivalent	BV_{DSS} (Volts)	$r_{DS(on)}$ (Ohms)
VN0104N1	40	4.0	TO-3	VN67AA	60	3.5
VN0104N2	40	4.0	TO-39	VN67AB	60	3.5
VN0104N3	40	4.0	TO-92	—	—	—
VN0104N4	40	4.0	TO-202	VN46AF	40	3.0
VN0104N5	40	4.0	TO-220	VN46AD	40	3.0
VN0104N6	40	4.0	DIP	VQ1004J**	60	3.5
VN0106N1	60	4.0	TO-3	VN67AA	60	3.5
VN0106N2	60	4.0	TO-39	VN67AB	60	3.5
VN0106N3	60	4.0	TO-92	—	—	—
VN0106N4	60	4.0	TO-202	VN67AF	60	3.5
VN0106N5	60	4.0	TO-220	VN67AD	60	3.5
VN0106N6	60	4.0	DIP	VQ1004J**	60	3.5
VN0108N1	80	4.0	TO-3	2N6658	90	4.0
VN0108N2	80	4.0	TO-39	2N6661	90	4.0
VN0108N3	80	4.0	TO-92	—	—	—
VN0108N4	80	4.0	TO-202	VN88AF	80	4.0
VN0108N5	80	4.0	TO-220	VN88AD	80	4.0
VN0108N6	80	4.0	DIP	VQ1006J**	90	4.5
VN0109N1	90	4.0	TO-3	2N6658	90	4.0
VN0109N2	90	4.0	TO-39	2N6661	90	4.0
VN0109N3	90	4.0	TO-92	—	—	—
VN0109N4	90	4.0	TO-202	—	—	—
VN0109N5	90	4.0	TO-220	—	—	—
VN0109N6	90	4.0	DIP	VQ1006J**	90	4.5
VN0204N1	40	2.0	TO-3	—	—	—
VN0204N2	40	2.0	TO-39	—	—	—
VN0204N5	40	2.0	TO-220	—	—	—
VN0204N6	40	2.0	DIP	—	—	—
VN0206N1	60	2.0	TO-3	—	—	—
VN0206N2	60	2.0	TO-39	—	—	—
VN0206N5	60	2.0	TO-220	—	—	—
VN0206N6	60	2.0	DIP	—	—	—
VN0208N1	80	2.0	TO-3	—	—	—
VN0208N2	80	2.0	TO-39	—	—	—
VN0208N5	80	2.0	TO-220	—	—	—
VN0208N6	80	2.0	DIP	—	—	—
VN0209N1	90	2.0	TO-3	—	—	—
VN0209N2	90	2.0	TO-39	—	—	—
VN0209N5	90	2.0	TO-220	—	—	—
VN0209N6	90	2.0	DIP	—	—	—
VN0330N1	300	3.0	TO-3	IRF323	350	2.5
VN0330N2	300	3.0	TO-39	—	—	—

**Refer to data sheet for pinout differences

1

MOSPOWER Cross Reference List (Cont'd)

SUPERTEX (Cont'd)

Industry Part No.	BVDSS (Volts)	rDS(on) (Ohms)	Package	Siliconix Equivalent	BVDSS (Volts)	rDS(on) (Ohms)
VN0330N5	300	3.0	TO-220	IRF723	350	2.5
VN0335A1	350	1.0	TO-3	VN3500A	350	1.0
VN0335N1	350	3.0	TO-3	IRF323	350	2.5
VN0335N2	350	3.0	TO-39	—	—	—
VN0335N5	350	3.0	TO-220	IRF723	350	2.5
VN0340A1	400	1.0	TO-3	VN4000A	400	1.0
VN0340N1	400	3.0	TO-3	IRF322	400	2.5
VN0340N2	400	3.0	TO-39	—	—	—
VN0340N5	400	3.0	TO-220	IRF722	400	2.5
VN0345A1	450	1.0	TO-3	IRF441	450	0.85
VN0345N1	450	3.0	TO-3	IRF421	450	3.0
VN0345N2	450	3.0	TO-39	—	—	—
VN0345N5	450	3.0	TO-220	IRF821	450	3.0
VN0350A1	500	1.0	TO-3	IRF440	500	1.0
VN0430N1	300	0.8	TO-3	IRF343	350	0.8
VN0435N1	350	0.8	TO-3	IRF343	350	0.8
VN0440N1	400	0.8	TO-3	IRF342	400	0.8
VN0445N1	450	0.8	TO-3	IRF441	450	0.85
VN1204N1	40	0.4	TO-3	IRF123	60	0.4
VN1204N2	40	0.4	TO-39	IRFF123	60	0.4
VN1204N5	40	0.4	TO-220	IRF523	60	0.4
VN1206N1	60	0.4	TO-3	IRF123	60	0.4
VN1206N2	60	0.4	TO-39	IRFF123	60	0.4
VN1206N5	60	0.4	TO-220	IRF523	60	0.4
VN1208N1	80	0.4	TO-3	IRF122	100	0.4
VN1208N2	80	0.4	TO-30	IRFF122	100	0.4
VN1208N5	80	0.4	TO-220	IRF522	100	0.4
VN1209N1	90	0.4	TO-3	IRF122	100	0.4
VN1209N2	90	0.4	TO-39	IRFF122	100	0.4
VN1209N5	90	0.4	TO-220	IRF522	90	0.4
VN1304N2	40	10.0	TO-39	VN90AB	60	5.0
VN1304N3	40	10.0	TO-92	VN2222L	60	7.5
VN1304N6	40	10.0	DIP	VQ1000J**	90	5.5
VN1306N2	60	10.0	TO-39	VN90AB	60	5.0
VN1306N3	60	10.0	TO-92	VN2222L	60	7.5
VN1306N6	60	10.0	DIP	VQ1000J**	90	5.5
VN1308N2	80	10.0	TO-39	VN90AB	90	5.0
VN1308N3	80	10.0	TO-92	—	—	—
VN1308N6	80	10.0	DIP	VQ1006J**	90	4.5
VN1309N2	90	10.0	TO-39	VN90AB	90	5.0
VN1309N3	90	10.0	TO-92	—	—	—
VN1309N6	90	10.0	DIP	VQ1006J**	90	4.5
VP0104N1	−40	8.0	TO-3	—	—	—
VP0104N2	−40	8.0	TO-39	VP0808B	−60	5.0
VP0104N3	−40	8.0	TO-92	VP0808L	−60	5.0
VP0104N5	−40	8.0	TO-220	—	—	—
VP0104N6	−40	8.0	DIP	—	—	—
VP0106N1	−60	8.0	TO-3	—	—	—
VP0106N2	−60	8.0	TO-39	VP0808B	−60	5.0
VP0106N3	−60	8.0	TO-92	VP0808L	−60	5.0
VP0106N5	−60	8.0	TO-220	—	—	—
VP0106N6	−60	8.0	DIP	—	—	—
VP0108N1	−80	8.0	TO-3	—	—	—
VP0108N2	−80	8.0	TO-39	VP0808B	−80	5.0
VP0108N3	−80	8.0	TO-92	VP0808L	−80	5.0
VP0108N5	−80	8.0	TO-220	—	—	—
VP0108N6	−80	8.0	DIP	—	—	—
VP0109N1	−90	8.0	TO-3	—	—	—
VP0109N2	−90	8.0	TO-39	VP1008B	−100	5.0
VP0109N3	−90	8.0	TO-92	VP1008L	−100	5.0
VP0109N5	−90	8.0	TO-220	—	—	—
VP0109N6	−90	8.0	DIP	—	—	—
VP0204N1	−40	4.0	TO-3	—	—	—
VP0204N2	−40	4.0	TO-39	—	—	—
VP0204N5	−40	4.0	TO-220	—	—	—
VP0204N6	−40	4.0	DIP	—	—	—
VP0206N1	−60	4.0	TO-3	—	—	—
VP0206N2	−60	4.0	TO-39	—	—	—
VP0206N5	−60	4.0	TO-220	—	—	—
VP0206N6	−60	4.0	DIP	—	—	—
VP0208N1	−80	4.0	TO-3	—	—	—

**Refer to data sheet for pinout differences

MOSPOWER Cross Reference List (Cont'd)

SUPERTEX (Cont'd)

Industry Part No.	BV_{DSS} (Volts)	$r_{DS(on)}$ (Ohms)	Package	Siliconix Equivalent	BV_{DSS} (Volts)	$r_{DS(on)}$ (Ohms)
VP0208N2	−80	4.0	TO-39	—	—	—
VP0208N5	−80	4.0	TO-220	—	—	—
VP0208N6	−80	4.0	DIP	—	—	—
VP0209N1	−90	4.0	TO-3	—	—	—
VP0209N2	−90	4.0	TO-39	—	—	—
VP0209N5	−90	4.0	TO-220	—	—	—
VP0209N6	−90	4.0	DIP	—	—	—
VP1204N1	−40	0.8	TO-3	IRF9133*	−60	0.4
VP1204N2	−40	0.8	TO-39	—	—	—
VP1204N5	−40	0.8	TO-220	IRF9523*	−60	0.8
VP1206N1	−60	0.8	TO-3	IRF9133*	−60	0.4
VP1206N2	−60	0.8	TO-39	—	—	—
VP1206N5	−60	0.8	TO-220	IRF9523*	−100	0.8
VP1208N1	−80	0.8	TO-3	IRF9132*	−100	0.4
VP1208N2	−80	0.8	TO-39	—	—	—
VP1208N5	−80	0.8	TO-220	IRF9522*	−100	0.8
VP1209N1	−90	0.8	TO-3	IRF9132*	−100	0.4
VP1209N2	−90	0.8	TO-39	—	—	—
VP1209N5	−90	0.8	TO-220	IRF9522*	−100	0.8

*Product family available by March 1983

MOSPOWER

Introduction 1
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IRFF120 ■ IRFF121 ■ IRFF122 ■ IRFF123

Siliconix
Advanced Information

100V N-Channel Enhancement Mode MOSPOWER

These power FETs are designed especially for offline switching regulators, power converters, solenoid and relay drivers.

FEATURES

- No Second Breakdown
- High Input Impedance
- Internal Drain-Source Diode
- Very Rugged: Excellent SOA
- Extremely Fast Switching

BENEFITS

- Reduced Component Count
- Improved Performance
- Simpler Designs
- Improved Reliability

Product Summary

Part Number	BV_{DSS}	$R_{DS(ON)}$	I_D	Package
IRFF120	100V	0.30Ω	6A	TO-39
IRFF121	60V			
IRFF122	100V	0.40Ω	5A	
IRFF123	60V			

ABSOLUTE MAXIMUM RATINGS ($T_C = 25°C$ unless otherwise noted)

Drain-Source Voltage
- IRFF120,IRFF122 .... 100V
- IRFF121,IRFF123 .... 60V

Drain-Gate Voltage
- IRFF120,IRFF122 .... 100V
- IRFF121,IRFF123 .... 60V

Drain Current Continuous[1]
- IRFF120,IRFF121 .... ± 6A
- IRFF122,IRFF124 .... ± 5A

Pulsed[2]................................. ± 24A

Gate Current (Peak) .... ± 3A

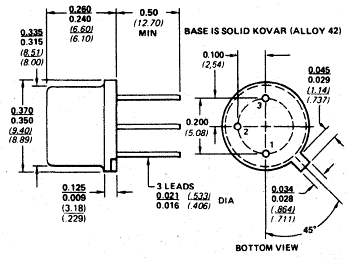
Gate Source Voltage .... ± 40V

Total Power Dissipation 20W
- Linear Derating Factor .... 0.16W/°C

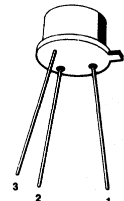
Storage and Junction Temperature ....-55°C to +150°C

Notes:
1. Limited by package dissipation.
2. Pulse test—80μs to 300μs, 1% duty cycle.

PACKAGE DIMENSIONS



PIN 1 — Source
PIN 2 — Gate
PIN 3 & CASE — Drain



TO-39

ELECTRICAL CHARACTERISTICS ($T_C = 25°C$ unless otherwise noted)

Symbol	Parameter	Part Number	Min	Typ	Max	Unit	Test Conditions
Static							
BV_{DSS}	Drain-Source Breakdown	IRFF 120 IRFF 122	100			V	$V_{GS} = 0$, $I_D = 250 \mu A$
		IRFF 121 IRFF 123	60				
$V_{GS(th)}$	Gate Threshold Voltage	All	2		4	V	$V_{GS} = V_{DS}$, $I_D = 1 mA$
I_{GSS}	Gate Body Leakage	All			±100	nA	$V_{GS} = \pm 20V$, $V_{DS} = 0$
I_{DSS}	Zero Gate Voltage Drain Current	All		0.1	0.25	mA	V_{DS} = Rated V_{DS}, $V_{GS} = 0$
				0.2	1		V_{DS} = Rated V_{DS}, $V_{GS} = 0$, $T_C = 125°C$
$r_{DS(on)}$	Drain-Source On Resistance	IRFF 120 IRFF 121		0.25	0.30	Ω	$V_{GS} = 10V$, $I_D = 3A$ (Note 1)
		IRFF 122 IRFF 123		0.30	0.40		
$I_{D(on)}$	On-State Drain Current	All	6			A	$V_{DS} = 15V$, $V_{GS} = 10V$ (Note 1)
Dynamic							
g_{fs}	Forward Transconductance	All	1.5	2.5		S	$V_{DS} = 25V$, $I_{DS} = 3A$ (Note 1)
C_{iss}	Input Capacitance	All		450	600	pF	$V_{GS} = 0$, $V_{DS} = 25V$, $f = 1 MHz$
C_{rss}	Reverse Transfer Capacitance	All		50	100		
C_{oss}	Common-Source Output Capacitance	All		200	400		
$t_{d(on)}$	Turn-On Delay Time	All		20	40	ns	$V_{DD} = 30V$, $I_D \approx 3A$, $R_L = 10Ω$, $R_g = 10Ω$ (Figure 1)
t_r	Rise Time	All		35	70		
$t_{d(off)}$	Turn-Off Delay Time	All		50	100		
t_f	Fall Time	All		35	70		
Drain-Source Diode Characteristics							
V_{SD}	Forward ON Voltage	All		−2.5		V	$I_S = -6A$, $V_{GS} = 0$ (Note 1)
t_{rr}	Reverse Recovery Time	All		150		ns	$I_F = -6A$, $V_{GS} = 0$, $di/dt = 100 A/\mu s$ (Figure 2)

Note 1: Pulse Test—80µs to 300 µs, 1% duty cycle

TEST CIRCUITS

FIGURE 1 Switching Test Circuit

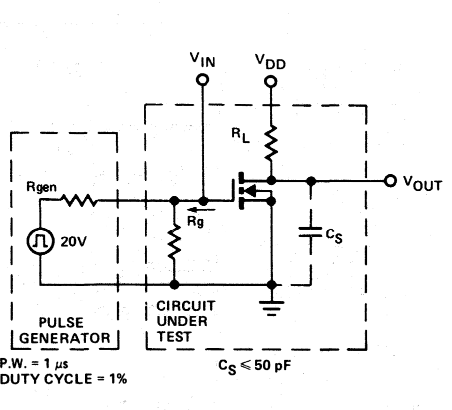
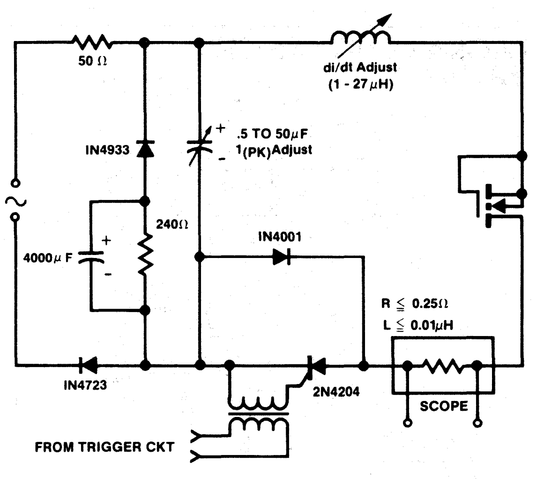


FIGURE 2 Reverse Recovery Test Circuit



IRF120 ■ IRF121 ■ IRF122 ■ IRF123
IRF520 ■ IRF521 ■ IRF522 ■ IRF523

Advanced Information

100V N-Channel Enhancement Mode MOSPOWER

These power FETs are designed especially for off-line switching regulators, converters, solenoid and relay drivers.

FEATURES

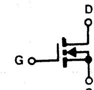
- High Voltage
- No Second Breakdown
- High Input Impedance
- Internal Drain-Source Diode
- Very Rugged: Excellent SOA
- Extremely Fast Switching

BENEFITS

- Reduced Component Count
- Improved Performance
- Simpler Designs
- Improved Reliability

Product Summary

Part Number	BV_{DSS}	$R_{DS(ON)}$	I_D	Package
IRF120	100V	0.30Ω	8A	TO-3
IRF121	60V			
IRF122	100V	0.40Ω	7A	
IRF123	60V			
IRF520	100V	0.30Ω	8A	TO-220AB
IRF521	60V			
IRF522	100V	0.40Ω	7A	
IRF523	60V			



ABSOLUTE MAXIMUM RATINGS (T_C = 25°C unless otherwise noted)

Drain-Source Voltage
- IRF120, 122, 520, 522 .... 100V
- IRF121, 123, 521, 523 .... 60V

Drain-Gate Voltage
- IRF120, 122, 520, 522 .... 100V
- IRF121, 123, 521, 523 .... 60V

Drain Current Continuous
- IRF120, 121, 520, 521 .... ±8A
- IRF122, 123, 522, 523 .... ±7A

Drain Current
Pulsed (80μs to 300μs, 1% duty cycle) .... ±32A

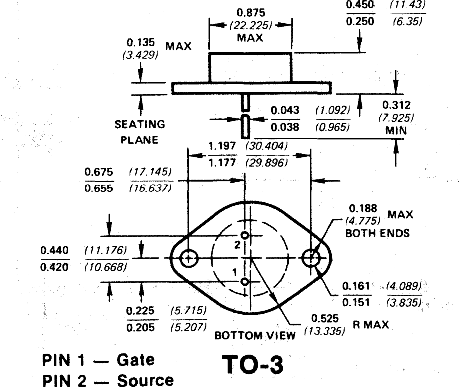
Gate Current (Peak) .... ±3A

Gate-Source Voltage .... ±40V

Total Power Dissipation .... 40 W
Linear Derating Factor .... 0.32 W/°C

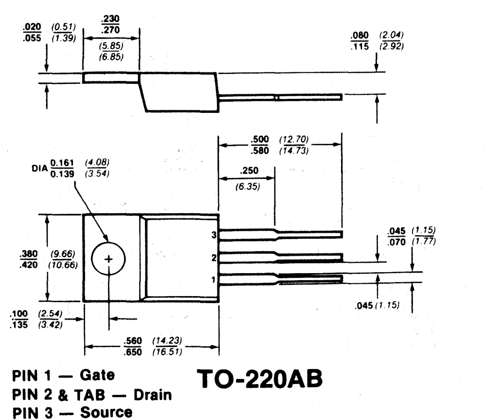
Operating and Storage
Temperature .... -55°C to +150°C

PACKAGE DIMENSIONS



PIN 1 — Gate
PIN 2 — Source
CASE — Drain

TO-3



PIN 1 — Gate
PIN 2 & TAB — Drain
PIN 3 — Source

TO-220AB

ELECTRICAL CHARACTERISTICS ($T_C = 25°C$ unless otherwise noted)

Symbol	Parameter	Part Number	Min	Typ	Max	Unit	Test Conditions
Static							
BV_{DSS}	Drain-Source Breakdown Voltage	IRF120, 520 IRF122, 522	100			V	$V_{GS} = 0$, $I_D = 250\mu A$
		IRF121, 521 IRF123, 523	60				
$V_{GS(th)}$	Gate Threshold Voltage	All	2.0		4.0	V	$V_{DS} = V_{GS}$, $I_D = 1$ mA
I_{GSS}	Gate-Body Leakage	All			±100	nA	$V_{GS} = \pm 20V$, $V_{DS} = 0$
I_{DSS}	Zero Gate Voltage Drain Current	All		0.1	0.25	mA	V_{DS} = Rated V_{DS}, $V_{GS} = 0$
				0.2	1.0		V_{DS} = Rated V_{DS}, $V_{GS} = 0$, $T_C = 125°C$
$I_{D(on)}$	On-State Drain Current	All	8.0			A	$V_{DS} = 25V$, $V_{GS} = 10V$ (Note 1)
$r_{DS(on)}$	Static Drain-Source On-State Resistance	IRF120, 121 IRF520, 521		0.25	0.30	Ω	$V_{GS} = 10V$, $I_D = 4A$ (Note 1)
		IRF122, 123 IRF522, 523		0.30	0.40		
Dynamic							
g_{fs}	Forward Transconductance	All	1.5	2.5		S	$V_{DS} = 25V$, $I_D = 4A$ (Note 1)
C_{iss}	Input Capacitance	All		450	600	pF	$V_{GS} = 0$, $V_{DS} = 25V$, f = 0.1 MHz
C_{oss}	Output Capacitance			200	400		
C_{rss}	Reverse Transfer Capacitance			50	100		
$t_{d(on)}$	Turn-On Delay Time	All		20	40	ns	$V_{DD} = 30V$, $I_D \approx 4A$, $R_L = 7\Omega$, $R_g = 25\Omega$ (Figure 1)
t_r	Rise Time	All		35	70		
$t_{d(off)}$	Turn-Off Delay Time	All		50	100		
t_f	Fall Time	All		35	70		
Drain-Source Diode Characteristics							
V_{SD}	Forward On Voltage	All		−1.9		V	$I_S = -8A$ (Note 1)
t_{rr}	Reverse Recovery Time	All		150		ns	$I_F = -8A$, $V_{GS} = 0$, di/dt = 100A/µs (Fig. 2)

Note 1: Pulse test — 80 µs to 300 µs, 1% duty cycle

TEST CIRCUITS

FIGURE 1 Switching Test Circuit

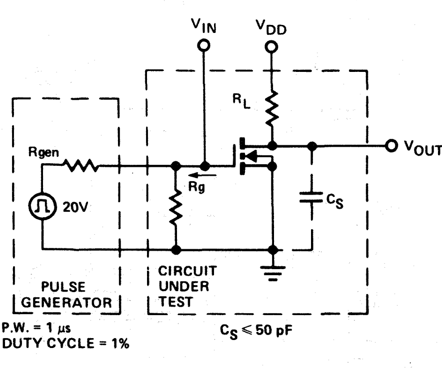
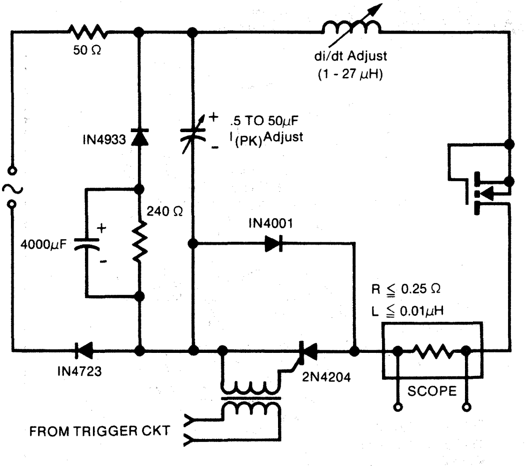


FIGURE 2 JEDEC Reverse Recovery Circuit



IRF130 ■ IRF131 ■ IRF132 ■ IRF133
IRF530 ■ IRF531 ■ IRF532 ■ IRF533

Siliconix

100V N-Channel Enhancement Mode MOSPOWER

These power FETs are designed especially for audio amplifiers, power converters, and drivers for motors, solenoids and relays.

FEATURES

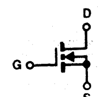
- No Second Breakdown
- High Input Impedance
- Internal Drain-Source Diode
- Very Rugged: Excellent SOA
- Extremely Fast Switching

BENEFITS

- Reduced Component Count
- Improved Performance
- Simpler Designs
- Improved Reliability

Product Summary

Part Number	BV_{DSS}	$R_{DS(ON)}$	I_D	Package
IRF130	100V	0.18Ω	14A	TO-3
IRF131	60V			
IRF132	100V	0.25Ω	12A	
IRF133	60V			
IRF530	100V	0.18Ω	14A	TO-220AB
IRF531	60V			
IRF532	100V	0.25Ω	12A	
IRF533	60V			



ABSOLUTE MAXIMUM RATINGS (T_C = 25°C unless otherwise noted)

Drain-Source Voltage
- IRF130,132; IRF530,532 .... 100V
- IRF131,133; IRF531,533 .... 60V

Drain-Gate Voltage
- IRF130,132; IRF530,532 .... 100V
- IRF131,133; IRF531,533 .... 60V

Drain Current Continuous
- IRF130, 131, 530, 531 .... ±14A
- IRF132, 133, 532, 533 .... ±12A

Drain Current
Pulsed (80μs to 300μs, 1% duty cycle) .... ±56A

Gate Current (Peak) .... ±3A

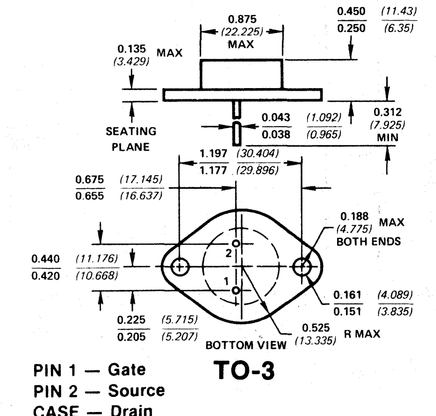
Gate-Source Voltage .... ±40V

Total Power Dissipation 75W

Linear Derating Factor .... 0.6W/°C

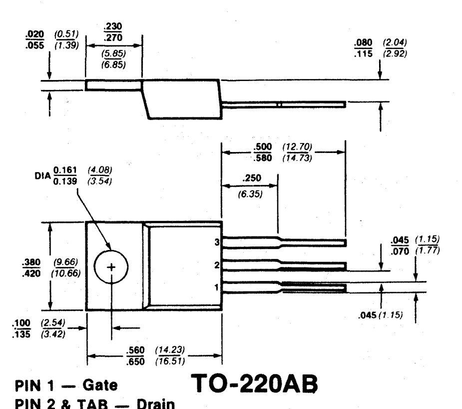
Operating and Storage Temperature .... -55°C to + 150°C

PACKAGE DIMENSIONS



TO-3

PIN 1 — Gate
PIN 2 — Source
CASE — Drain



TO-220AB

PIN 1 — Gate
PIN 2 & TAB — Drain
PIN 3 — Source

ELECTRICAL CHARACTERISTICS ($T_C = 25°C$ unless otherwise noted)

Parameter		Part Number	Min	Typ	Max	Unit	Test Conditions
Static							
BV_{DSS}	Drain-Source Breakdown Voltage	IRF130, 132 IRF530, 532	100			V	$V_{GS} = 0$, $I_D = 250\mu A$
		IRF131, 133 IRF531, 533	60				
$V_{GS(th)}$	Gate Threshold Voltage	All	2.0		4.0	V	$V_{GS} = V_{DS}$, $I_D = 1$ mA
I_{GSS}	Gate-Body Leakage	All			±100	nA	$V_{GS} = \pm 20V$, $V_{DS} = 0$
I_{DSS}	Zero Gate Voltage Drain Current	All			0.25	mA	V_{DS} = Rated V_{DS}, $V_{GS} = 0$
					1.0		V_{DS} = Rated V_{DS}, $V_{GS} = 0$, $T_C = 125°C$
$V_{DS(on)}$	Drain-Source ON-State Voltage	IRF130, 131 IRF530, 531			1.44	V	$V_{GS} = 10V$, $I_D = 8A$, (Note 1)
		IRF132, 133 IRF532, 533			2.0		
$r_{DS(on)}$	Drain-Source On Resistance	IRF130, 131 IRF530, 531			0.18	Ω	$V_{GS} = 10V$, $I_D = 8A$ (Note 1)
		IRF132, 133 IRF532, 533			0.25		
$I_{D(on)}$	On-State Drain Current	All	14			A	$V_{DS} = 25V$, $V_{GS} = 10V$, (Note 1)
Dynamic							
g_{fs}	Forward Transconductance	All	4.0			S	$V_{DS} = 25V$, $I_D = 8A$, (Note 1)
C_{iss}	Input Capacitance	All			800	pF	$V_{GS} = 0$, $V_{DS} = 25V$, f = 1 MHz
C_{rss}	Reverse Transfer Capacitance	All			150		
C_{oss}	Output Capacitance	All			500		
$t_{d(on)}$	Turn-On Delay Time	All			30	ns	$V_{DD} = 30V$, $I_D \approx 8A$, $R_L = 3.5\Omega$, $R_g = 10\Omega$ (Figure 1)
t_r	Rise Time	All			75		
$t_{d(off)}$	Turn-Off Delay Time	All			40		
t_f	Fall Time	All			45		
Drain-Source Diode Characteristics							
V_{SD}	Forward On Voltage	All		−1.5		V	$I_S = -14A$, $V_{GS} = 0$ (Note 1)
t_{rr}	Reverse Recovery Time	All		300		ns	$I_F = -14A$, di/dt = 100A/μs, $V_{GS} = 0$ (Figure 2)

Note 1: Pulse test — 80 μs to 300 μs, 1% duty cycle

Refer to VNDA12 Design Curves (See Section 4)

TEST CIRCUITS

FIGURE 1 Switching Test Circuit

V_{IN} V_{DD} R_L Rgen Rg V_{OUT} C_S

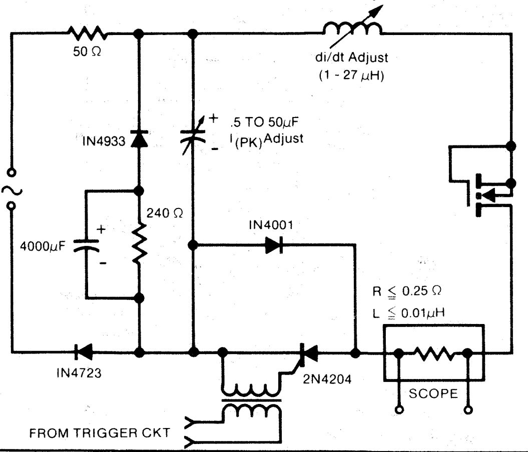
PULSE GENERATOR

CIRCUIT UNDER TEST

P.W. = 1 μs
DUTY CYCLE = 1%

$C_S \leq 50$ pF

FIGURE 2 JEDEC Reverse Recovery Circuit



IRF140 ■ IRF141 ■ IRF142 ■ IRF143
IRF540 ■ IRF541 ■ IRF542 ■ IRF543

Siliconix

Advance Information

100V N-Channel Enhancement-Mode MOSPOWER

These power FETs are designed especially for switching regulators, converters, solenoid drivers, relay drivers and audio amplifiers.

FEATURES

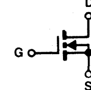
- Low On Resistance
- No Second Breakdown
- High Input Impedance
- Internal Drain-Source Diode
- Very Rugged: Excellent SOA
- Extremely Fast Switching

BENEFITS

- Reduced Component Count
- Improved Performance
- Simpler Designs
- Improved Reliability

Product Summary

Part Number	BV_{DSS}	$r_{DS(ON)}$	I_D	Package
IRF140	100V	0.085Ω	27A	TO-3
IRF141	60V			
IRF142	100V	0.11Ω	24A	
IRF143	60V			
IRF540	100V	0.085Ω	27A	TO-220AB
IRF541	60V			
IRF542	100V	0.11Ω	24A	
IRF543	60V			



ABSOLUTE MAXIMUM RATINGS (T_C=25°C unless otherwise noted)

Drain-Source Voltage
- IRF140, 142, 540, 542 .... 100V
- IRF141, 143, 541, 543 .... 60V

Drain-Gate Voltage
- IRF140, 142, 540, 542 .... 100V
- IRF141, 143, 541, 543 .... 60V

Drain Current
- Continuous
  - IRF140, 141, 540, 541 .... ± 27A
  - IRF142, 143, 542, 543 .... ± 24A
- Pulsed[2] .... ±108A

Gate Current (Peak) .... ± 3A

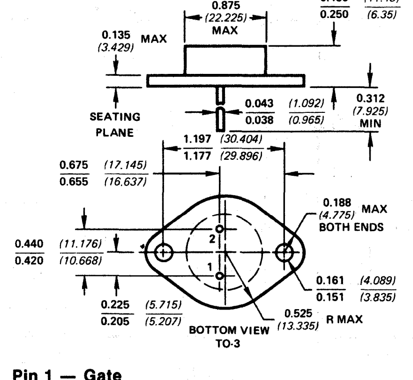
Gate-Source Voltage .... ±40V

Total Power Dissipation 125W
- Linear Derating Factor .... 1.0W/°C

Operating and
- Storage Temperature .... −55°C to +150°C

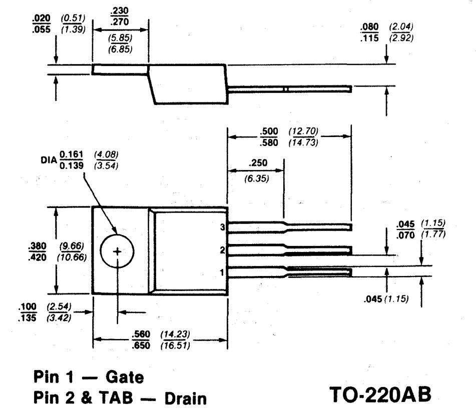
Notes:
1. Limited by package dissipation.
2. Pulse test—80μs to 300μs, 1% duty cycle.

PACKAGE DIMENSIONS



Pin 1 — Gate
Pin 2 — Source
CASE — Drain

TO-3



Pin 1 — Gate
Pin 2 & TAB — Drain
Pin 3 — Source

TO-220AB

ELECTRICAL CHARACTERISTICS ($T_C = 25°C$ unless otherwise noted)

	Parameter	Part Number	Min	Typ	Max	Unit	Test Conditions
			Static				
BV_{DSS}	Drain-Source Breakdown Voltage	IRF140, 142 IRF540, 542	100			V	$V_{GS} = 0$, $I_D = 250\mu A$
		IRF141, 143 IRF541, 543	60				
$V_{GS(th)}$	Gate Threshold Voltage	All	2.0		4.0	V	$V_{DS} = V_{GS}$, $I_D = 1$ mA
I_{GSS}	Gate-Body Leakage				±100	nA	$V_{GS} = \pm 20V$, $V_{DS} = 0$
I_{DSS}	Zero Gate Voltage Drain Current	All		0.1	0.25	mA	V_{DS} = Rated V_{DS}, $V_{GS} = 0V$
				0.2	1.0		V_{DS} = Rated V_{DS}, $V_{GS} = 0V$, $T_C = 125°C$
$I_{D(on)}$	On-State Drain Current	IRF140, 141 IRF540, 541	27			A	$V_{DS} = 25V$, $V_{GS} = 10V$ (Note 1)
		IRF142, 143 IRF542, 543	24				
$r_{DS(on)}$	Static Drain-Source On-State Resistance	IRF140, 141 IRF540, 541		0.07	0.085	Ω	$V_{GS} = 10V$, $I_D = 15A$ (Note 1)
		IRF142, 143 IRF542, 543		0.09	0.11		
			Dynamic				
g_{fs}	Forward Transconductance	All	6.0	10.0		S	$V_{DS} = 25V$, $I_D = 15A$ (Note 1)
C_{iss}	Input Capacitance	All		1275	1600	pF	$V_{GS} = 0$, $V_{DS} = 25V$, f = 1 MHz
C_{oss}	Output Capacitance			550	800		
C_{rss}	Reverse Transfer Capacitance			160	300		
$t_{d(on)}$	Turn-On Delay Time	All		16	30	ns	$V_{DD} = 30V$, $I_D \approx 15A$, $R_L = 2\Omega$, $R_g = 10\Omega$
t_r	Rise Time	All		27	60		
$t_{d(off)}$	Turn-Off Delay Time	All		38	80		
t_f	Fall Time	All		14	30		
			Drain-Source Diode Characteristics				
V_{SD}	Forward On Voltage	All		−2.50		V	$I_S = -27A$, $V_{GS} = 0$ (Note 1)
t_{rr}	Reverse Recovery Time	All		250		ns	$I_F = -27A$, $V_{GS} = 0$, di/dt = 100A/μs

Note 1: Pulse test 80 μs to 300 μs, 1% duty cycle

TEST CIRCUITS

FIGURE 1 Switching Test Circuit

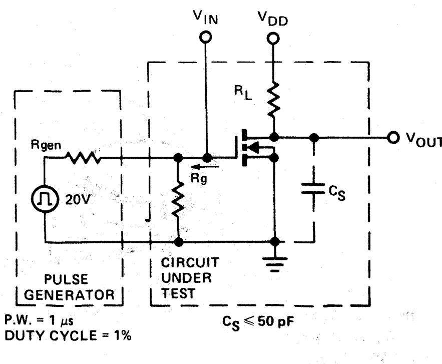
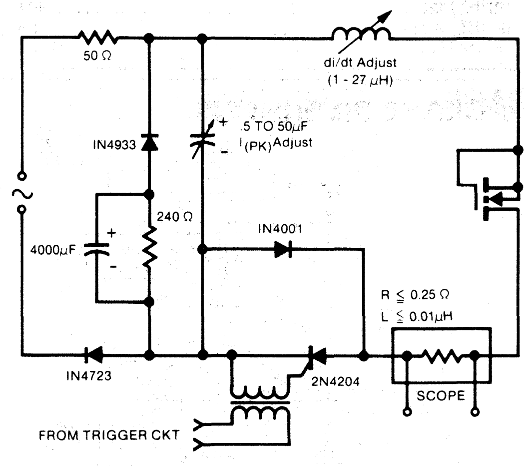
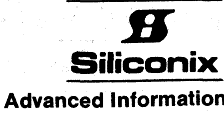


FIGURE 2 Reverse Recovery Test Circuit



IRF150 ■ IRF151 ■ IRF152 ■ IRF153



Advanced Information

100V N-Channel Enhancement Mode MOSPOWER

These power FETs are designed especially for off-line switching regulators, converters, solenoid and relay drivers.

FEATURES

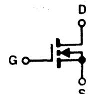
- High Voltage
- No Second Breakdown
- High Input Impedance
- Internal Drain-Source Diode
- Very Rugged: Excellent SOA
- Extremely Fast Switching

BENEFITS

- Reduced Component Count
- Improved Performance
- Simpler Designs
- Improved Reliability

Product Summary

Part Number	BV_{DSS}	$R_{DS(ON)}$	I_D	Package
IRF150	100V	0.055Ω	40A	TO-3
IRF151	60V			
IRF152	100V	0.08Ω	33A	
IRF153	60V			



ABSOLUTE MAXIMUM RATINGS (T_C = 25°C unless otherwise noted)

Drain-Source Voltage
- IRF150 .... 100V
- IRF151 .... 60V
- IRF152 .... 100V
- IRF153 .... 60V

Drain-Gate Voltage
- IRF150 .... 100V
- IRF151 .... 60V
- IRF152 .... 100V
- IRF153 .... 60V

Drain Current Continuous
- IRF150, 151 .... 40A
- IRF152, 153 .... 33A

Drain Current
Pulsed (80μs to 300μs, 1% duty cycle) .... ±160A

Gate Current (Peak) .... ±3A

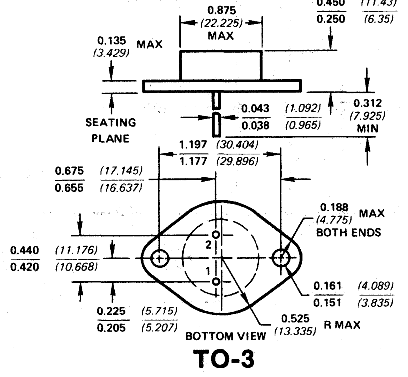
Gate-Source Voltage .... ±40V

Total Power Dissipation 150W

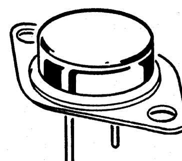
Linear Derating Factor .... 1.2W/°C

Operating and Storage Temperature .... -55°C to + 150°C

PACKAGE DIMENSIONS



TO-3



PIN 1 — Gate
PIN 2 — Source
CASE — Drain

ELECTRICAL CHARACTERISTICS ($T_C = 25°C$ unless otherwise noted)

Symbol	Parameter	Part Number	Min	Typ	Max	Unit	Test Conditions
Static							
BV_{DSS}	Drain-Source Breakdown Voltage	IRF150 IRF152	100			V	$V_{GS} = 0$, $I_D = 250\mu A$
		IRF151 IRF153	60				
$V_{GS(th)}$	Gate Threshold Voltage	All	2		4.0	V	$V_{DS} = V_{GS}$, $I_D = 1$ mA
I_{GSS}	Gate-Body Leakage	All			±100	nA	$V_{GS} = \pm 20V$, $V_{DS} = 0$
I_{DSS}	Zero Gate Voltage Drain Current	All		0.1	0.25	mA	V_{DS} = Rated V_{DS}, $V_{GS} = 0V$
				0.2	1.0		V_{DS} = Rated V_{DS}, $V_{GS} = 0V$, $T_C = 125°C$
$I_{D(on)}$	On-State Drain Current	All	40			A	$V_{DS} = 25V$, $V_{GS} = 10V$ (Note 1)
$r_{DS(on)}$	Static Drain-Source On-State Resistance	IRF150 IRF151		0.045	0.055	Ω	$V_{GS} = 10V$, $I_D = 20A$ (Note 1)
		IRF152 IRF153		0.06	0.08		
Dynamic							
g_{fs}	Forward Transconductance	All	9	10		S	$V_{DS} = 25V$, $I_D = 20A$ (Note 1)
C_{iss}	Input Capacitance	All		2500	3000	pF	$V_{GS} = 0$, $V_{DS} = 25V$, f = 1 MHz
C_{oss}	Output Capacitance			1000	1500		
C_{rss}	Reverse Transfer Capacitance			350	500		
$t_{d(on)}$	Turn-On Delay Time	All			35	ns	$V_{DD} = 30V$, $I_D \approx 20A$, $R_L = 1.5\Omega$, $R_g = 10\Omega$, (Fig. 1)
t_r	Rise Time	All			100		
$t_{d(off)}$	Turn-Off Delay Time	All			125		
t_f	Fall Time	All			100		
Drain-Source Diode Characteristics							
V_{SD}	Forward On Voltage	All		−1.7		V	$I_S = -40A$ (Note 1)
t_{rr}	Reverse Recovery Time	All		500		ns	$I_F = -40A$, $V_{GS} = 0$, di/dt = 100A/μs (Fig. 2)

Note 1: Pulse test — 80 μs to 300 μs, 1% duty cycle

TEST CIRCUITS

FIGURE 1 Switching Test Circuit

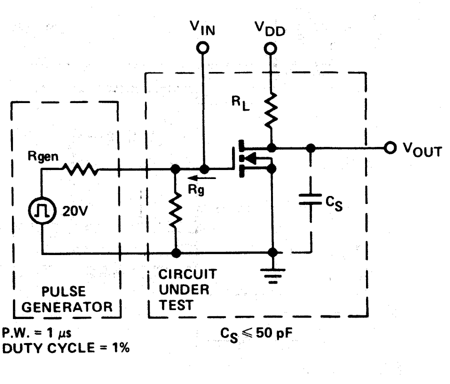
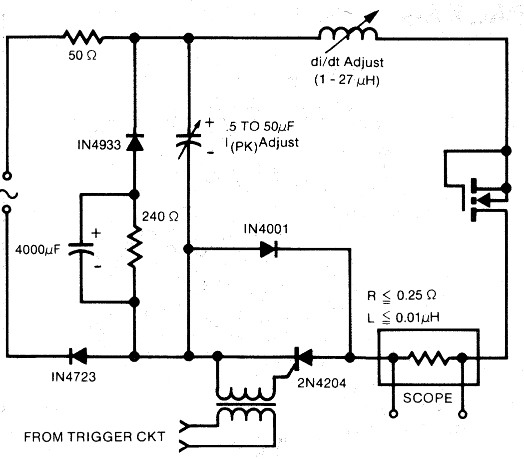


FIGURE 2 JEDEC Reverse Recovery Circuit



IRF220 ■ IRF221 ■ IRF222 ■ IRF223
IRF620 ■ IRF621 ■ IRF622 ■ IRF623

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Advanced Information

200V N-Channel Enhancement Mode MOSPOWER

These power FETs are designed especially for switching regulators, power converters, solenoid drivers and relay drivers.

FEATURES

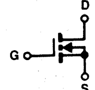
- No Second Breakdown
- High Input Impedance
- Internal Drain-Source Diode
- Very Rugged: Excellent SOA
- Extremely Fast Switching

BENEFITS

- Reduced Component Count
- Improved Performance
- Simpler Designs
- Improved Reliability

Product Summary

Part Number	BV_{DSS}	$R_{DS(ON)}$	I_D	Package
IRF220	200V	0.8Ω	5.0A	TO-3
IRF221	150V			
IRF222	200V	1.2Ω	4.0A	
IRF223	150V			
IRF620	200V	0.8Ω	5.0A	TO-220AB
IRF621	150V			
IRF622	200V	1.2Ω	4.0A	
IRF623	150V			



ABSOLUTE MAXIMUM RATINGS ($T_C = 25°C$ unless otherwise noted)

Drain-Source Voltage
- IRF220,222,620,622 .... 200V
- IRF221,223,621,623 .... 150V

Drain-Gate Voltage
- IRF220,222,620,622 .... 200V
- IRF221,223,621,623 .... 150V

Drain Current Continuous[1]
- IRF220,221,620,621 .... ± 5.0A
- IRF222,223,622,623 .... ± 4.0A

Pulsed[2] .... ± 20A

Gate Current (Peak) .... ± 2A

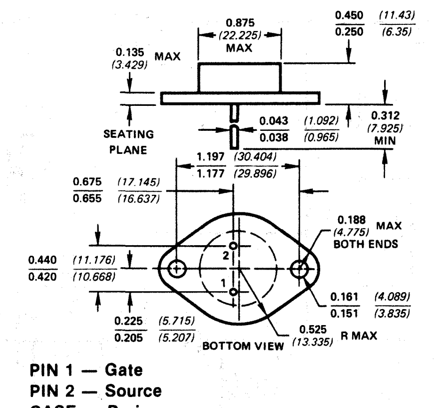
Gate Source Voltage .... ± 40V

Total Power Dissipation 40W
- Linear Derating Factor .... 0.32W/°C

Storage and Junction
- Temperature .... -55°C to +150°C

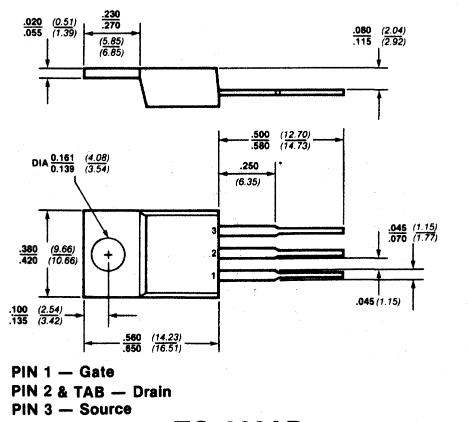
Notes:
1. Limited by package dissipation.
2. Pulse test—80μs to 300μs, 1% duty cycle.

PACKAGE DIMENSIONS



PIN 1 — Gate
PIN 2 — Source
CASE — Drain

TO-3



PIN 1 — Gate
PIN 2 & TAB — Drain
PIN 3 — Source

TO-220AB

ELECTRICAL CHARACTERISTICS ($T_C = 25°C$ unless otherwise noted)

Symbol	Parameter	Part Number	Min	Typ	Max	Unit	Test Conditions
Static							
BV_{DSS}	Drain-Source Breakdown	IRF 220, 222 IRF 620, 622	200			V	$V_{GS} = 0$, $I_D = 250\mu A$
		IRF 221, 223 IRF 621, 623	150				
$V_{GS(th)}$	Gate Threshold Voltage	All	2		4	V	$V_{GS} = V_{DS}$, $I_D = 1\,mA$
I_{GSS}	Gate Body Leakage	All			±100	nA	$V_{GS} = \pm 20V$, $V_{DS} = 0$
I_{DSS}	Zero Gate Voltage Drain Current	All		0.1	0.25	mA	V_{DS} = Rated V_{DS}, $V_{GS} = 0$
				0.2	1.0		V_{DS} = Rated V_{DS}, $V_{GS} = 0$, $T_C = 125°C$
$r_{DS(on)}$	Drain-Source On Resistance	IRF 220, 221 IRF 620, 621		0.5	0.8	Ω	$V_{GS} = 10V$, $I_D = 2.5A$ (Note 1)
		IRF 222, 223 IRF 622, 623		0.8	1.2		
$I_{D(on)}$	On-State Drain Current	All	5			A	$V_{DS} = 25V$, $V_{GS} = 10V$ (Note 1)
Dynamic							
g_{fs}	Forward Transconductance	All	1.3	2.3		S	$V_{DS} = 25V$, $I_D = 2.5A$ (Note 1)
C_{iss}	Input Capacitance	All		450	600	pF	$V_{GS} = 0$, $V_{DS} = 25V$, $f = 1\,MHz$
C_{rss}	Reverse Transfer Capacitance	All		40	80		
C_{oss}	Common-Source Output Capacitance	All		150	300		
$t_{d(on)}$	Turn-On Delay Time	All			40	ns	$V_{DD} = 75V$, $I_D \approx 2.5A$, $R_L = 30\Omega$, $R_g = 25\Omega$, (Figure 1)
t_r	Rise Time	All			60		
$t_{d(off)}$	Turn-Off Delay Time	All			100		
t_f	Fall Time	All			60		
Drain-Source Diode Characteristics							
V_{SD}	Forward ON Voltage	All		−1.57		V	$I_S = -5A$, $V_{GS} = 0$ (Note 1)
t_{rr}	Reverse Recovery Time	All		450		ns	$I_F = -5A$, $V_{GS} = 0$, $di/dt = 100\,A/\mu s$ (Figure 2)

Note 1: Pulse Test—80μs to 300 μs, 1% duty cycle

TEST CIRCUITS

FIGURE 1 Switching Test Circuit

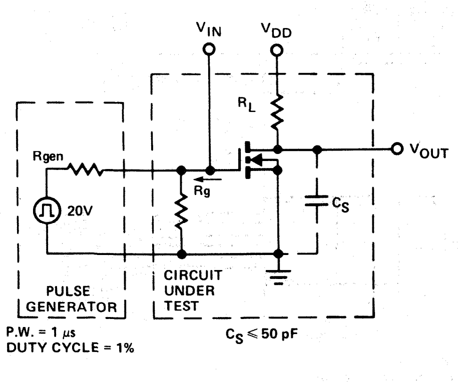
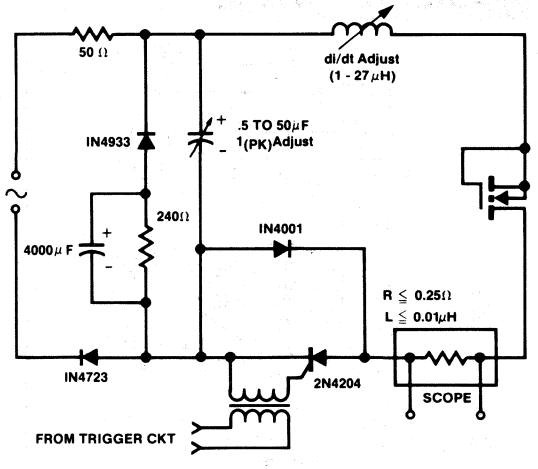


FIGURE 2 Reverse Recovery Test Circuit



2

IRF230 ■ IRF231 ■ IRF232 ■ IRF233 IRF630 ■ IRF631 ■ IRF632 ■ IRF633

IRF230 ■ IRF231 ■ IRF232 ■ IRF233
IRF630 ■ IRF631 ■ IRF632 ■ IRF633

Siliconix

Advance Information

200V N-Channel Enhancement Mode MOSPOWER

These power FETs are designed especially for switching regulators, power converters, solenoid drivers and relay drivers.

FEATURES

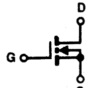
- No Second Breakdown
- High Input Impedance
- Internal Drain-Source Diode
- Very Rugged: Excellent SOA
- Extremely Fast Switching

BENEFITS

- Reduced Component Count
- Improved Performance
- Simpler Designs
- Improved Reliability

Product Summary

Part Number	BV_{DSS}	$R_{DS(ON)}$	I_D	Package
IRF230	200V	0.4Ω	9A	TO-3
IRF231	150V			
IRF232	200V	0.6Ω	8A	
IRF233	150V			
IRF630	200V	0.4Ω	9A	TO-220AB
IRF631	150V			
IRF632	200V	0.6Ω	8A	
IRF633	150V			



ABSOLUTE MAXIMUM RATINGS ($T_C = 25°C$ unless otherwise noted)

Drain-Source Voltage
- IRF230,232,630,632 .... 200V
- IRF231,233,631,633 .... 150V

Drain-Gate Voltage
- IRF230,232,630,632 .... 200V
- IRF231,233,631,633 .... 150V

Drain Current Continuous[1]
- IRF230,231,630,631 .... ± 9A
- IRF232,233,632,633 .... ± 8A

Pulsed[2] .... ± 36A

Gate Current (Peak) .... ± 3A

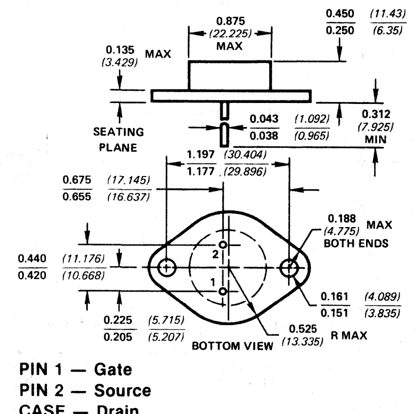
Gate-Source Voltage .... ± 40V

Total Power Dissipation 75W
- Linear Derating Factor .... 0.6W/°C

Storage and Junction
- Temperature .... -55°C to 150°C

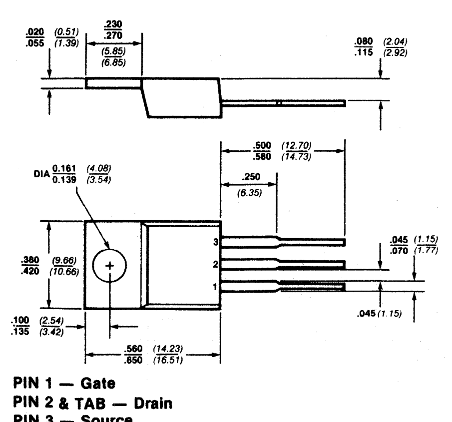
Notes:
1. Limited by package dissipation.
2. Pulse test—80μs to 300μs, 1% duty cycle.

PACKAGE DIMENSIONS



PIN 1 — Gate
PIN 2 — Source
CASE — Drain

TO-3



PIN 1 — Gate
PIN 2 & TAB — Drain
PIN 3 — Source

TO-220AB

ELECTRICAL CHARACTERISTICS ($T_C = 25°C$ unless otherwise noted)

Symbol	Parameter	Part Number	Min	Typ	Max	Unit	Test Conditions
Static							
BV_{DSS}	Drain-Source Breakdown	IRF 230, 232 IRF 630, 632	200			V	$V_{GS} = 0$, $I_D = 250\mu A$
		IRF 231, 233 IRF 631, 633	150				
$V_{GS(th)}$	Gate Threshold Voltage	All	2		4	V	$V_{GS} = V_{DS}$, $I_D = 1 mA$
I_{GSS}	Gate Body Leakage	All			±100	nA	$V_{GS} = \pm 20V$, $V_{DS} = 0$
I_{DSS}	Zero Gate Voltage Drain Current	All		0.1	0.25	mA	V_{DS} = Rated V_{DS}, $V_{GS} = 0$
				0.2	1.0		V_{DS} = Rated V_{DS}, $V_{GS} = 0$, $T_C = 125°C$
$r_{DS(on)}$	Drain-Source On Resistance	IRF 230, 231 IRF 630, 631		0.25	0.4	Ω	$V_{GS} = 10V$, $I_D = 5A$ (Note 1)
		IRF 232, 233 IRF 632, 633		0.4	0.6		
$I_{D(on)}$	On-State Drain Current	All	9			A	$V_{DS} = 25V$, $V_{GS} = 10V$ (Note 1)
Dynamic							
g_{fs}	Forward Transconductance	All	2.5	4.5		S	$V_{DS} = 25V$, $I_D = 5A$ (Note 1)
C_{iss}	Input Capacitance	All		700	800	pF	$V_{GS} = 0$, $V_{DS} = 25V$, $f = 1 MHz$
C_{rss}	Reverse Transfer Capacitance	All		80	150		
C_{oss}	Common-Source Output Capacitance	All		250	450		
$t_{d(on)}$	Turn-On Delay Time	All			30	ns	$V_{DD} = 75V$, $I_D \approx 5A$, $R_L = 15\Omega$, $R_g = 25\Omega$, (Figure 1)
t_r	Rise Time	All			50		
$t_{d(off)}$	Turn-Off Delay Time	All			50		
t_f	Fall Time	All			40		
Drain-Source Diode Characteristics							
V_{SD}	Forward ON Voltage			−1.8		V	$I_S = -9A$, $V_{GS} = 0$ (Note 1)
t_{rr}	Reverse Recovery Time			650		ns	$I_F = -9A$, $V_{GS} = 0$, $di/dt = 100 A/\mu s$ (Figure 2)

Note 1: Pulse Test — 80μs to 300 μs, 1% duty cycle

TEST CIRCUITS

FIGURE 1 Switching Test Circuit

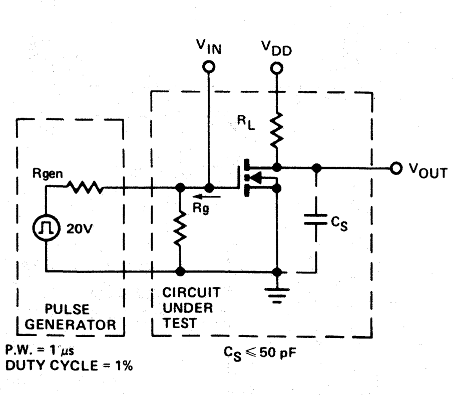
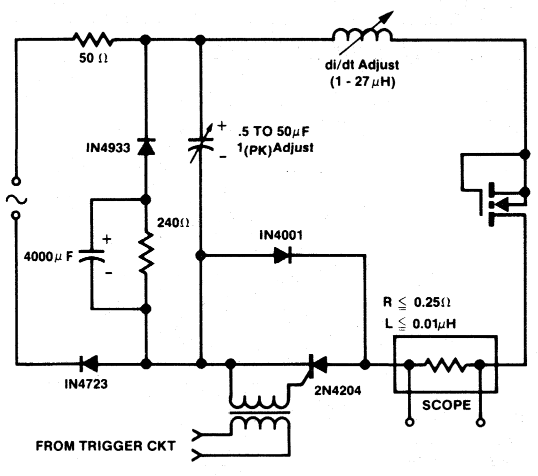


FIGURE 2 Reverse Recovery Test Circuit



IRF240 ■ IRF241 ■ IRF242 ■ IRF243
IRF640 ■ IRF641 ■ IRF642 ■ IRF643

Siliconix

Advanced Information

IRF240 ■ IRF241 ■ IRF242 ■ IRF243 ■ IRF640 ■ IRF641 ■ IRF642 ■ IRF643

IRF240 ■ IRF241 ■ IRF242 ■ IRF243 / IRF640 ■ IRF641 ■ IRF642 ■ IRF643

200V N-Channel Enhancement-Mode MOSPOWER

These power FETs are designed especially for offline switching regulators, converters, solenoid and relay drivers.

FEATURES

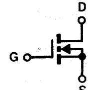
- No Second Breakdown
- High Input Impedance
- Internal Drain-Source Diode
- Very Rugged: Excellent SOA
- Extremely Fast Switching

BENEFITS

- Reduced Component Count
- Improved Performance
- Simpler Designs
- Improved Reliability

Product Summary

Part Number	BV_{DSS}	$r_{DS(ON)}$	I_D	Package
IRF240	200	0.18Ω	18A	TO-3
IRF241	150			
IRF242	200	0.22Ω	16A	
IRF243	150			
IRF640	200	0.18Ω	18A	TO-220AB
IRF641	150			
IRF642	200	0.22Ω	16A	
IRF643	150			



ABSOLUTE MAXIMUM RATINGS (T_C = 25°C unless otherwise noted)

Drain-Source Voltage
- IRF240, 242, 640, 642 .... 200V
- IRF241, 243, 641, 643 .... 150V

Drain-Gate Voltage
- IRF240, 242, 640, 642 .... 200V
- IRF241, 243, 641, 643 .... 150V

Drain Current
- Continuous[1]
  - IRF240, 241, 640, 641 .... ± 18A
  - IRF242, 243, 642, 643 .... ± 16A
- Pulsed[2] .... ±72A

Gate Current (Peak) .... ± 3A

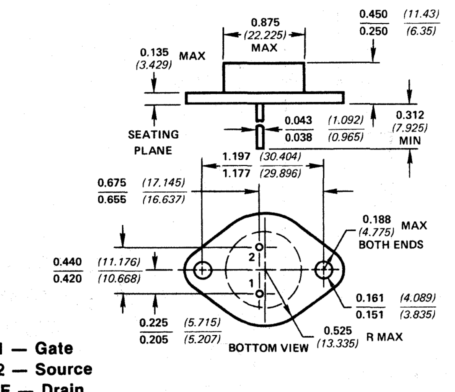
Gate-Source Voltage .... ± 40V

Total Power Dissipation 125W
- Linear Derating Factor .... 1.0W/°C

Operating and Storage
- Temperature .... −55 to +150°C

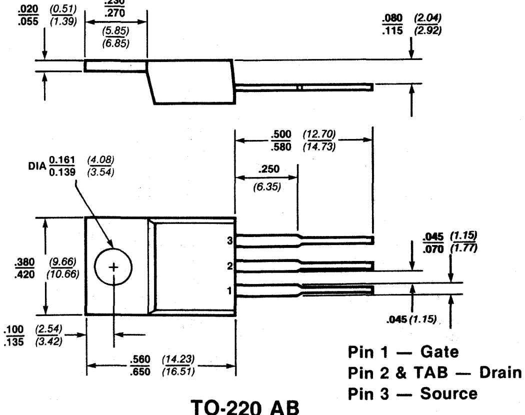
Notes:
1. Limited by package dissipation.
2. Pulse test—80μs to 300μs, 1% duty cycle.

PACKAGE DIMENSIONS



Pin 1 — Gate
Pin 2 — Source
CASE — Drain

TO-3



Pin 1 — Gate
Pin 2 & TAB — Drain
Pin 3 — Source

TO-220 AB

ELECTRICAL CHARACTERISTICS ($T_C = 25°C$ unless otherwise noted)

Symbol	Parameter	Part Number	Min	Max	Unit	Test Conditions
	Static					
BV_{DSS}	Drain-Source Breakdown Voltage	IRF240, 242 IRF640, 642	200		V	$V_{GS} = 0$, $I_D = 250\mu A$
		IRF241, 243 IRF641, 643	150			
$V_{GS(th)}$	Gate Threshold Voltage	All	2.0	4.0	V	$V_{GS} = V_{DS}$, $I_D = 1$ mA
I_{GSS}	Gate-Body Leakage	All		±100	nA	$V_{GS} = \pm 20V$, $V_{DS} = 0$
I_{DSS}	Zero Gate Voltage Drain Current	All		0.25	mA	V_{DS} = Rated V_{DS}, $V_{GS} = 0$
				1.0		V_{DS} = Rated V_{DS}, $V_{GS} = 0$, $T_C = 125°C$
$I_{D(on)}$	On-State Drain Current	All	18		A	$V_{DS} = 25V$, $V_{GS} = 10V$ (Note 1)
$r_{DS(on)}$	Static Drain-Source On-State Resistance	IRF240, 241 IRF640, 641		0.18	Ω	$V_{GS} = 10V$, $I_D = 10A$ (Note 1)
		IRF242, 243 IRF642, 643		0.22		
	Dynamic					
g_{fs}	Forward Transconductance	All	6.0		S	$V_{DS} = 25V$, $I_D = 10A$ (Note 1)
C_{iss}	Input Capacitance	All		1600	pF	$V_{GS} = 0$, $V_{DS} = 25V$, f = 1 MHz
C_{oss}	Output Capacitance			750		
C_{rss}	Reverse Transfer Capacitance			300		
$t_{d(on)}$	Turn-On Delay Time	All		30	ns	$V_{DD} = 75V$, $I_D \approx 10A$, $R_L = 7.5\Omega$, $R_g = 4.7\Omega$ (Fig 1)
t_r	Rise Time	All		60		
$t_{d(off)}$	Turn-Off Delay Time	All		80		
t_f	Fall Time	All		60		
	Drain-Source Diode Characteristics					
			Typ			
V_{SD}	Forward On Voltage	All	−2.0		V	$I_S = -18A$ $V_{GS} = 0$ (Note 1)
t_{rr}	Reverse Recovery Time	All	425		ns	$I_F = -18A$, $V_{GS} = 0$, di/dt = 100A/μs

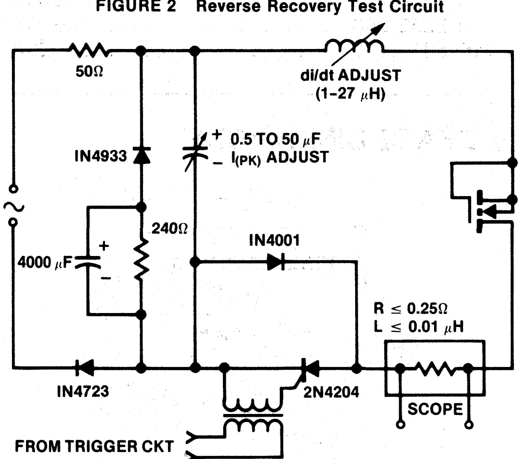
Note:
1. Pulse test: 80 μs to 300 μs, 1% duty cycle.

TEST CIRCUITS

FIGURE 1 Switching Test Circuit

V_{IN} V_{DD} R_L V_{OUT} Rgen 20V Rg C_S PULSE GENERATOR CIRCUIT UNDER TEST
P.W. = 1 μs
DUTY CYCLE = 1%
$C_S \leq 50$ pF

FIGURE 2 Reverse Recovery Test Circuit



IRF250 ■ IRF251 ■ IRF252 ■ IRF253

Siliconix

Advanced Information

200V N-Channel Enhancement-Mode MOSPOWER

These power FETs are designed especially for offline switching regulators, power converters, solenoid and relay drivers.

FEATURES

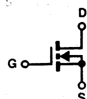
- No Second Breakdown
- High Input Impedance
- Internal Drain-Source Diode
- Very Rugged: Excellent SOA
- Extremely Fast Switching

BENEFITS

- Reduced Component Count
- Improved Performance
- Simpler Designs
- Improved Reliability

Product Summary

Part Number	BV_{DSS}	$r_{DS(ON)}$	I_D	Package
IRF250	200	0.085Ω	30A	TO-3
IRF251	150			
IRF252	200	0.120Ω	25A	
IRF253	150			



ABSOLUTE MAXIMUM RATINGS (T_C=25°C unless otherwise noted)

Drain-Source Voltage
- IRF250, 252 . . . . . 200V
- IRF251, 253 . . . . . 150V

Drain-Gate Voltage
- IRF250, 252 . . . . . 200V
- IRF251, 253 . . . . . 150V

Drain Current
- Continuous[1]
  - IRF250, 251 . . . . . ±30A
  - IRF252, 253 . . . . . ±25A
- Pulsed[2] . . . . . ±120A

Gate Current (Peak) . . . . . ±3A

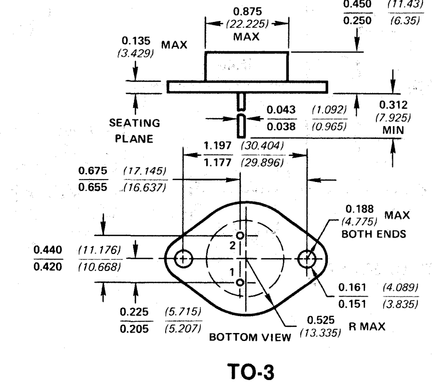
Gate-Source Voltage . . . . . ±40V

Total Power Dissipation 150W
- Linear Derating Factor . . . . . 1.2W/°C

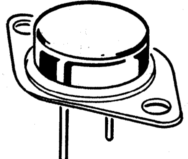
Operating and Storage
- Temperature . . . . . −55 to +150°C

Notes:
1. Limited by package dissipation.
2. Pulse test—80μs to 300μs, 1% duty cycle.

PACKAGE DIMENSIONS



TO-3



Pin 1 — Gate
Pin 2 — Source
CASE — Drain

ELECTRICAL CHARACTERISTICS ($T_C = 25°C$ unless otherwise noted)

Symbol	Parameter	Part Number	Min	Max	Unit	Test Conditions
			Static			
BV_{DSS}	Drain-Source Breakdown Voltage	IRF250, 252	200		V	$V_{GS} = 0$, $I_D = 250 \mu A$
		IRF251, 253	150			
$V_{GS(th)}$	Gate Threshold Voltage	All	2.0	4.0	V	$V_{GS} = V_{DS}$, $I_D = 1$ mA
I_{GSS}	Gate-Body Leakage	All		±100	nA	$V_{GS} = \pm 20V$, $V_{DS} = 0$
I_{DSS}	Zero Gate Voltage Drain Current	All		0.25	mA	V_{DS} = Rated V_{DS}, $V_{GS} = 0$
				1.0		V_{DS} = Rated V_{DS}, $V_{GS} = 0$, $T_C = 125°C$
$I_{D(on)}$	On-State Drain Current	All	30		A	$V_{DS} = 25V$, $V_{GS} = 10V$ (Note 1)
$r_{DS(on)}$	Static Drain-Source On-State Resistance	IRF250, 251		0.085	Ω	$V_{GS} = 10V$, $I_D = 16A$ (Note 1)
		IRF252, 253		0.120		
			Dynamic			
g_{fs}	Forward Transconductance	All	8		S	$V_{DS} = 12V$, $I_D = 16A$ (Note 1)
C_{iss}	Input Capacitance	All		3000	pF	$V_{GS} = 0$, $V_{DS} = 25V$, f = 1 MHz
C_{oss}	Output Capacitance			1200		
C_{rss}	Reverse Transfer Capacitance			500		
$t_{d(on)}$	Turn-On Delay Time	All		35	ns	$V_{DD} = 75V$, $I_D \approx 16A$, $R_L = 7.5\Omega$, $R_g = 4.7\Omega$, (Figure 1)
t_r	Rise Time	All		100		
$t_{d(off)}$	Turn-Off Delay Time	All		125		
t_f	Fall Time	All		100		
			Drain-Source Diode Characteristics			
			Typ			
V_{SD}	Forward On Voltage	All	−1.6		V	$I_S = -30A$ (Note 1)
t_{rr}	Reverse Recovery Time	All	500		ns	$I_F = -30A$, $V_{GS} = 0$, di/dt = 100A/µs (Fig. 2)

Note:
1. Pulse test: 80 µs to 300 µs, 1% duty cycle.

TEST CIRCUITS

FIGURE 1 Switching Test Circuit

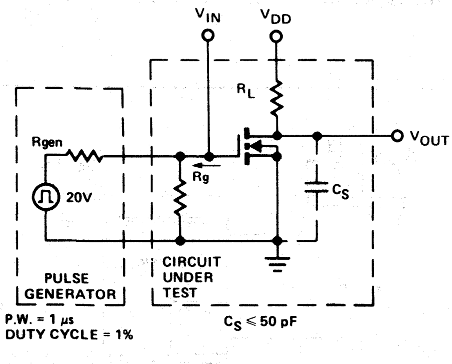


FIGURE 2 Reverse Recovery Test Circuit

50Ω
di/dt ADJUST (1-27 µH)
IN4933
0.5 TO 50 µF $I_{(PK)}$ ADJUST
240Ω
4000 µF
IN4001
R ≤ 0.25Ω
L ≤ 0.01 µH
IN4723
2N4204
SCOPE
FROM TRIGGER CKT

IRF320 ■ IRF321 ■ IRF322 ■ IRF323
IRF720 ■ IRF721 ■ IRF722 ■ IRF723

Siliconix

Advanced Information

400V N-Channel Enhancement Mode MOSPOWER

These power FETs are designed especially for off-line switching regulators, converters, solenoid and relay drivers.

FEATURES

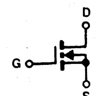
- High Voltage
- No Second Breakdown
- High Input Impedance
- Internal Drain-Source Diode
- Very Rugged: Excellent SOA
- Extremely Fast Switching

BENEFITS

- Reduced Component Count
- Improved Performance
- Simpler Designs
- Improved Reliability

Product Summary

Part Number	BV_{DSS}	$R_{DS(ON)}$	I_D	Package
IRF320	400V	1.8Ω	3A	TO-3
IRF321	350V			
IRF322	400V	2.5Ω	2.5A	
IRF323	350V			
IRF720	400V	1.8Ω	3A	TO-220AB
IRF721	350V			
IRF722	400V	2.5Ω	2.5A	
IRF723	350V			



ABSOLUTE MAXIMUM RATINGS ($T_C = 25°C$ unless otherwise noted)

Drain-Source Voltage
- IRF320, 322, 720, 722 .... 400V
- IRF321, 323, 721, 723 .... 350V

Drain-Gate Voltage
- IRF320, 322, 720, 722 .... 400V
- IRF321, 323, 721, 723 .... 350V

Drain Current Continuous
- IRF320, 321, 720, 721 .... ±3A
- IRF322, 323, 722, 723 .... ±2.5A

Drain Current
- Pulsed (80μs to 300μs, 1% duty cycle) .... ±12A

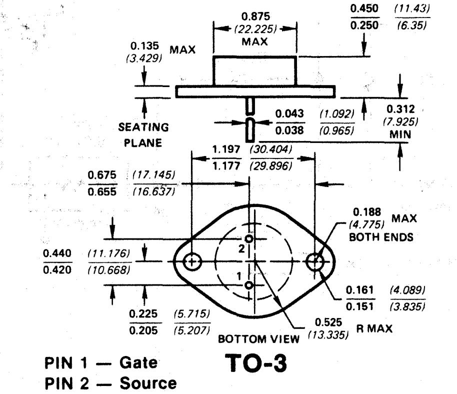
Gate Current (Peak) .... ±1A

Gate-Source Voltage .... ±40V

Total Power Dissipation .... 40 W
- Linear Derating Factor .... 0.32 W/°C

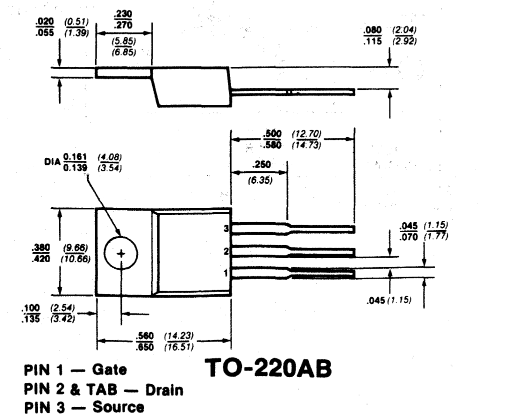
Operating and Storage Temperature .... -55°C to +150°C

PACKAGE DIMENSIONS



PIN 1 — Gate
PIN 2 — Source
CASE — Drain

TO-3



PIN 1 — Gate
PIN 2 & TAB — Drain
PIN 3 — Source

TO-220AB

ELECTRICAL CHARACTERISTICS ($T_C = 25°C$ unless otherwise noted)

Parameter		Part Number	Min	Typ	Max	Unit	Test Conditions
Static							
BV_{DSS}	Drain-Source Breakdown Voltage	IRF320, 322 IRF720, 722	400			V	$V_{GS} = 0$, $I_D = 250\mu A$
		IRF321, 323 IRF721, 723	350				
$V_{GS(th)}$	Gate Threshold Voltage	All	2.0		4.0	V	$V_{DS} = V_{GS}$, $I_D = 1.0$ mA
I_{GSS}	Gate-Body Leakage	All			±100	nA	$V_{GS} = \pm 20V$, $V_{DS} = 0$
I_{DSS}	Zero Gate Voltage Drain Current	All		0.1	0.25	mA	V_{DS} = Rated V_{DS}, $V_{GS} = 0$
				0.2	1.0		V_{DS} = Rated V_{DS}, $V_{GS} = 0$, $T_C = 125°C$
$I_{D(on)}$	On-State Drain Current	All	3.0			A	$V_{DS} = 25V$, $V_{GS} = 10V$ (Note 1)
$r_{DS(on)}$	Static Drain-Source On-State Resistance	IRF320, 321 IRF720, 721		1.5	1.8	Ω	$V_{GS} = 10V$, $I_D = 1.5A$ (Note 1)
		IRF322, 323 IRF722, 723		1.8	2.5		
Dynamic							
g_{fs}	Forward Transconductance	All	1.0	2.0		S	$V_{DS} = 25V$, $I_D = 1.5A$ (Note 1)
C_{iss}	Input Capacitance	All		450	600	pF	$V_{GS} = 0$, $V_{DS} = 25V$, f = 1 MHz
C_{oss}	Output Capacitance			100	200		
C_{rss}	Reverse Transfer Capacitance			20	40		
$t_{d(on)}$	Turn-On Delay Time	All		20	40	ns	$V_{DD} = 200V$, $I_D \approx 1.5A$, $R_L = 130\Omega$, $R_g = 25\Omega$, (Fig. 1)
t_r	Rise Time	All		25	50		
$t_{d(off)}$	Turn-Off Delay Time	All		50	100		
t_f	Fall Time	All		25	50		
Drain-Source Diode Characteristics							
V_{SD}	Forward On Voltage	All		−1.3		V	$I_S = -3A$ $V_{GS} = 0$ (Note 1)
t_{rr}	Reverse Recovery Time	All		400		ns	$I_F = -3A$, $V_{GS} = 0$, di/dt = 100A/μs (Fig. 1)

Note 1: Pulse test — 80 μs to 300 μs, 1% duty cycle

TEST CIRCUITS

FIGURE 1 Switching Test Circuit

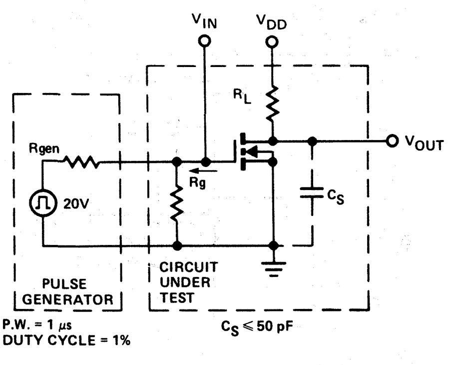
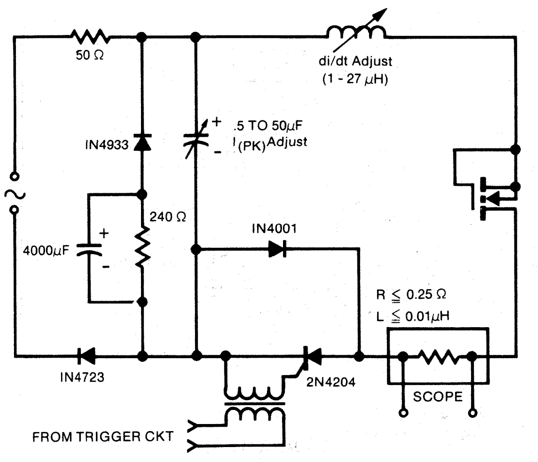


FIGURE 2 JEDEC Reverse Recovery Circuit



IRF330 ■ IRF331 ■ IRF332 ■ IRF333
IRF730 ■ IRF731 ■ IRF732 ■ IRF733

Siliconix

N-Channel MOSPOWER FETs 400V Enhancement-Mode

These power FETs are designed especially for off-line switching regulators, converters, solenoid and relay drivers.

FEATURES

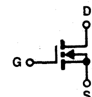
- High Voltage
- No Second Breakdown
- High Input Impedance
- Internal Drain-Source Diode
- Very Rugged: Excellent SOA
- Extremely Fast Switching

BENEFITS

- Reduced Component Count
- Improved Performance
- Simpler Designs
- Improved Reliability

Product Summary

Part Number	BV_{DSS}	$R_{DS(ON)}$	I_D	Package
IRF330	400V	1.0Ω	5.5A	TO-3
IRF331	350V			
IRF332	400V	1.5Ω	4.5A	
IRF333	350V			
IRF730	400V	1.0Ω	5.5A	TO-220AB
IRF731	350V			
IRF732	400V	1.5Ω	4.5A	
IRF733	350V			

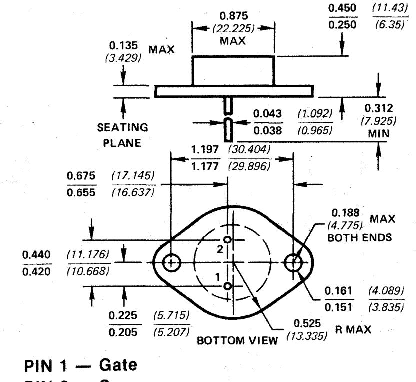


ABSOLUTE MAXIMUM RATINGS ($T_C = 25°C$ unless otherwise noted)

Drain-Source Voltage
IRF330, 332, 730, 732 .... 400V
IRF331, 333, 731, 733 .... 350V
Drain-Gate Voltage
IRF330, 332, 730, 732 .... 400V
IRF331, 333, 731, 733 .... 350V
Continuous Drain Current, $T_C = 25°C$
IRF330, 331, 730, 731 .... ±5.5A
IRF332, 333, 732, 733 .... ±4.5A

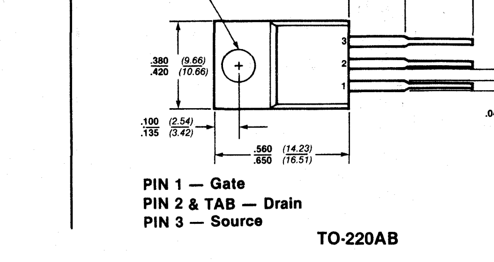
Pulsed Drain Current (80μs to 300μs, 1% duty cycle) .... ±22A
Gate Current (Peak) .... ±3A
Gate-Source Voltage .... ±40V
Maximum Power Dissipation 75W
Linear Derating Factor .... 0.6 W/°C
Operating and Storage Temperature .... −55 to 150°C

PACKAGE DIMENSIONS



PIN 1 — Gate
PIN 2 — Source
CASE — Drain

TO-204AA (TO-3)



PIN 1 — Gate
PIN 2 & TAB — Drain
PIN 3 — Source

TO-220AB

Electrical Characteristics (T_C=25°C unless otherwise specified)

Symbol	Parameter	Part Number	Min	Typ	Max	Unit	Test Conditions
Static							
BV_{DSS}	Drain-Source Breakdown	IRF 330, 730 IRF 332, 732	400			V	$V_{GS}=0$, $I_D=250\mu A$
		IRF 331, 731 IRF 333, 733	350				
$V_{GS(th)}$	Gate Threshold Voltage	All	2	3.3	4	V	$V_{GS}=V_{DS}$, $I_D=1mA$
I_{GSS}	Gate Body Leakage	All		10	±100	nA	$V_{GS}=\pm 20V$, $V_{DS}=0$
I_{DSS}	Zero Gate Voltage Drain Current	All		0.1	0.25	mA	V_{DS} = Rated V_{DS}, $V_{GS}=0$
				0.5	1.0		V_{DS} = Rated V_{DS}, $V_{GS}=0$, $T_C=125°C$
$r_{DS(on)}$	Drain-Source On Resistance	IRF 330, 730 IRF 331, 731		0.9	1	Ω	$V_{GS}=10V$, $I_D=3A$ (Note 1)
		IRF 332, 732 IRF 333, 733		1.2	1.5		
$I_{D(on)}$	On-State Drain Current	IRF 330, 730 IRF 331, 731	5.5	8		A	$V_{DS}=25V$, $V_{GS}=10V$ (Note 1)
		IRF 332, 732 IRF 333, 733	4.5	8			
Dynamic							
g_{fs}	Forward Transconductance	All	3	3.5		S	$V_{DS}=100V$, $I_D=3A$ (Note 1)
C_{iss}	Input Capacitance	All		800	900	pF	$V_{GS}=0$, $V_{DS}=25V$, f = 1 MHz
C_{rss}	Reverse Transfer Capacitance	All		25	80		
C_{oss}	Common-Source Output Capacitance	All		150	300		
$t_{d(on)}$	Turn-On Delay Time	All			30	ns	$V_{DD}=200V$, $I_D \approx 3A$, $R_L=67\Omega$, $R_g=10\Omega$, (Figure 1)
t_r	Rise Time	All			35		
$t_{d(off)}$	Turn-Off Delay Time	All			55		
t_f	Fall Time	All			35		
Drain-Source Diode Characteristics							
				Typ.			
V_{SD}	Forward ON Voltage	All		−1.4		V	$I_S=-5.5A$ (Note 1)
t_{rr}	Reverse Recovery Time	All		400		ns	$I_F=I_R=-5.5A$, $V_{GS}=0$, (Figure 2)

Note 1: Pulse Test—80μs to 300 μs, 1% duty cycle

Refer to VNDA40 Design Curves (See Section 4)

TEST CIRCUITS

FIGURE 1 Switching Test Circuit

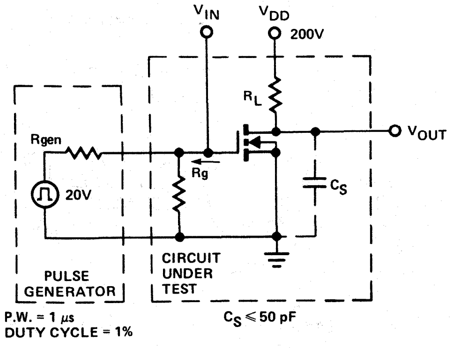
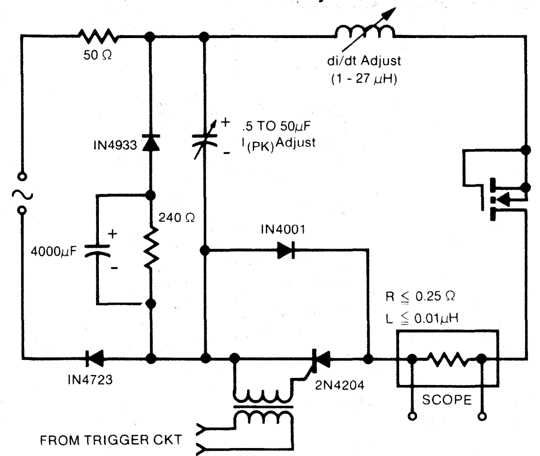


FIGURE 2 Reverse Recovery Test Circuit



IRF340 ■ IRF341 ■ IRF342 ■ IRF343
IRF740 ■ IRF741 ■ IRF742 ■ IRF743

Siliconix

400V N-Channel Enhancement-Mode MOSPOWER

Advance Information

These power FETs are designed especially for offline switching regulators, converters, solenoid and relay drivers.

FEATURES

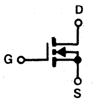
- High Voltage
- No Second Breakdown
- High Input Impedance
- Internal Drain-Source Diode
- Very Rugged: Excellent SOA
- Extremely Fast Switching

BENEFITS

- Reduced Component Count
- Improved Performance
- Simpler Designs
- Improved Reliability

Product Summary

Part Number	BV_{DSS}	$r_{DS(ON)}$	I_D	Package
IRF340	400V	0.55Ω	10A	TO-3
IRF341	350V			
IRF342	400V	0.80Ω	8.0A	
IRF343	350V			
IRF740	400V	0.55Ω	10A	TO-220AB
IRF741	350V			
IRF742	400V	0.80Ω	8.0A	
IRF743	350V			



ABSOLUTE MAXIMUM RATINGS (T_C=25°C unless otherwise noted)

Drain-Source Voltage
- IRF340, 342, 740, 742 .... 400V
- IRF341, 343, 741, 743 .... 350V

Drain-Gate Voltage
- IRF340, 342, 740, 742 .... 400V
- IRF341, 343, 741, 743 .... 350V

Drain Current
- Continuous
  - IRF340, 341, 740, 741 .... ± 10A
  - IRF342, 343, 742, 743 .... ± 8A
- Pulsed[2] .... ± 40A

Gate Current (Peak) .... ± 3A

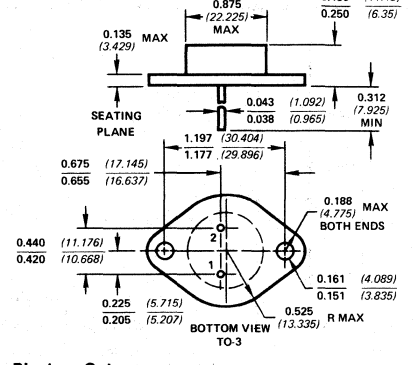
Gate-Source Voltage .... ± 40V

Total Power Dissipation 125W
- Linear Derating Factor .... 1.0W/°C

Operating and
- Storage Temperature .... − 55°C to + 150°C

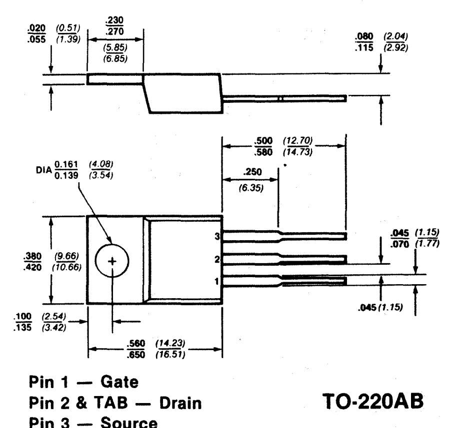
Notes:
1. Limited by package dissipation.
2. Pulse test—80μs to 300μs, 1% duty cycle.

PACKAGE DIMENSIONS



Pin 1 — Gate
Pin 2 — Source
CASE — Drain

TO-3



Pin 1 — Gate
Pin 2 & TAB — Drain
Pin 3 — Source

TO-220AB

ELECTRICAL CHARACTERISTICS ($T_C = 25°C$ unless otherwise noted)

	Parameter	Part Number	Min	Typ	Max	Unit	Test Conditions
		Static					
BV_{DSS}	Drain-Source Breakdown Voltage	IRF340, 740 IRF342, 742	400			V	$V_{GS} = 0$, $I_D = 250\mu A$
		IRF341, 741 IRF343, 743	350				
$V_{GS(th)}$	Gate Threshold Voltage	All	2.0	3.3	4.0	V	$V_{DS} = V_{GS}$, $I_D = 1$ mA
I_{GSS}	Gate-Body Leakage	All		10	±100	nA	$V_{GS} = \pm 20V$, $V_{DS} = 0$
I_{DSS}	Zero Gate Voltage Drain Current	All		0.1	0.25	mA	V_{DS} = Rated V_{DS}, $V_{GS} = 0V$
				0.2	1.0		V_{DS} = Rated V_{DS}, $V_{GS} = 0V$, $T_C = 125°C$
$I_{D(on)}$	On-State Drain Current	IRF340, 341 IRF740, 741	10			A	$V_{DS} = 25V$, $V_{GS} = 10V$ (Note 1)
		IRF342, 343 IRF742, 743	8.0				
$r_{DS(on)}$	Static Drain-Source On-State Resistance	IRF340, 341 IRF740, 741		0.47	0.55	Ω	$V_{GS} = 10V$, $I_D = 5A$ (Note 1)
		IRF342, 343 IRF742, 743		0.68	0.80		
		Dynamic					
g_{fs}	Forward Transconductance	All	4.0	7.0		S	$V_{DS} = 25V$, $I_D = 5A$ (Note 1)
C_{iss}	Input Capacitance	All		1250	1600	pF	$V_{GS} = 0$, $V_{DS} = 25V$, f = 1 MHz
C_{oss}	Output Capacitance			300	450		
C_{rss}	Reverse Transfer Capacitance			80	150		
$t_{d(on)}$	Turn-On Delay Time	All		17	35	ns	$V_{DD} = 175V$, $I_D \approx 5A$, $R_L = 35\Omega$, $R_g = 10\Omega$
t_r	Rise Time	All		5.0	15		
$t_{d(off)}$	Turn-Off Delay Time	All		45	90		
t_f	Fall Time	All		16	35		
		Drain-Source Diode Characteristics					
V_{SD}	Forward On Voltage	All		−2.0		V	$I_S = -10A$ $V_{GS} = 0$ (Note 1)
t_{rr}	Reverse Recovery Time	All		600		ns	$I_F = -10A$, $V_{GS} = 0$, di/dt = 100A/μs

Note 1: Pulse test 80 μs to 300 μs, 1% duty cycle

TEST CIRCUITS

FIGURE 1 Switching Test Circuit

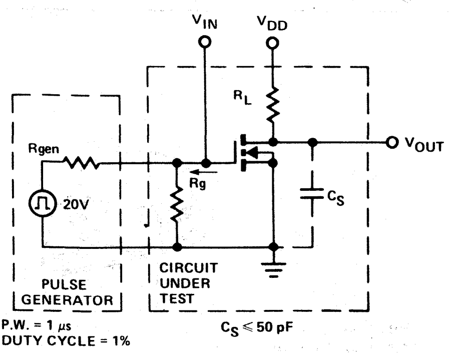
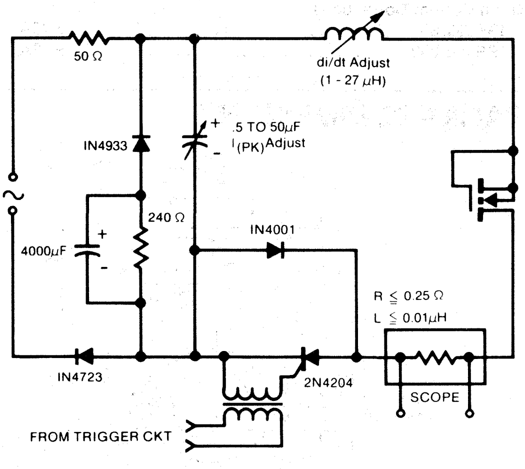


FIGURE 2 Reverse Recovery Test Circuit



IRF350 ▪ IRF351 ▪ IRF352 ▪ IRF353

IRF350 ▪ IRF351 ▪ IRF352 ▪ IRF353

Advanced Information

400V N-Channel Enhancement Mode MOSPOWER

These power FETs are designed especially for off-line switching regulators, converters, solenoid and relay drivers.

FEATURES

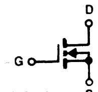
- High Voltage
- No Second Breakdown
- High Input Impedance
- Internal Drain-Source Diode
- Very Rugged: Excellent SOA
- Extremely Fast Switching

BENEFITS

- Reduced Component Count
- Improved Performance
- Simpler Designs
- Improved Reliability

Product Summary

Part Number	BV_{DSS}	$R_{DS(ON)}$	I_D	Package
IRF350	400V	0.3Ω	15A	TO-3
IRF351	350V			
IRF352	400V	0.4Ω	13A	
IRF353	350V			



ABSOLUTE MAXIMUM RATINGS (T_C = 25°C unless otherwise noted)

Drain-Source Voltage
- IRF350 .... 400V
- IRF351 .... 350V
- IRF352 .... 400V
- IRF353 .... 350V

Drain-Gate Voltage
- IRF350 .... 400V
- IRF351 .... 350V
- IRF352 .... 400V
- IRF353 .... 350V

Drain Current Continuous
- IRF350, 351 .... ±15A
- IRF352, 353 .... ±13A

Drain Current
Pulsed (80μs to 300μs, 1% duty cycle) .... ±60A

Gate Current (Peak) .... ±3A

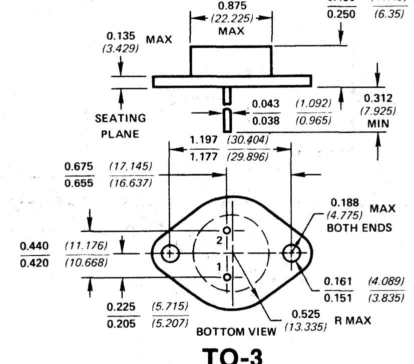
Gate-Source Voltage .... ±40V

Total Power Dissipation .... 150 W

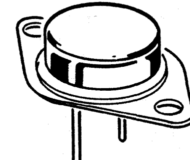
Linear Derating Factor .... 1.2 W/°C

Operating and Storage
Temperature .... -55°C to +150°C

PACKAGE DIMENSIONS



TO-3



PIN 1 — Gate
PIN 2 — Source
CASE — Drain

ELECTRICAL CHARACTERISTICS ($T_C = 25°C$ unless otherwise noted)

Parameter		Part Number	Min	Typ	Max	Unit	Test Conditions
Static							
BV_{DSS}	Drain-Source Breakdown Voltage	IRF350 IRF352	400			V	$V_{GS} = 0$, $I_D = 250\mu A$
		IRF351 IRF353	350				
$V_{GS(th)}$	Gate Threshold Voltage	All	2.0	3.2	4.0	V	$V_{DS} = V_{GS}$, $I_D = 1$ mA
I_{GSS}	Gate-Body Leakage	All		50	±100	nA	$V_{GS} = \pm 20V$, $V_{DS} = 0$
I_{DSS}	Zero Gate Voltage Drain Current	All		0.1	0.25	mA	V_{DS} = Rated V_{DS}, $V_{GS} = 0$
				0.2	1.0		V_{DS} = Rated V_{DS}, $V_{GS} = 0$, $T_C = 125°C$
$I_{D(on)}$	On-State Drain Current	All	15			A	$V_{DS} = 25V$, $V_{GS} = 10V$ (Note 1)
$r_{DS(on)}$	Static Drain-Source On-State Resistance	IRF350 IRF351		0.25	0.3	Ω	$V_{GS} = 10V$, $I_D = 8A$ (Note 1)
		IRF352 IRF353		0.3	0.4		
Dynamic							
g_{fs}	Forward Transconductance	All	8	9.0		S	$V_{DS} = 100V$, $I_D = 8A$ (Note 1)
C_{iss}	Input Capacitance	All		2500	3000	pF	$V_{GS} = 0$, $V_{DS} = 25V$, f = 1 MHz
C_{oss}	Output Capacitance			400	600		
C_{rss}	Reverse Transfer Capacitance			100	200		
$t_{d(on)}$	Turn-On Delay Time	All		25	35	ns	$V_{DD} = 200V$, $I_D \simeq 8A$, $R_L = 25\Omega$, $R_g = 5\Omega$ (Fig. 1)
t_r	Rise Time	All		50	65		
$t_{d(off)}$	Turn-Off Delay Time	All		75	150		
t_f	Fall Time	All		50	75		
Drain-Source Diode Characteristics							
V_{SD}	Forward On Voltage	All		−1.5		V	$I_S = -15A$ $V_{GS} = 0$ (Note 1)
t_{rr}	Reverse Recovery Time	All		400		ns	$I_F = -15A$, $V_{GS} = 0$, di/dt = 100A/μs (Fig. 2)

Note 1: Pulse test — 80 μs to 300 μs, 1% duty cycle

TEST CIRCUITS

FIGURE 1 Switching Test Circuit

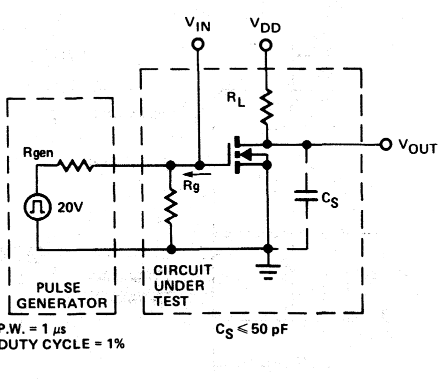
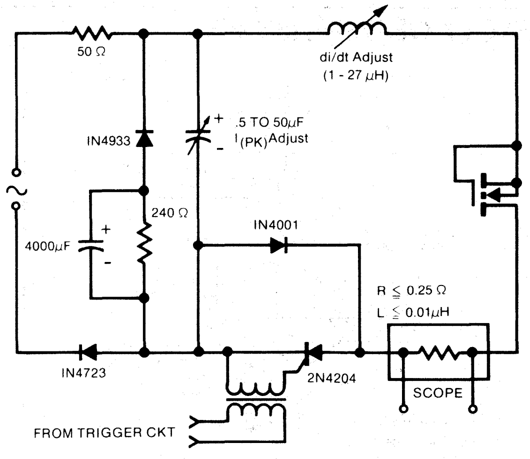


FIGURE 2 JEDEC Reverse Recovery Circuit



IRF420 ■ IRF421 ■ IRF422 ■ IRF423
IRF820 ■ IRF821 ■ IRF822 ■ IRF823

Siliconix

Advanced Information

500V N-Channel Enhancement Mode MOSPOWER

These power FETs are designed especially for off-line switching regulators, converters, solenoid and relay drivers.

FEATURES

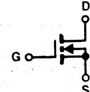
- High Voltage
- No Second Breakdown
- High Input Impedance
- Internal Drain-Source Diode
- Very Rugged: Excellent SOA
- Extremely Fast Switching

BENEFITS

- Reduced Component Count
- Improved Performance
- Simpler Designs
- Improved Reliability

Product Summary

Part Number	BV_{DSS}	$R_{DS(ON)}$	I_D	Package
IRF420	500V	3Ω	2.5A	TO-3
IRF421	450V			
IRF422	500V	4Ω	2.0A	
IRF423	450V			
IRF820	500V	3Ω	2.5A	TO-220AB
IRF821	450V			
IRF822	500V	4Ω	2.0A	
IRF823	450V			



ABSOLUTE MAXIMUM RATINGS (T_C = 25°C unless otherwise noted)

Drain-Source Voltage
- IRF420, 422 / IRF820, 822 .... 500V
- IRF421, 423 / IRF821, 823 .... 450V

Drain-Gate Voltage
- IRF420, 422 / IRF820, 822 .... 500V
- IRF421, 423 / IRF821, 823 .... 450V

Drain Current Continuous
- IRF420, 421 .... ±2.5A
- IRF422, 423 .... ±2.0A

Drain Current
- Pulsed (80μs to 300μs, 1% duty cycle) .... ± 10A

Gate Current (Peak) .... ± 1A

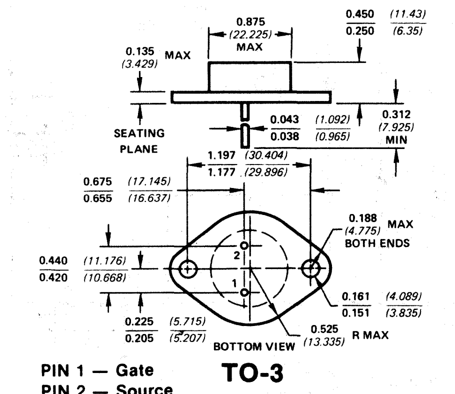
Gate-Source Voltage .... ± 40V

Total Power Dissipation .... 40 W

Linear Derating Factor .... 0.32 W/°C

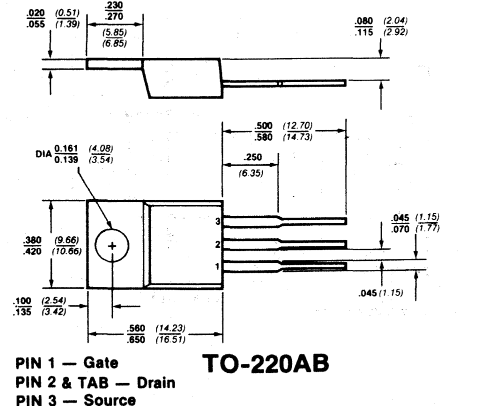
Operating and Storage Temperature .... -55°C to + 150°C

PACKAGE DIMENSIONS



TO-3

PIN 1 — Gate
PIN 2 — Source
CASE — Drain



TO-220AB

PIN 1 — Gate
PIN 2 & TAB — Drain
PIN 3 — Source

ELECTRICAL CHARACTERISTICS ($T_C = 25°C$ unless otherwise noted)

Symbol	Parameter	Part Number	Min	Typ	Max	Unit	Test Conditions
	Static						
BV_{DSS}	Drain-Source Breakdown Voltage	IRF420, 820 IRF422, 822	500			V	$V_{GS} = 0$, $I_D = 250\mu A$
		IRF421, 821 IRF423, 823	450				
$V_{GS(th)}$	Gate Threshold Voltage	All	2.0	3.3	4.0	V	$V_{DS} = V_{GS}$, $I_D = 1$ mA
I_{GSS}	Gate-Body Leakage	All		10	±100	nA	$V_{GS} = \pm 20V$, $V_{DS} = 0$
I_{DSS}	Zero Gate Voltage Drain Current	All		0.1	0.25	mA	$V_{DS} = 0.8$ Rated V_{DS}, $V_{GS} = 0$
				0.2	1.0		$V_{DS} =$ Rated V_{DS}, $V_{GS} = 0$, $T_C = 125°C$
$I_{D(on)}$	On-State Drain Current	All	2.5			A	$V_{DS} = 25V$, $V_{GS} = 10V$ (Note 1)
$r_{DS(on)}$	Static Drain-Source On-State Resistance	IRF420, 820 IRF421, 821		2.5	3.0	Ω	$V_{GS} = 10V$, $I_D = 1A$ (Note 1)
		IRF422, 822 IRF423, 823		3.0	4.0		
	Dynamic						
g_{fs}	Forward Transconductance	All	1.0	1.75		S	$V_{DS} = 25V$, $I_D = 1A$ (Note 1)
C_{iss}	Input Capacitance	All		300	400	pF	$V_{GS} = 0$, $V_{DS} = 25V$, f = 1 MHz
C_{oss}	Output Capacitance			75	150		
C_{rss}	Reverse Transfer Capacitance			20	40		
$t_{d(on)}$	Turn-On Delay Time	All		30	60	ns	$V_{DD} = 250V$, $I_D \approx 1A$, $R_L = 240\Omega$, $R_g = 50\Omega$, $V_{GS} = 10V$ (Fig. 1)
t_r	Rise Time	All		25	50		
$t_{d(off)}$	Turn-Off Delay Time	All		30	60		
t_f	Fall Time	All		15	30		
	Drain-Source Diode Characteristics						
V_{SD}	Forward On Voltage	All		−1.0		V	$I_S = -2.5A$ $V_{GS} = 0$ (Note 1)
t_{rr}	Reverse Recovery Time	All		200		ns	$I_F = -2.5A$, $V_{GS} = 0$, $di/dt = 100A/\mu s$ (Fig. 2)

Note 1: Pulse test — 80 μs to 300 μs, 1% duty cycle

TEST CIRCUITS

FIGURE 1 Switching Test Circuit

P.W. = 1 μs
DUTY CYCLE = 1%

$C_S \leq 50$ pF

FIGURE 2 JEDEC Reverse Recovery Circuit

R ≦ 0.25 Ω
L ≦ 0.01μH

IRF430 ■ IRF431 ■ IRF432 ■ IRF433
IRF830 ■ IRF831 ■ IRF832 ■ IRF833

Siliconix

500V N-Channel Enhancement Mode MOSPOWER

These power FETs are designed especially for offline switching regulators, converters, solenoid and relay drivers.

FEATURES

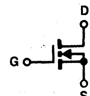
- High Voltage
- No Second Breakdown
- High Input Impedance
- Internal Drain-Source Diode
- Very Rugged: Excellent SOA
- Extremely Fast Switching

BENEFITS

- Reduced Component Count
- Improved Performance
- Simpler Designs
- Improved Reliability

Product Summary

Part Number	BV_{DSS}	$r_{DS(ON)}$	I_D	Package
IRF430	500V	1.5Ω	4.5A	TO-3
IRF431	450V			
IRF432	500V	2.0Ω	4A	
IRF433	450V			
IRF830	500V	1.5Ω	4.5A	TO-220AB
IRF831	450V			
IRF832	500V	2.0Ω	4A	
IRF833	450V			



ABSOLUTE MAXIMUM RATINGS ($T_C = 25°C$ unless otherwise noted)

Drain-Source Voltage
- IRF430, 432, 830, 832 .... 500V
- IRF431, 433, 831, 833 .... 450V

Drain-Gate Voltage
- IRF430, 432, 830, 832 .... 500V
- IRF431, 433, 831, 833 .... 450V

Continuous Drain Current, $T_C = 25°C$[1]
- IRF430, 431, 830, 831 .... ± 4.5A
- IRF432, 433, 832, 833 .... ± 4A

Pulsed Drain Current[2] .... ± 18A

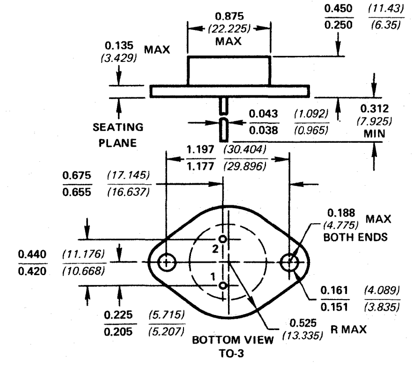
Gate-Source Voltage .... ± 40V

Maximum Power Dissipation 75W
- Linear Derating Factor .... 0.6 W/°C

Operating and Storage Temperature .... – 55 to 150°C

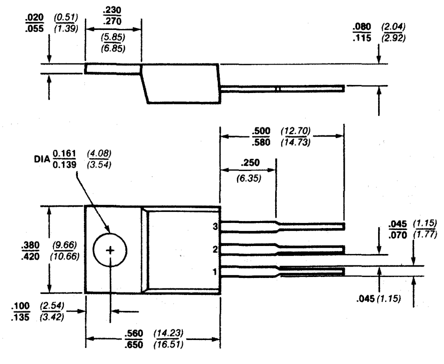
Notes:
1. Limited by package dissipation.
2. Pulse test — 80μs to 300μs, 1% duty cycle.

PACKAGE DIMENSIONS



PIN 1 — Gate
PIN 2 — Source
CASE — Drain

TO-204AA (TO-3)



PIN 1 — Gate
PIN 2 & TAB — Drain
PIN 3 — Source

TO-220AB

ELECTRICAL CHARACTERISTICS ($T_C = 25°C$ unless otherwise noted)

Symbol	Parameter	Part Number	Min	Max	Unit	Test Conditions
Static						
BV_{DSS}	Drain-Source Breakdown	IRF430, 2 IRF830, 2	500		V	$V_{GS} = 0$, $I_D = 250\mu A$
		IRF431, 3 IRF831, 3	450		V	$V_{GS} = 0$, $I_D = 250\mu A$
$V_{GS(th)}$	Gate Threshold Voltage	All	2	4	V	$V_{DS} = V_{GS}$, $I_D = 1$ mA
I_{GSS}	Gate-Body Leakage	All		±100	nA	$V_{GS} = \pm 20V$, $V_{DS} = 0$
I_{DSS}	Zero Gate Voltage Drain Current	All		0.25	mA	V_{DS} = Rated V_{DS}, $V_{GS} = 0$
				1.0	mA	V_{DS} = Rated V_{DS}, $V_{GS} = 0$, $T_C = 125°C$
$I_{D(on)}$	On-State Drain Current	IRF430, 1 IRF830, 1	4.5		A	$V_{DS} = 25V$, $V_{GS} = 10V$ (Note 1)
		IRF431, 3 IRF831, 3	4.0		A	$V_{DS} = 25V$, $V_{GS} = 10V$ (Note 1)
$r_{DS(on)}$	Static Drain-Source On-State Resistance	IRF430, 1 IRF830, 1		1.5	Ω	$V_{GS} = 10V$, $I_D = 2.5A$ (Note 1)
		IRF432, 3 IRF832, 3		2.0	Ω	$V_{GS} = 10V$, $I_D = 2.5A$ (Note 1)
Dynamic						
g_{fs}	Forward Transconductance	All	2.5		S	$V_{DS} = 100V$, $I_D = 2.5A$ (Note 1)
C_{iss}	Input Capacitance	All		800	pF	$V_{GS} = 0$, $V_{DS} = 25V$, f = 1 MHz
C_{oss}	Output Capacitance	All		200	pF	$V_{GS} = 0$, $V_{DS} = 25V$, f = 1 MHz
C_{rss}	Reverse Transfer Capacitance	All		60	pF	$V_{GS} = 0$, $V_{DS} = 25V$, f = 1 MHz
$t_{d(on)}$	Turn-On Delay Time	All		30	ns	$V_{DD} = 200V$, $I_D \approx 2.5A$, $R_L = 80\Omega$, $R_g = 10\Omega$ (Fig. 1)
t_r	Rise Time	All		30	ns	$V_{DD} = 200V$, $I_D \approx 2.5A$, $R_L = 80\Omega$, $R_g = 10\Omega$ (Fig. 1)
$t_{d(off)}$	Turn-Off Delay Time	All		55	ns	$V_{DD} = 200V$, $I_D \approx 2.5A$, $R_L = 80\Omega$, $R_g = 10\Omega$ (Fig. 1)
t_f	Fall Time	All		30	ns	$V_{DD} = 200V$, $I_D \approx 2.5A$, $R_L = 80\Omega$, $R_g = 10\Omega$ (Fig. 1)
Drain-Source Diode Characteristics						
			Typ			
V_{SD}	Forward On Voltage	All	−1.2		V	$I_S = -4.5A$ $V_{GS} = 0$ (Note 1)
t_{rr}	Reverse Recovery Time	All	400		ns	$I_F = I_R = -4.5A$, $V_{GS} = 0$(Fig. 2)

Note:
1. Pulse test: 80 μs–300 μs, 1% duty cycle.

Refer to VNDA50 Design Curves (See Section 4)

TEST CIRCUITS

FIGURE 1 Switching Test Circuit

P.W. = 1 μs
DUTY CYCLE = 1%

$C_S \leq 50$ pF

FIGURE 2 JEDEC Reverse Recovery Circuit

IRF440 ■ IRF441 ■ IRF442 ■ IRF443
IRF840 ■ IRF841 ■ IRF842 ■ IRF843

Siliconix

Advanced Information

500V N-Channel Enhancement Mode MOSPOWER

These power FETs are designed especially for off-line switching regulators, converters, solenoid and relay drivers.

FEATURES

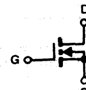
- High Voltage
- No Second Breakdown
- High Input Impedance
- Internal Drain-Source Diode
- Very Rugged: Excellent SOA
- Extremely Fast Switching

BENEFITS

- Reduced Component Count
- Improved Performance
- Simpler Designs
- Improved Reliability

Product Summary

Part Number	BV_{DSS}	$R_{DS(ON)}$	I_D	Package
IRF440	500V	0.85Ω	8.0A	TO-3
IRF441	450V			
IRF442	500V	1.10Ω	7.0A	
IRF443	450V			
IRF840	500V	0.85Ω	8.0A	TO-220AB
IRF841	450V			
IRF842	500V	1.10Ω	7.0A	
IRF843	450V			



ABSOLUTE MAXIMUM RATINGS ($T_C = 25°C$ unless otherwise noted)

Drain-Source Voltage
- IRF440, 442, 840, 842 .... 500V
- IRF441, 443, 841, 843 .... 450V

Drain-Gate Voltage
- IRF440, 442, 840, 842 .... 500V
- IRF441, 443, 841, 843 .... 450V

Drain Current Continuous[1]
- IRF440, 441, 840, 841 .... ± 8A
- IRF442, 443, 842, 843 .... ± 7A

Drain Current
Pulsed (80μs to 300μs, 1% duty cycle) .... ± 32A

Gate Current (Peak) .... ± 3A

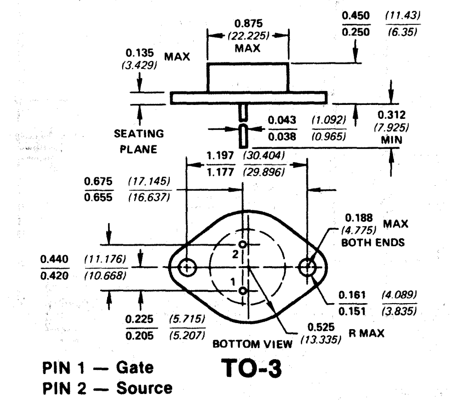
Gate-Source Voltage .... ± 40V

Total Power Dissipation .... 125 W
Linear Derating Factor .... 1.0 W/°C

Operating and Storage Temperature .... -55°C to + 150°C

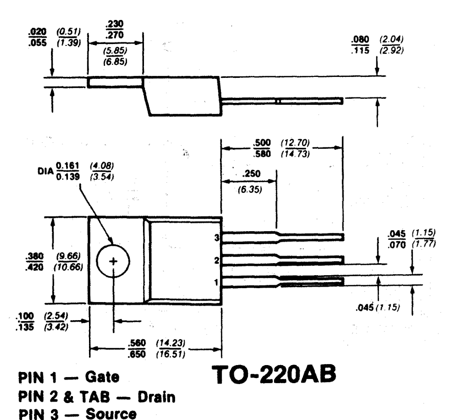
Notes:
1. Limited by package dissipation.

PACKAGE DIMENSIONS



TO-3

PIN 1 — Gate
PIN 2 — Source
CASE — Drain



TO-220AB

PIN 1 — Gate
PIN 2 & TAB — Drain
PIN 3 — Source

ELECTRICAL CHARACTERISTICS ($T_C = 25°C$ unless otherwise noted)

	Parameter	Part Number	Min	Typ	Max	Unit	Test Conditions
Static							
BV_{DSS}	Drain-Source Breakdown Voltage	IRF440, 442 IRF840, 842	500			V	$V_{GS} = 0$, $I_D = 250\mu A$
		IRF441, 443 IRF841, 843	450				
$V_{GS(th)}$	Gate Threshold Voltage	All	2.0	3.3	4.0	V	$V_{DS} = V_{GS}$, $I_D = 1$ mA
I_{GSS}	Gate-Body Leakage	All		10	±100	nA	$V_{GS} = \pm 20V$, $V_{DS} = 0$
I_{DSS}	Zero Gate Voltage Drain Current	All		0.1	0.25	mA	V_{DS} = Rated V_{DS}, $V_{GS} = 0V$
				0.2	1.0		V_{DS} = Rated V_{DS}, $V_{GS} = 0V$, $T_C = 125°C$
$I_{D(on)}$	On-State Drain Current	All	8.0			A	$V_{DS} = 25V$, $V_{GS} = 10V$ (Note 1)
$r_{DS(on)}$	Static Drain-Source On-State Resistance	IRF440, 441 IRF840, 841		0.8	0.85	Ω	$V_{GS} = 10V$, $I_D = 4A$ (Note 1)
		IRF442, 443 IRF842, 843		1.00	1.10		
Dynamic							
g_{fs}	Forward Transconductance	All	4.0	6.5		S	$V_{DS} = 25V$, $I_D = 4A$ (Note 1)
C_{iss}	Input Capacitance	All		1225	1600	pF	$V_{GS} = 0$, $V_{DS} = 25V$, f = 1 MHz
C_{oss}	Output Capacitance			200	350		
C_{rss}	Reverse Transfer Capacitance			85	150		
$t_{d(on)}$	Turn-On Delay Time	All		17	35	ns	$V_{DD} = 200V$, $I_D \approx 4A$, $R_L = 50\Omega$, $R_g = 10\Omega$ $V_{GS} = 10V$ (Fig. 1)
t_r	Rise Time	All		5	15		
$t_{d(off)}$	Turn-Off Delay Time	All		42	90		
t_f	Fall Time	All		14	30		
Drain-Source Diode Characteristics							
V_{SD}	Forward On Voltage	All		−2.0		V	$I_S = -8A$, $V_{GS} = 0$ (Note 1)
t_{rr}	Reverse Recovery Time	All		800		ns	$I_F = -8A$, $V_{GS} = 0$, di/dt = 100A/µs (Fig. 2)

Note 1: Pulse test — 80 µs to 300 µs, 1% duty cycle

TEST CIRCUITS

FIGURE 1 Switching Test Circuit

V_{IN} V_{DD} R_L V_{OUT} Rgen 20V R_g C_S
PULSE GENERATOR
CIRCUIT UNDER TEST
P.W. = 1 µs
DUTY CYCLE = 1%
$C_S \leq 50$ pF

FIGURE 2 JEDEC Reverse Recovery Circuit

50 Ω
di/dt Adjust (1 - 27 µH)
IN4933
.5 TO 50µF $I_{(PK)}$ Adjust
240 Ω
4000µF
IN4001
R ≦ 0.25 Ω
L ≦ 0.01µH
IN4723
2N4204
SCOPE
FROM TRIGGER CKT

IRF450 ■ IRF451 ■ IRF452 ■ IRF453

Advanced Information

500V N-Channel Enhancement Mode MOSPOWER

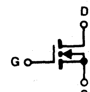
These power FETs are designed especially for off-line switching regulators, converters, solenoid and relay drivers.

FEATURES

- High Voltage
- No Second Breakdown
- High Input Impedance
- Internal Drain-Source Diode
- Very Rugged: Excellent SOA
- Extremely Fast Switching

Product Summary

Part Number	BV_{DSS}	$R_{DS(ON)}$	I_D	Package
IRF450	500V	0.4Ω	13A	TO-3
IRF451	450V			
IRF452	500V	0.5Ω	12A	
IRF453	450V			



BENEFITS

- Reduced Component Count
- Improved Performance
- Simpler Designs
- Improved Reliability

ABSOLUTE MAXIMUM RATINGS (T_C = 25°C unless otherwise noted)

Drain-Source Voltage
- IRF450 .... 500V
- IRF451 .... 450V
- IRF452 .... 500V
- IRF453 .... 450V

Drain-Gate Voltage
- IRF450 .... 500V
- IRF451 .... 450V
- IRF452 .... 500V
- IRF453 .... 450V

Drain Current Continuous
- IRF450, 451 .... ± 13A
- IRF452, 453 .... ± 12A

Drain Current
Pulsed (80μs to 300μs, 1% duty cycle) .... ± 52A

Gate Current (Peak) .... ± 3A

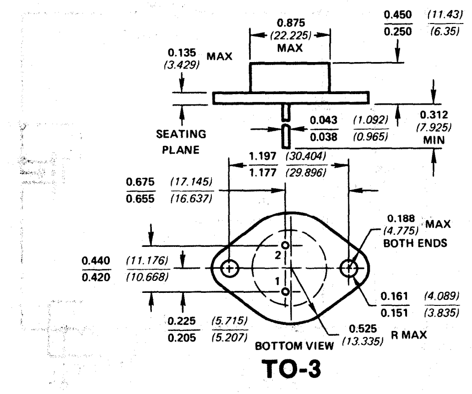
Gate-Source Voltage .... ±40V

Total Power Dissipation .... 150 W

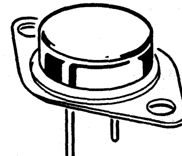
Linear Derating Factor .... 1.2 W/°C

Operating and Storage
Temperature .... -55°C to + 150°C

PACKAGE DIMENSIONS



TO-3



PIN 1 — Gate
PIN 2 — Source
CASE — Drain

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Symbol	Parameter	Part Number	Min	Typ	Max	Unit	Test Conditions
Static							
BV_{DSS}	Drain-Source Breakdown Voltage	IRF450 IRF452	500			V	V_{GS} = 0, I_D = 250μA
		IRF451 IRF453	450				
$V_{GS(th)}$	Gate Threshold Voltage	All	2.0	3.2	4.0	V	V_{DS} = V_{GS}, I_D = 1 mA
I_{GSS}	Gate-Body Leakage	All		50	±100	nA	V_{GS} = ±20V, V_{DS} = 0
I_{DSS}	Zero Gate Voltage Drain Current	All		0.1	0.25	mA	V_{DS} = 0.8 Rated V_{DS}, V_{GS} = 0
				0.5	1.0		V_{DS} = Rated V_{DS}, V_{GS} = 0, T_C = 125°C
$I_{D(on)}$	On-State Drain Current	All	13			A	V_{DS} = 25V, V_{GS} = 10V (Note 1)
$r_{DS(on)}$	Static Drain-Source On-State Resistance	IRF450 IRF451		0.3	0.4	Ω	V_{GS} = 10V, I_D = 7A (Note 1)
		IRF452 IRF453		0.4	0.5		
Dynamic							
g_{fs}	Forward Transconductance	All	6	10		S	V_{DS} = 25V, I_D = 7A (Note 1)
C_{iss}	Input Capacitance	All		2000	3000	pF	V_{GS} = 0, V_{DS} = 25V, f = 1 MHz
C_{oss}	Output Capacitance			400	600		
C_{rss}	Reverse Transfer Capacitance			100	200		
$t_{d(on)}$	Turn-On Delay Time	All		40	35	ns	V_{DD} = 210V, I_D = 7A, R_L = 30Ω, R_g = 10Ω (Fig. 1)
t_r	Rise Time	All		60	50		
$t_{d(off)}$	Turn-Off Delay Time	All		200	150		
t_f	Fall Time	All		90	70		
Drain-Source Diode Characteristics							
V_{SD}	Forward On Voltage	All		−1.3		V	I_S = −13A, V_{GS} = 0 (Note 1)
t_{rr}	Reverse Recovery Time	All		400		ns	I_F = −13A, V_{GS} = 0, di/dt = 100A/μs (Fig. 2)

Note 1: Pulse test — 80 μs to 300 μs, 1% duty cycle

TEST CIRCUITS

FIGURE 1 Switching Test Circuit

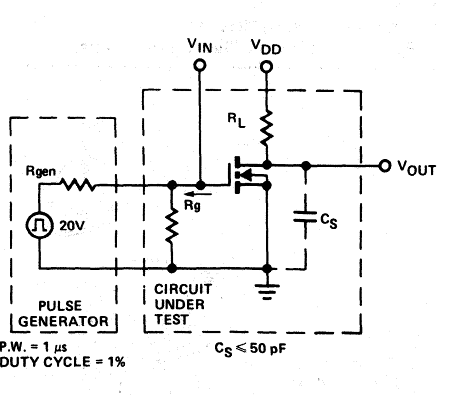


FIGURE 2 JEDEC Reverse Recovery Circuit

VNL001A ■ VNM001A ■ VNN002A ■ VNP002A

Siliconix

500V N-Channel Enhancement Mode MOSPOWER

These power FETs are designed especially for offline switching regulators, converters, solenoid and relay drivers.

FEATURES

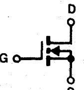
- 200°C Rating
- High Voltage
- No Second Breakdown
- High Input Impedance
- Internal Drain-Source Diode
- Very Rugged: Excellent SOA
- Extremely Fast Switching

Product Summary

Part Number	PRO ELECTRON Part Number	BV_{DSS}	$R_{DS(on)}$	I_D	Package
VNL001A	BUP68	350V	1Ω	8A	TO-3
VNM001A	BUP69	400V			
VNN002A	BUP70	450V	1.5Ω	6.5A	
VNP002A	BUP71	500V			

BENEFITS

- Reduced Component Count
- Improved Performance
- Simpler Designs
- Improved Reliability



ABSOLUTE MAXIMUM RATINGS ($T_C = 25°C$ unless otherwise noted)

Drain-Source Voltage
- VNL001A 350V
- VNM001A 400V
- VNN002A 450V
- VNP002A 500V

Drain-Gate Voltage
- VNL001A 350V
- VNM001A 400V
- VNN002A 450V
- VNP002A 500V

Drain Current
- Continuous[1]
  - VNL001A, VNM001A . . . . ±8.0A
  - VNN002A, VNP002A . . . . ±6.5A
- Pulsed[2]
  - VNL001A, VNM001A . . . . ±16A
  - VNN002A, VNP002A . . . . ±10A

Gate Current (Peak) . . . . ±3A

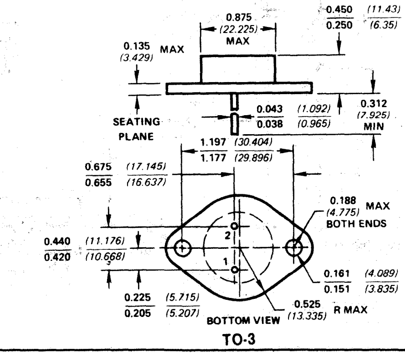
Gate-Source Voltage . . . . ±40V

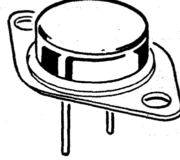
Total Power Dissipation 175W
- Linear Derating Factor . . . . 1.0W/°C

Storage and Junction Temperature . . . . −55 to 200°C

Notes:
1. Limited by package dissipation.
2. Pulse test—80μs to 300μs, 1% duty cycle.

PACKAGE DIMENSIONS





PIN 1 — Gate
PIN 2 — Source
CASE — Drain

ELECTRICAL CHARACTERISTICS ($T_C = 25°C$ unless otherwise noted)

Symbol	Parameter	Part Number	Min	Max	Unit	Test Conditions
		Static				
BV_{DSS}	Drain-Source Breakdown	VNL001A	350		V	$V_{GS} = 0$, $I_D = 1$ mA
		VNM001A	400			
		VNN002A	450			
		VNP002A	500			
$V_{GS(th)}$	Gate Threshold Voltage	All	3	6		$V_{GS} = V_{DS}$, $I_D = 1$ mA
I_{GSS}	Gate Body Leakage	All		100	nA	$V_{GS} = 30V$, $V_{DS} = 0$
I_{DSS}	Zero Gate Voltage Drain Current	All		1	mA	V_{DS} = Rated V_{DS}, $V_{GS} = 0$
				2.5		V_{DS} = Rated V_{DS}, $V_{GS} = 0$, $T_C = 150°C$
$V_{DS(on)}$	Drain-Source Saturation Voltage	VNL001A VNM001A		2	V	$V_{GS} = 10V$, $I_D = 2A$ (Note 1)
		VNN002A VNP002A		3		
$r_{DS(on)}$	Drain-Source On Resistance	VNL001A VNM001A		1	Ω	$V_{GS} = 10V$, $I_D = 2A$ (Note 1)
		VNN002A VNP002A		1.5		
$I_{D(on)}$	On-State Drain Current	All	8		A	$V_{DS} = 30V$, $V_{GS} = 10V$ (Note 1)
		Dynamic				
g_{fs}	Forward Transconductance	All	2.5		mS	$V_{DS} = 30V$, $I_D = 2A$ (Note 1)
C_{iss}	Input Capacitance	All		1000	pF	$V_{GS} = 0$, $V_{DS} = 30V$, f = 1 MHz
C_{rss}	Reverse Transfer Capacitance	All		40		
C_{oss}	Common-Source Output Capacitance	All		220		
$t_{d(on)}$	Turn-On Delay Time	All		50	ns	$V_{DD} = 200V$, $I_D \approx 2A$, $R_L = 100\Omega$, $R_g = 10\Omega$, (Figure 1)
t_r	Rise Time	All		50		
$t_{d(off)}$	Turn-Off Delay Time	All		100		
t_f	Fall Time	All		100		
		Drain-Source Diode Characteristics				
			Typ			
V_{SD}	Forward On Voltage	All	−1.2		V	$I_S = -4A$, $V_{GS} = 0$ (Note 1)
t_{rr}	Reverse Recovery Time	All	400		ns	$I_F = I_R = 4A$, $V_{GS} = 0$ (Figure 2)

Note:
1. Pulse test—80μs to 300μs, 1% duty cycle.

Refer to VNDA / 200°C Design Curves (See Section 4)

TEST CIRCUITS

FIGURE 1 Switching Test Circuit

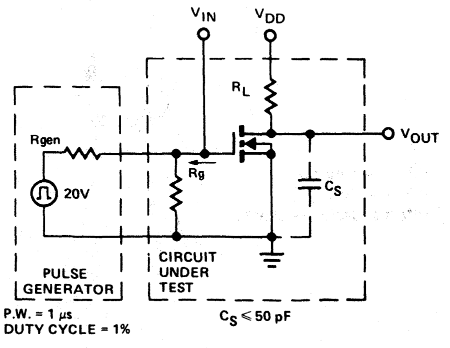
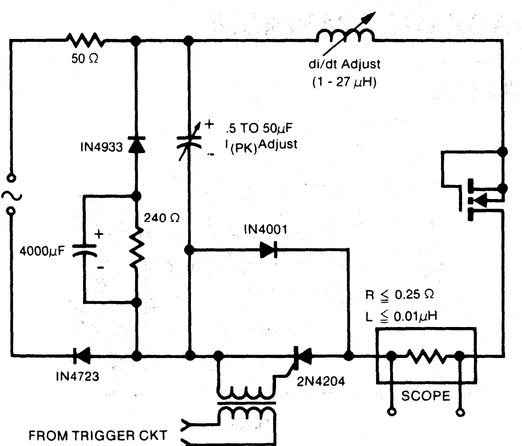


FIGURE 2 JEDEC Reverse Recovery Circuit



VN10KE ■ VN10LE

60V N-Channel Enhancement Mode MOSPOWER

These power FETs are designed especially for low power high frequency inverters, interface to CMOS and TTL logic, and line drivers.

FEATURES

- High Input Impedance
- Extremely Fast Switching
- Rugged—Dissipation Limited SOA
- Internal Drain-Source Diode

BENEFITS

- Reduced Component Count
- Simpler Designs
  - — Directly Interfaces CMOS & TTL
- Improved Circuit Performance
- Increased Reliability

Product Summary

Part Number	BV_{DSS} (Volts)	$R_{DS(ON)}$ (Ohms)	Package
VN10KE	60	5	TO-52
VN10LE	60	5	TO-52

D G S VN10KE

D G S VN10LE

ABSOLUTE MAXIMUM RATINGS ($T_A = 25°C$ unless otherwise noted)

Drain-Source Voltage 60V

Drain-Gate Voltage 60V

Gate Current (Peak) .... 100 mA

Gate-Source Voltage
- VN10KE .... +15V, −0.3V
- VN10LE .... ±40V

Drain Current
- Continuous[1] .... ±0.2A
- Pulsed[2]...................... ±1A

Maximum Dissipation at 25°C Case 0.315W

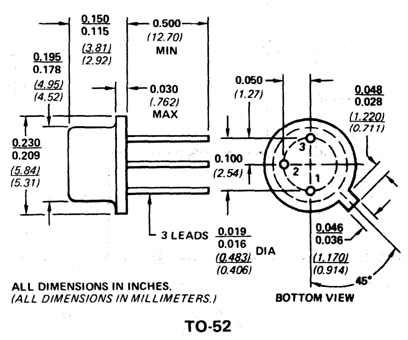
Linear Derating Factor .... 2.5 mW/°C

Operating and Storage Temperature .... −55°C to +150°C

Lead Temperature (1/16" from Case for 10 secs) .. +300°C

Notes:
1. Limited by package dissipation.
2. Pulse test—80μs to 300μs, 1% duty cycle.

PACKAGE DIMENSIONS



TO-52

PIN 1 — Source
PIN 2 — Gate
PIN 3 & CASE — Drain

3 2 1

ELECTRICAL CHARACTERISTICS ($T_C = 25°C$ unless otherwise noted)

Parameter		Part Number	Min	Max	Unit	Test Conditions
Static						
BV_{DSS}	Drain-Source Breakdown	All	60		V	$I_D = 100\ \mu A$, $V_{GS} = 0$
$V_{GS(th)}$	Gate Threshold Voltage	All	0.8	2.5	V	$V_{DS} = V_{GS}$, $I_D = 1$ mA
I_{GSS}	Gate-Body Leakage	VN10KE		100	nA	$V_{GS} = 15V$, $V_{DS} = 0$
		VN10LE		100	nA	$V_{GS} = 30V$, $V_{DS} = 0$
I_{DSS}	Zero Gate Voltage Drain Current	All		10	μA	$V_{DS} = 50V$, $V_{GS} = 0$
$I_{D(on)}$	ON-State Drain Current	All	0.75		A	$V_{DS} = 15V$, $V_{GS} = 10V$ (Note 1)
$V_{DS(on)}$	Drain-Source Saturation Voltage	All		1.5	V	$V_{GS} = 5V$, $I_D = 0.2A$ (Note 1)
				2.5		$V_{GS} = 10V$, $I_D = 0.5A$ (Note 1)
$r_{DS(on)}$	Static-Drain-Source ON-State Resistance	All		7.5	Ω	$V_{GS} = 5V$, $I_D = 0.2A$ (Note 1)
				5.0		$V_{GS} = 10V$, $I_D = 0.5A$ (Note 1)
Dynamic						
g_{fs}	Forward Transconductance	All	200		mS	$V_{DS} = 15V$, $I_D = 0.5A$ (Note 1)
C_{iss}	Input Capacitance	All		60	pF	$V_{DS} = 25V$, f = 1 MHz
C_{rss}	Reverse Transfer Capacitance			5		
C_{oss}	Common Source Output Capacitance			25		
t_{ON}	Turn-ON Time	All		10	ns	$V_{DD} = 15V$, $R_L = 23Ω$, $R_g = 25Ω$, $I_D = 0.6A$
t_{OFF}	Turn-OFF Time	All		10		
Drain-Source Diode Characteristics						
			Typ			
V_{SD}	Forward ON Voltage	All	−0.85		V	$I_S = -0.5A$, $V_{GS} = 0$ (Note 1)
t_{rr}	Reverse Recovery Time	All	160		ns	$V_{GS} = 0$, $I_F = I_R = 0.5A$

Note:
1. Pulse test: 80–300 μs, 1% duty cycle.

Refer to VNML ■ VNMK Design Curves (See Section 4)

TEST CIRCUITS

FIGURE 1 Switching Test Circuit

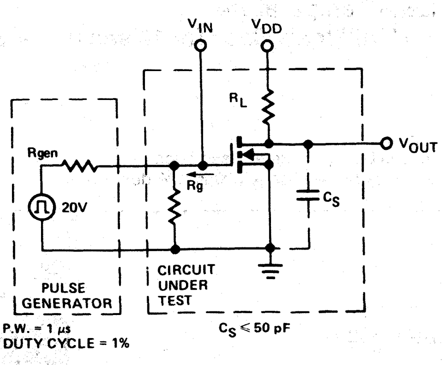
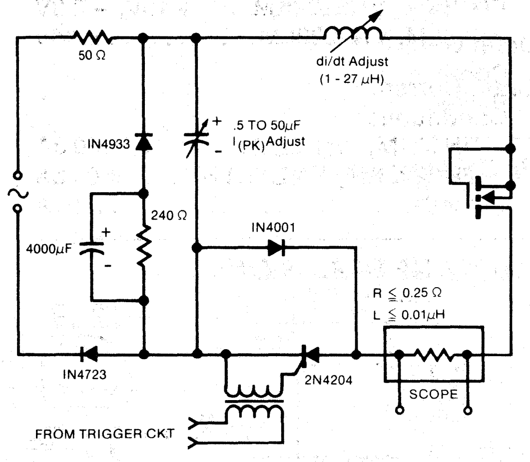


FIGURE 2 JEDEC Reverse Recovery Circuit



VN10KM ■ VN10LM ■ VN2222KM ■ VN2222LM

Siliconix

60V N-Channel Enhancement Mode MOSPOWER

These power FETs are designed especially for low power high frequency inverters, interface to CMOS and TTL logic, and line drivers.

FEATURES

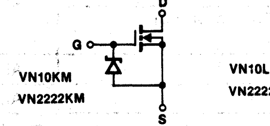
- High Input Impedance
- Extremely Fast Switching
- Rugged—Dissipation Limited SOA
- Internal Drain-Source Diode
- Low Cost Package

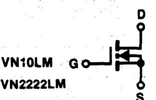
BENEFITS

- Reduced Component Count
- Simpler Designs
  - — Directly Interfaces CMOS & TTL
- Improved Circuit Performance
- Increased Reliability

Product Summary

Part Number	PRO ELECTRON Part Number	BV_{DSS} (Volts)	$R_{DS(on)}$ (Ohms)	Package
VN10KM		60	5	TO-237
VN10LM	BSR65	60	5	TO-237
VN2222KM		60	7.5	TO-237
VN2222LM	BSR64	60	7.5	TO-237





ABSOLUTE MAXIMUM RATINGS ($T_A = 25°C$ unless otherwise noted)

Drain-Source Voltage 60V

Drain-Gate Voltage 60V

Gate Current (Peak) . . . . ±400mA

Gate-Source Voltage
  VN10KM, VN2222KM . . . . + 15V, − 0.3V
  VN10LM, VN2222LM . . . . ± 40V

Drain Current
  Continuous[1]
    VN10KM, VN10LM . . . . ±0.3A
    VN2222KM, VN2222LM . . . . . ±0.25A
  Pulsed[2] . . . . ± 1A

Maximum Dissipation
  at 25°C 1W

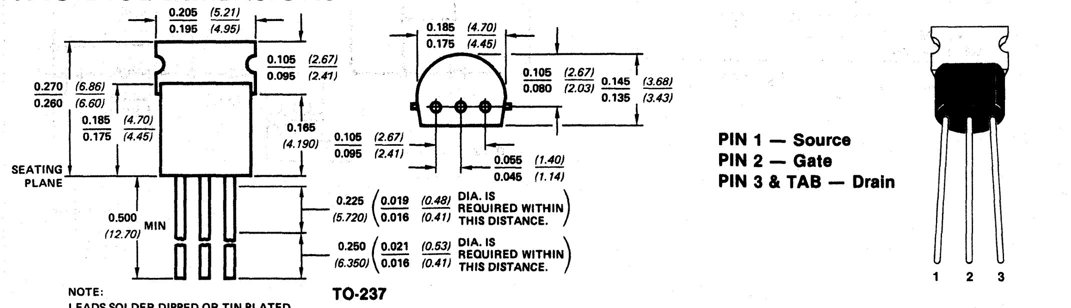
Linear Derating Factor . . . . 8 mW/°C

Operating and Storage
  Temperature . . . . −55°C to +150°C

Lead Temperature
  (1/16" from Case for 10 secs) . . +300°C

Notes:
1. Limited by package dissipation.
2. Pulse test—80μs to 300μs, 1% duty cycle.

PACKAGE DIMENSIONS



ELECTRICAL CHARACTERISTICS ($T_C = 25°C$ unless otherwise noted)

Parameter		Part Number	Min	Max	Unit	Test Conditions
Static						
BV_{DSS}	Drain-Source Breakdown	All	60		V	$V_{GS} = 0$, $I_D = 100\ \mu A$
$V_{GS(th)}$	Gate Threshold Voltage	VN10KM VN10LM	0.8	2.5	V	$V_{DS} = V_{GS}$, $I_D = 1\ mA$
		VN2222KM VN2222LM	0.6	2.5		
BV_{GSS}	Gate-Source Breakdown	VN10KM VN2222KM	15		V	$V_{DS} = 0$, $I_G = 10\ \mu A$
I_{GSS}	Gate Body Leakage	All		100	nA	$V_{DS} = 0$, $V_{GS} = 15V$
I_{DSS}	Zero Gate Voltage Drain Current	All		10	μA	$V_{DS} = 45V$, $V_{GS} = 0$
$V_{DS(on)}$	Drain-Source Saturation Voltage[1]	All		1.5	V	$V_{GS} = 5V$, $I_D = 200\ mA$
		VN10KM VN10LM		2.5		$V_{GS} = 10V$, $I_D = 500\ mA$
		VN2222KM VN2222LM		3.75		
$r_{DS(on)}$	Static Drain-Source ON-State Resistance[1]	All		7.5	Ω	$V_{GS} = 5V$, $I_D = 200\ mA$
		VN10KM VN10LM		5.0		$V_{GS} = 10V$, $I_D = 500\ mA$
		VN2222KM VN2222LM		7.5		
$I_{D(on)}$	ON-State Drain Current[1]	All	0.75		A	$V_{DS} = 15V$, $V_{GS} = 10V$
Dynamic						
g_{fs}	Forward Transconductance[1]	All	100		mS	$V_{DS} = 15V$, $I_D = 500\ mA$
C_{iss}	Input Capacitance	All		60	pF	$V_{DS} = 25V$, $V_{GS} = 0$, $f = 1\ MHz$
C_{rss}	Reverse Transfer Capacitance			5.0		
C_{oss}	Common Source Output Capacitance			25		
t_{ON}	Turn-ON Time	All		10	ns	$V_{DD} = 15V$, $I_D \approx 0.6A$, $R_L = 23\Omega$, $R_g = 25\Omega$
t_{OFF}	Turn-OFF Time	All		10		
Drain-Source Diode Characteristics						
			Typ			
V_{SD}	Forward ON Voltage[1]	All	−0.85		V	$I_S = -1A$, $V_{GS} = 0$
t_{rr}	Reverse Recovery Time	All	160		ns	$V_{GS} = 0$, $I_F = I_R = 0.5A$

Note:
1. Pulse test: 80–300 μs, 1% duty cycle.

Refer to VNML/VNMK Design Curves (See Section 4)

TEST CIRCUITS

FIGURE 1. Switching Test Circuit

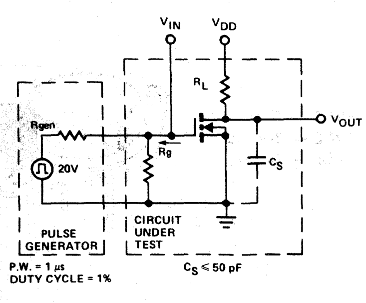
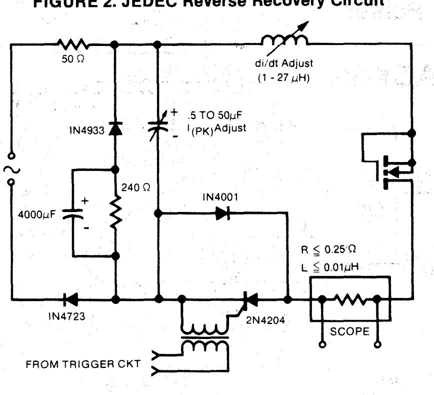


FIGURE 2. JEDEC Reverse Recovery Circuit



2N6656 ■ VN35AA

35V N-Channel Enhancement Mode MOSPOWER

These power FETs are designed especially for low power high frequency inverters, interface to CMOS and TTL logic, and line drivers.

FEATURES

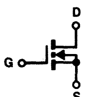
- High Input Impedance
- Extremely Fast Switching
- Rugged—Dissipation Limited SOA
- Internal Drain-Source Diode

BENEFITS

- Reduced Component Count
- Simpler Designs
  - — Directly Interfaces CMOS & TTL
- Improved Circuit Performance
- Increased Reliability

Product Summary

Part Number	BV_{DSS} (Volts)	$R_{DS(ON)}$ (Ohms)	Package
2N6656	35	1.8	TO-3
VN35AA	35	2.5	TO-3



ABSOLUTE MAXIMUM RATINGS ($T_A = 25°C$ unless otherwise noted)

Drain-Source Voltage 35V

Drain-Gate Voltage 35V

Gate Current (Peak) . . . . ±1A

Gate-Source Voltage . . . . ± 40V

Drain Current
  Continuous[1] . . . . ±2A
  Pulsed[2] . . . . ±3A

Maximum Dissipation at 25°C Case . . 25W

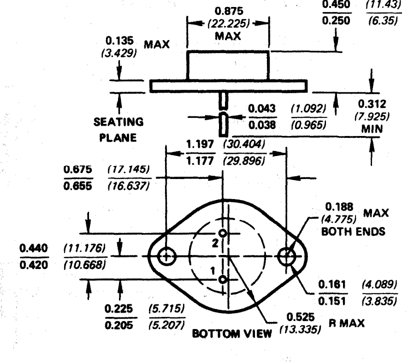
Linear Derating Factor . . . . 200 mW/°C

Operating and Storage
  Temperature . . . . −55°C to +150°C

Lead Temperature
  (1/16" from Case for 10 secs) . . +300°C

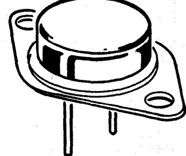
Notes:
1. Limited by package dissipation.
2. Pulse test—80μs to 300μs, 1% duty cycle.

PACKAGE DIMENSIONS



TO-3

PIN 1 — Gate
PIN 2 — Source
CASE — Drain



ELECTRICAL CHARACTERISTICS ($T_C = 25°C$ unless otherwise noted)

Symbol	Parameter	Part Number	Min	Max	Unit	Test Conditions
	Static					
BV_{DSS}	Drain-Source Breakdown Voltage	All	35		V	$V_{GS} = 0$, $I_D = 10\ \mu A$
$V_{GS(th)}$	Gate Threshold Voltage	All	.8	2.0	V	$V_{DS} = V_{GS}$, $I_D = 1$ mA
I_{GSS}	Gate-Body Leakage Current	All		100	nA	$V_{GS} = 15V$, $V_{DS} = 0$
				500		$V_{GS} = 15V$, $V_{DS} = 0$, $T_A = 125°C$
I_{DSS}	Zero Gate Voltage Drain Current	All		10	μA	$V_{GS} = 0$, $V_{DS} =$ Max Rating
				500		$V_{GS} = 0$, $V_{DS} = 0.8$ Max Rating, $T_A = 125°C$
$I_{D(on)}$	ON-State Drain Current[1]	All	1.5		A	$V_{DS} = 25V$, $V_{GS} = 10V$
$V_{DS(on)}$	Drain-Source ON-State Voltage[1]	All		1.5	V	$V_{GS} = 5V$, $I_D = 0.3A$
		VN35AA		2.5		$V_{GS} = 10V$, $I_D = 1.0A$
		2N6656		1.8		
$r_{DS(on)}$	Drain-Source ON-State Resistance[1]	All		5.0	Ω	$V_{GS} = 5V$, $I_D = 0.3A$
		2N6656		1.8		$V_{GS} = 10V$, $I_D = 1.0A$
		VN35AA		2.5		
	Dynamic					
$r_{ds(on)}$	Small Signal Drain-Source ON-State Resistance	2N6656		1.8	Ω	$V_{GS} = 10V$, $I_D = 1.0A$, f = 1 kHz
g_{fs}	Forward Transconductance[1]	All	170		mS	$V_{DS} = 24V$, $I_D = 0.5A$
C_{iss}	Input Capacitance	All		50	pF	$V_{DS} = 25V$, $V_{GS} = 0$, f = 1 MHz
C_{rss}	Reverse Transfer Capacitance	All		10		
C_{oss}	Common Source Output Capacitance	All		65		
t_{ON}	Turn-ON Time	All		10*	ns	$V_{DD} = 25V$, $I_D \approx 1A$, $R_L = 23Ω$, $R_g = 25Ω$
t_{OFF}	Turn-OFF Time	All		10*		
	Drain-Source Diode Characteristics					
			Typ			
V_{SD}	Forward ON Voltage[1]	All	−0.9		V	$I_S = -1A$, $V_{GS} = 0$
t_{rr}	Reverse Recovery Time	All	35		ns	$V_{GS} = 0$, $I_F = I_R = 1.0A$

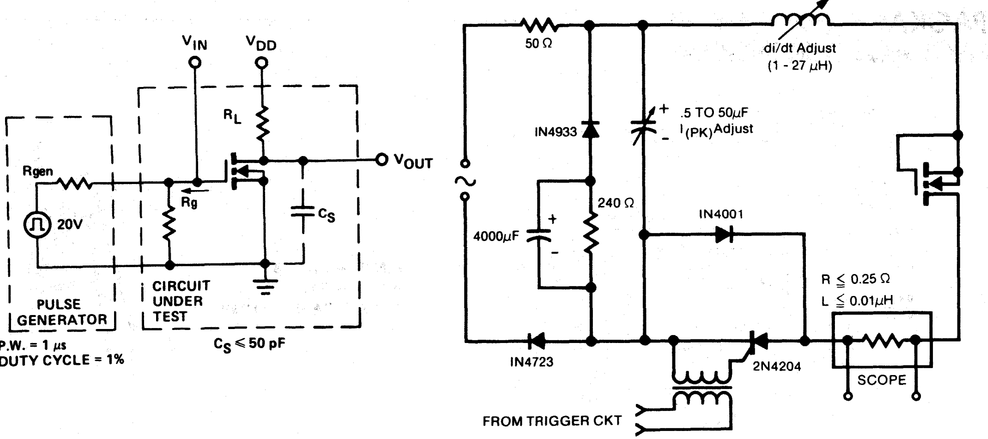
*JEDEC Devices specified at 5 ns max for each parameter $t_{d(on)}$, t_r, $t_{d(off)}$, t_f.

Refer to VNMA Design Curves (See Section 4)

Note:
1. Pulse test: 80–300 μs, 1% duty cycle.

TEST CIRCUITS

FIGURE 1. Switching Test Circuit **FIGURE 2. JEDEC Reverse Recovery Circuit**



2N6659 ■ VN35AB

Siliconix

35V N-Channel Enhancement Mode MOSPOWER

These power FETs are designed especially for low power high frequency inverters, interface to CMOS and TTL logic, and line drivers.

FEATURES

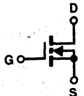
- High Input Impedance
- Extremely Fast Switching
- Rugged—Dissipation Limited SOA
- Internal Drain-Source Diode

BENEFITS

- Reduced Component Count
- Simpler Designs
  — Directly Interfaces CMOS & TTL
- Improved Circuit Performance
- Increased Reliability

Product Summary

Part Number	BV_{DSS} (Volts)	$R_{DS(ON)}$ (Ohms)	Package
2N6659	35	1.8	TO-39
VN35AB	35	2.5	TO-39



ABSOLUTE MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

Drain-Source Voltage 35V

Drain-Gate Voltage 35V

Gate Current (Peak). . . . . ±1A

Gate-Source Voltage . . . . ± 40V

Drain Current
  Continuous[1]
    2N6659 . . . . ±1.4A
    VN35AB. . . . . ±1.2A
  Pulsed[2]. . . . . ±3A

Maximum Dissipation
  at 25°C Case 6.25W

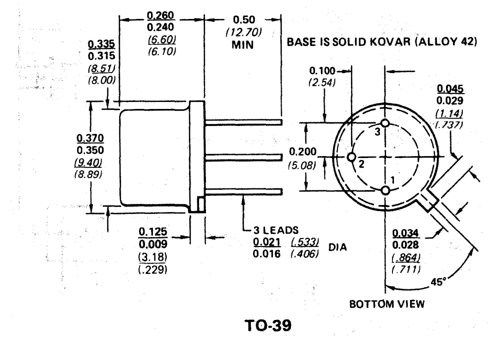
Linear Derating Factor. . . . . . . .50 mW/°C

Operating and Storage
  Temperature . . . . −55°C to +150°C

Lead Temperature
  (1/16" from Case for 10 secs) . . +300°C

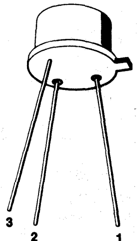
Notes:
1. Limited by package dissipation.
2. Pulse test—80μs to 300μs, 1% duty cycle.

PACKAGE DIMENSIONS



TO-39

PIN 1 — Source
PIN 2 — Gate
PIN 3 & CASE — Drain



ELECTRICAL CHARACTERISTICS (T_C=25°C unless otherwise noted)

	Parameter	Part Number	Min	Max	Unit	Test Conditions
			Static			
BV_{DSS}	Drain-Source Breakdown	All	35		V	$V_{GS} = 0$, $I_D = 10\ \mu A$
$V_{GS(th)}$	Gate Threshold Voltage	All	0.8	2	V	$V_{DS} = V_{GS}$, $I_D = 1$ mA
I_{GSS}	Gate Body Leakage	All		0.1	μA	$V_{GS} = 15V$, $V_{DS} = 0$
				0.5		$V_{GS} = 15V$, $V_{DS} = 0$, $T_A = 125°C$
I_{DSS}	Zero Gate Voltage Drain Current	All		10	μA	V_{DS} = Max Ratings, $V_{GS} = 0$
				500		V_{DS} = 0.8 Max Ratings, $V_{GS} = 0$, $T_A = 125°C$
$V_{DS(on)}$	Drain-Source Saturation Voltage[1]	All		1.5	V	$V_{GS} = 5V$, $I_D = 0.3A$
		2N6659		1.8		$V_{GS} = 10V$, $I_D = 1A$
		VN35AB		2.5		
$r_{DS(on)}$	Drain-Source ON Resistance[1]	All		5	Ω	$V_{GS} = 5V$, $I_D = 0.3A$
		2N6659		1.8		$V_{GS} = 10V$, $I_D = 1A$
		VN35AB		2.5		
$I_{D(on)}$	ON-State Drain Current[1]	All	1.5		A	$V_{DS} = 25V$, $V_{GS} = 10V$
			Dynamic			
$r_{ds(on)}$	Drain Source ON Resistance[1]	2N6659		1.8	Ω	$V_{GS} = 10V$, $I_D = 1A$, f = 1 kHz
g_{fs}	Forward Transconductance[1]	All	170		mS	$V_{DS} = 24V$, $I_D = 0.5A$
C_{iss}	Input Capacitance	All		50	pF	$V_{GS} = 0$, $V_{DS} = 25V$, f = 1 MHz
C_{rss}	Reverse Transfer Capacitance			10		
C_{oss}	Common-Source Output Capacitance			65		
t_{ON}	Turn-ON Time	All		10*	ns	$V_{DD} = 25V$, $I_D \approx 1A$, $R_L = 23\Omega$, $R_g = 25\Omega$
t_{OFF}	Turn-OFF Time	All		10*		
			Drain-Source Diode Characteristics			
			Typ			
V_{SD}	Forward ON Voltage[1]	All	−0.9		V	$I_S = -1A$, $V_{GS} = 0$
t_{rr}	Reverse Recovery Time	All	35		ns	$V_{GS} = 0$, $I_F = I_R = 1A$

*JEDEC Device meets 5 ns max for $t_{d(on)}$, t_r, $t_{d(off)}$, and t_f.

Refer to VNMA Design Curves (See Section 4)

Note:
1. Pulse test: 80 μs, 1% duty cycle.

TEST CIRCUITS

FIGURE 1. Switching Test Circuit

FIGURE 2. JEDEC Reverse Recovery Circuit

VN40AD ■ VN46AD

Siliconix

40V N-Channel Enhancement Mode MOSPOWER

These power FETs are designed especially for low power high frequency inverters, interface to CMOS and TTL logic, and line drivers.

FEATURES

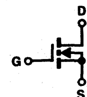
- High Input Impedance
- Extremely Fast Switching
- Rugged—Dissipation Limited SOA
- Internal Drain-Source Diode

BENEFITS

- Reduced Component Count
- Simpler Designs
  — Directly Interfaces CMOS & TTL
- Improved Circuit Performance
- Increased Reliability

Product Summary

Part Number	PRO ELECTRON Part Number	BV_{DSS} (Volts)	$R_{DS(on)}$ (Ohms)	Package
VN40AD		40	5	TO-220
VN46AD	BSR80	40	3	TO-220



ABSOLUTE MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

Drain-Source Voltage 40V

Drain-Gate Voltage 40V

Gate Current (Peak) . . . . ±0.5A

Gate-Source Voltage . . . . ± 40V

Drain Current
  Continuous[1]
    VN40AD. . . . . ±1.5A
    VN46AD. . . . . ±1.9A
  Pulsed[2]. . . . . ±3A

Maximum Dissipation at 25°C Case . . 20W

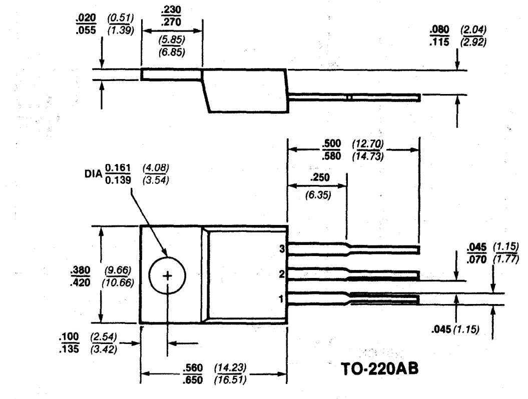
Linear Derating Factor. . . . . . . 160 mW/°C

Operating and Storage
  Temperature. . . . . −55°C to +150°C

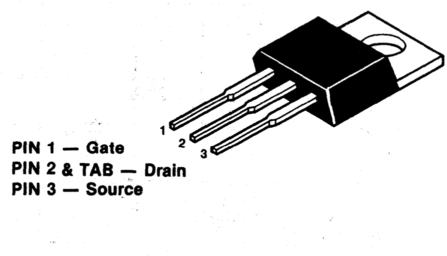
Lead Temperature
  (1/16" from Case for 10 secs) . . +300°C

Notes:
1. Limited by package dissipation.
2. Pulse test—80μs to 300μs, 1% duty cycle.

PACKAGE DIMENSIONS



TO-220AB



PIN 1 — Gate
PIN 2 & TAB — Drain
PIN 3 — Source

ELECTRICAL CHARACTERISTICS ($T_C = 25°C$ unless otherwise noted)

	Parameter	Part Number	Min	Max	Unit	Test Conditions
Static						
BV_{DSS}	Drain-Source Breakdown	All	40		V	$V_{GS} = 0$, $I_D = 10\ \mu A$
$V_{GS(th)}$	Gate-Source Threshold Voltage	All	0.80	2.5	V	$V_{DS} = V_{GS}$, $I_D = 1$ mA
I_{GSS}	Gate-Body Leakage	All		10	nA	$V_{GS} = 15V$, $V_{DS} = 0$
				100		$V_{GS} = 15V$, $V_{DS} = 0$, $T_A = 125°C$
I_{DSS}	Zero Gate Voltage Drain Current	All		10	μA	V_{DS} = Max Rating, $V_{GS} = 0$
				500		V_{DS} = Max Rating, $V_{GS} = 0$, $T_A = 125°C$
$V_{DS(on)}$	Drain-Source ON-State Voltage[1]	All		1.5	V	$V_{GS} = 5.0V$, $I_D = 300$ mA
		VN40AD		5.0		$V_{GS} = 10V$, $I_D = 1A$
		VN46AD		3.0		$V_{GS} = 10V$, $I_D = 1A$
$r_{DS(on)}$	Drain-Source ON-State Resistance[1]	All		5.0	Ω	$V_{GS} = 5.0V$, $I_D = 300$ mA
		VN40AD		5.0		$V_{GS} = 10V$, $I_D = 1A$
		VN46AD		3.0		
Dynamic						
g_{fs}	Forward Transconductance[1]	All	170		mS	$V_{DS} = 24V$, $I_D = 0.5A$
C_{iss}	Input Capacitance	All		50	pF	$V_{DS} = 25V$, $V_{GS} = 0$, f = 1 MHz
C_{rss}	Reverse Transfer Capacitance	All		10		
C_{oss}	Common Source Output Capacitance	All		50		
t_{ON}	Turn-ON Time	All		10	ns	$V_{DD} = 25V$, $I_D \approx 1A$, $R_L = 23\Omega$, $R_g = 25\Omega$
t_{OFF}	Turn-OFF Time	All		10		
Drain-Source Diode Characteristics						
			Typ			
V_{SD}	Forward ON Voltage[1]	All	−0.9		V	$I_S = -1A$, $V_{GS} = 0$
t_{rr}	Reverse Recovery Time	All	35		ns	$V_{GS} = 0$, $I_F = I_R = 1.0A$

Note:
1. Pulse test: 80–300 µs, 1% duty cycle.

Refer to VNMA Design Curves (See Section 4)

TEST CIRCUITS

FIGURE 1. Switching Test Circuit

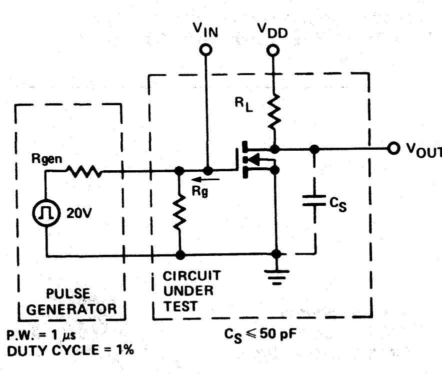
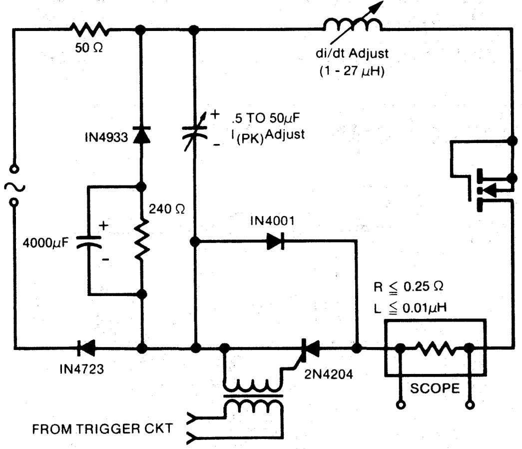


FIGURE 2. JEDEC Reverse Recovery Circuit



VN40AF ▪ VN46AF

Siliconix

40V N-Channel Enhancement Mode MOSPOWER

These power FETs are designed especially for low power high frequency inverters, interface to CMOS and TTL logic, and line drivers.

FEATURES

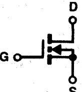
- High Input Impedance
- Extremely Fast Switching
- Rugged—Dissipation Limited SOA
- Internal Drain-Source Diode

BENEFITS

- Reduced Component Count
- Simpler Designs
  — Directly Interfaces CMOS & TTL
- Improved Circuit Performance
- Increased Reliability

Product Summary

Part Number	BV_{DSS} (Volts)	$R_{DS(ON)}$ (Ohms)	Package
VN40AF	40	5	TO-202
VN46AF	40	3	TO-202



ABSOLUTE MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

Drain-Source Voltage 40V

Drain-Gate Voltage 40V

Gate Current (Peak) . . . . ±1A

Gate-Source Voltage . . . . ± 40V

Drain Current
  Continuous[1]
    VN40AF . . . . ±1.3A
    VN46AF . . . . ±1.6A
  Pulsed[2] . . . . ±3A

Maximum Dissipation
  at 25°C Case 15W

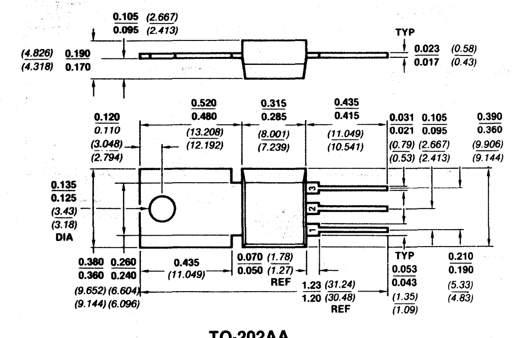
Linear Derating Factor . . . . 120 mW/°C

Operating and Storage
  Temperature . . . . −55°C to +150°C

Lead Temperature
  (1/16" from Case for 10 secs) . . +300°C

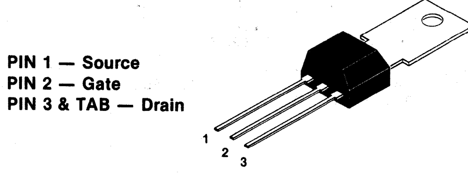
Notes:
1. Limited by package dissipation.
2. Pulse test—80μs to 300μs, 1% duty cycle.

PACKAGE DIMENSIONS



TO-202AA

PIN 1 — Source
PIN 2 — Gate
PIN 3 & TAB — Drain



ELECTRICAL CHARACTERISTICS ($T_C = 25°C$ unless otherwise noted)

Symbol	Parameter	Part Number	Min	Max	Unit	Test Conditions
		Static				
BV_{DSS}	Drain-Source Breakdown Voltage	All	40		V	$I_D = 10\ \mu A$, $V_{GS} = 0$
$V_{GS(th)}$	Gate Threshold Voltage	All	0.8		V	$I_D = 1$ mA, $V_{DS} = V_{GS}$
I_{GSS}	Gate-Body Leakage Current	All		100	nA	$V_{GS} = 15V$, $V_{DS} = 0$
I_{DSS}	Zero Gate Voltage Drain Current	All		10	μA	$V_{DS} = 0.8$ Max Rating, $V_{GS} = 0$
		All		500		$V_{DS} =$ Max Rating, $V_{GS} = 0$, $T_A = 125°C$
$I_{D(on)}$	ON-State Drain Current[1]	All	1.0		A	$V_{DS} = 25V$, $V_{GS} = 10V$
$V_{DS(on)}$	Drain-Source ON-State Voltage	All		1.5	V	$V_{GS} = 5V$, $I_D = 0.3A$
		VN40AF		5.0		$V_{GS} = 10V$, $I_D = 1A$
		VN46AF		3.0		
$r_{DS(on)}$	Drain-Source, ON-State Resistance[1]	All		5.0	Ω	$V_{GS} = 5V$, $I_D = 0.3A$
		VN40AF		5.0		$V_{GS} = 10V$, $I_D = 1A$
		VN46AF		3.0		
		Dynamic				
g_{fs}	Forward Transconductance[1]	All	170		mS	$V_{DS} = 25V$, $I_D = 0.5A$
C_{iss}	Input Capacitance	All		50	pF	$V_{DS} = 25V$, $V_{GS} = 0$, $f = 1$ MHz
C_{rss}	Reverse Transfer Capacitance	All		10		
C_{oss}	Common Source Output Capacitance	All		65		
t_{ON}	Turn-ON Time	All		10	ns	$V_{DD} = 25V$, $I_D \approx 1A$, $R_L = 23\Omega$, $R_g = 25\Omega$
t_{OFF}	Turn-OFF Time	All		10		
		Drain-Source Diode Characteristics				
			Typ			
V_{SD}	Forward ON Voltage[1]	All	−0.9		V	$I_S = -1A$, $V_{GS} = 0$
t_{rr}	Reverse Recovery Time	All	35		ns	$V_{GS} = 0$, $I_F = I_R = 1A$

Note:
1. Pulse test: 80–300 μs, 1% duty cycle.

Refer to VNMA Design Curves (See Section 4)

TEST CIRCUITS

FIGURE 1. Switching Test Circuit

V_{IN} V_{DD} R_L V_{OUT} Rgen R_g C_S 20V

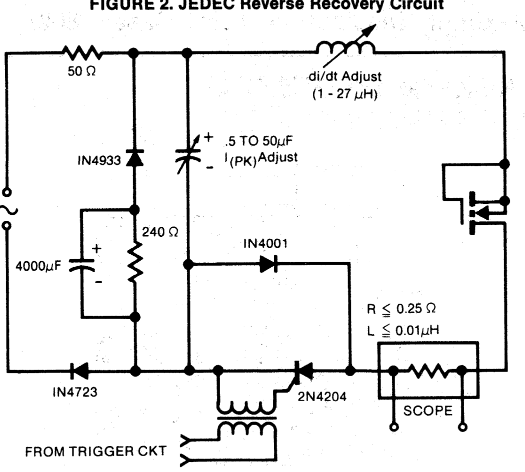
PULSE GENERATOR

CIRCUIT UNDER TEST

P.W. = 1 μs
DUTY CYCLE = 1%

$C_S \leq 50$ pF

FIGURE 2. JEDEC Reverse Recovery Circuit



VN64GA

Siliconix

60V N-Channel Enhancement Mode MOSPOWER

This power FET is designed especially for low power high frequency inverters, interface to CMOS and TTL logic, and line drivers.

FEATURES

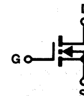
- High Input Impedance
- Extremely Fast Switching
- Rugged — Dissipation Limited SOA
- Internal Drain-Source Diode
- Low $r_{DS(on)}$

Product Summary

Part Number	BV_{DSS} (Volts)	$R_{DS(ON)}$ (Ohms)	Package
VN64GA	60	0.4	TO-3

BENEFITS

- Reduced Component Count
- Simpler Designs
  - Directly Interfaces CMOS
- Improved Circuit Performance
- Increased Reliability



ABSOLUTE MAXIMUM RATINGS ($T_A = 25°C$ unless otherwise noted)

Drain-Source Voltage 60V

Drain-Gate Voltage 60V

Gate Current (Peak) . . . . ±3A

Gate-Source Voltage . . . . ± 40V

Drain Current
  Continuous[1] . . . . ±10A
  Pulsed[2] . . . . ±15A

Maximum Dissipation at 25°C Case . . 80W

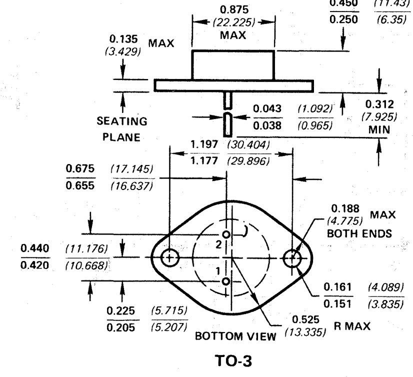
Linear Derating Factor . . . . 0.64W/°C

Operating and Storage
  Temperature . . . . −55°C to +150°C

Lead Temperature
  (1/16" from Case for 10 secs) . . +300°C

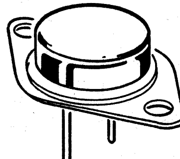
Notes:
1. Limited by package dissipation.
2. Pulse test — 80μs to 300μs, 1% duty cycle.

PACKAGE DIMENSIONS



TO-3

PIN 1 — Gate
PIN 2 — Source
CASE — Drain

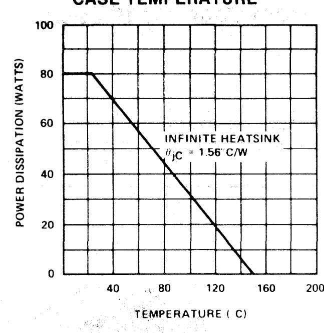


ELECTRICAL CHARACTERISTICS ($T_C = 25°C$ unless otherwise noted)

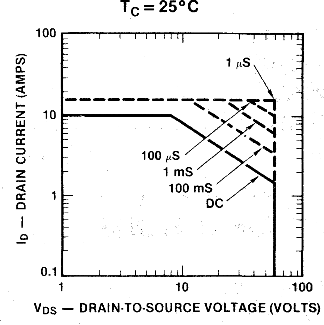
	Parameter	Min	Max	Unit	Test Conditions
	Static				
BV_{DSS}	Drain-Source Breakdown	60		V	$V_{GS} = 0$, $I_D = 500\ \mu A$
$V_{GS(th)}$	Gate Threshold Voltage	1	4	V	$V_{DS} = V_{GS}$, $I_D = 10$ mA
I_{GSS}	Gate-Body Leakage		0.1	μA	$V_{GS} = 12V$, $V_{DS} = 0$
I_{DSS}	Zero Gate Voltage Drain Current		500	μA	$V_{DS} = 60V$, $V_{GS} = 0$
$V_{DS(on)}$	Drain-Source Saturation Voltage[1]		4.0	V	$V_{GS} = 12V$, $I_D = 10A$
$r_{DS(on)}$	Static-Drain-Source ON-State Resistance[1]		0.4	Ω	$V_{GS} = 12V$, $I_D = 10A$
$I_{D(on)}$	ON-State Drain Current[1]	12.5		A	$V_{DS} = 25V$, $V_{GS} = 12V$
	Dynamic				
g_{fs}	Forward Transconductance[1]	1.5		S	$V_{DS} = 20V$, $I_D = 5A$
C_{iss}	Input Capacitance		800	pF	$V_{DS} = 25V$, $V_{GS} = 0$, f = 1 MHz
C_{rss}	Referse Transfer Capacitance		50	pF	$V_{DS} = 25V$, $V_{GS} = 0$, f = 1 MHz
C_{oss}	Common Source Output Capacitance		400	pF	$V_{DS} = 25V$, $V_{GS} = 0$, f = 1 MHz
t_{ON}	Turn-ON Time		60	ns	$V_{DD} = 50V$, $I_D \approx 5A$, $R_L = 10\Omega$, $R_g = 20\Omega$
t_{OFF}	Turn-OFF Time		80	ns	$V_{DD} = 50V$, $I_D \approx 5A$, $R_L = 10\Omega$, $R_g = 20\Omega$
	Drain-Source Diode Characteristics				
		Typ			
V_{SD}	Forward ON Voltage[1]	−0.95		V	$I_S = -4A$, $V_{GS} = 0$
t_{rr}	Reverse Recovery Time	110		ns	$V_{GS} = 0$, $I_F = I_R = 4.0A$

Note:
1. Pulse test: 80-300 μs, 1% duty cycle.

POWER DISSIPATION CASE TEMPERATURE



DC SAFE OPERATING REGION
$T_C = 25°C$



VN66AD ■ VN67AD

60V N-Channel Enhancement Mode MOSPOWER

These power FETs are designed especially for low power high frequency inverters, interface to CMOS and TTL logic, and line drivers.

FEATURES

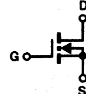
- High Input Impedance
- Extremely Fast Switching
- Rugged—Dissipation Limited SOA
- Internal Drain-Source Diode

BENEFITS

- Reduced Component Count
- Simpler Designs
  - Directly Interfaces CMOS & TTL
- Improved Circuit Performance
- Increased Reliability

Product Summary

Part Number	PRO ELECTRON Part Number	BV_{DSS} (Volts)	$R_{DS(on)}$ (Ohms)	Package
VN66AD	BSR81	60	3	TO-220
VN67AD		60	3.5	TO-220



ABSOLUTE MAXIMUM RATINGS ($T_A = 25°C$ unless otherwise noted)

Drain-Source Voltage 60V

Drain-Gate Voltage 60V

Gate Current (Peak) . . . . ±1A

Gate-Source Voltage . . . . ± 40V

Drain Current
- Continuous[1]
  - VN66AD . . . . ±1.9A
  - VN67AD . . . . ±1.8A
- Pulsed[2] . . . . ±3A

Maximum Dissipation at 25°C Case . . 20W

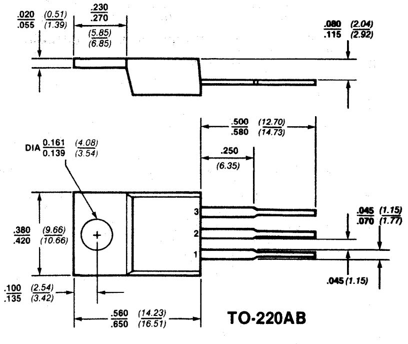
Linear Derating Factor . . . . 160 mW/°C

Operating and Storage Temperature . . . . −55°C to +150°C

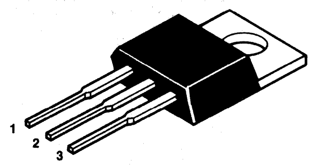
Lead Temperature (1/16" from Case for 10 secs) . . +300°C

Notes:
1. Limited by package dissipation.
2. Pulse test—80μs to 300μs, 1% duty cycle.

PACKAGE DIMENSIONS



TO-220AB



PIN 1 — Gate
PIN 2 & TAB — Drain
PIN 3 — Source

ELECTRICAL CHARACTERISTICS ($T_C = 25°C$ unless otherwise noted)

	Parameter	Part Number	Min	Max	Unit	Test Conditions
Static						
BV_{DSS}	Drain-Source Breakdown	All	60		V	$V_{GS} = 0$, $I_D = 10\ \mu A$
$V_{GS(th)}$	Gate Threshold Voltage	All	0.8	2.5	V	$V_{DS} = V_{GS}$, $I_D = 1$ mA
I_{GSS}	Gate Body Leakage	All		0.1	μA	$V_{GS} = 30V$, $V_{DS} = 0$
I_{DSS}	Zero Gate Voltage Drain Current	All		1	μA	$V_{DS} = 48V$, $V_{GS} = 0$
$V_{DS(on)}$	Drain-Source Saturation Voltage[1]	All		1.5	V	$V_{GS} = 5V$, $I_D = 300$ mA
		VN66AD		3	V	$V_{GS} = 10V$, $I_D = 1A$
		VN67AD		3.5	V	$V_{GS} = 10V$, $I_D = 1A$
$r_{DS(on)}$	Drain-Source ON Resistance[1]	All		5.0	Ω	$V_{GS} = 5V$, $I_D = 300$ mA
		VN66AD		3	Ω	$V_{GS} = 10V$, $I_D = 1A$
		VN67AD		3.5	Ω	$V_{GS} = 10V$, $I_D = 1A$
$I_{D(on)}$	ON-State Drain Current[1]	All	1.5		A	$V_{DS} = 25V$, $V_{GS} = 10V$
Dynamic						
g_{fs}	Forward Transconductance[1]	All	170		mS	$V_{DS} = 25V$, $I_D = 0.5A$
C_{iss}	Input Capacitance	All		50	pF	$V_{DS} = 25V$, $V_{GS} = 0$, $f = 1$ MHz
C_{rss}	Reverse Transfer Capacitance	All		10	pF	$V_{DS} = 25V$, $V_{GS} = 0$, $f = 1$ MHz
C_{oss}	Common Source Output Capacitance	All		50	pF	$V_{DS} = 25V$, $V_{GS} = 0$, $f = 1$ MHz
t_{ON}	Turn-ON Time	All		10	ns	$V_{DD} = 25V$, $I_D \approx 1A$, $R_L = 23\Omega$, $R_g = 25\Omega$
t_{OFF}	Turn-OFF Time	All		10	ns	$V_{DD} = 25V$, $I_D \approx 1A$, $R_L = 23\Omega$, $R_g = 25\Omega$
Drain-Source Diode Characteristics						
			Typ			
V_{SD}	Forward ON Voltage[1]	All	−0.9		V	$I_S = -1A$, $V_{GS} = 0$
t_{rr}	Reverse Recovery Time	All	35		ns	$V_{GS} = 0$, $I_F = I_R = 1A$

Note:
1. Pulse test: 80–300 μs, 1% duty cycle.

Refer to VNMA Design Curves (See Section 4)

TEST CIRCUITS

FIGURE 1. Switching Test Circuit

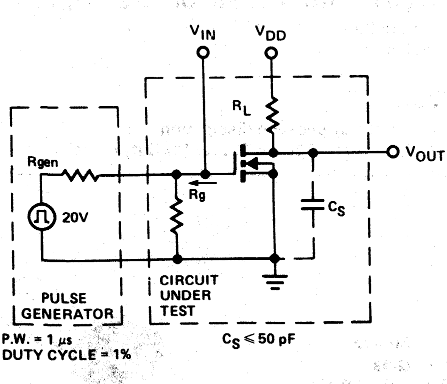
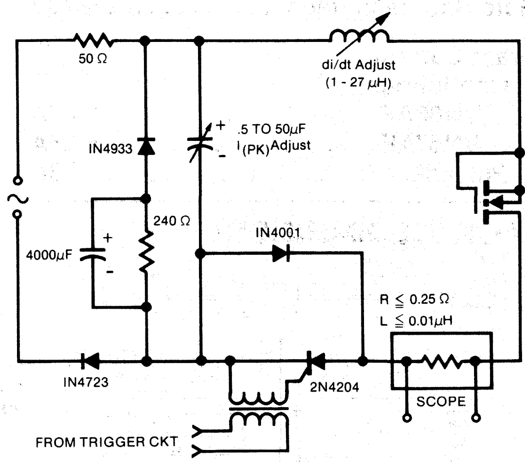


FIGURE 2. JEDEC Reverse Recovery Circuit



VN66AF ■ VN67AF

Siliconix

60V N-Channel Enhancement Mode MOSPOWER

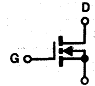
These power FETs are designed especially for low power high frequency inverters, interface to CMOS and TTL logic, and line drivers.

FEATURES

- High Input Impedance
- Extremely Fast Switching
- Rugged—Dissipation Limited SOA
- Internal Drain-Source Diode
- High Free Air Power Dissipation

Product Summary

Part Number	BV_{DSS} (Volts)	$R_{DS(ON)}$ (Ohms)	Package
VN66AF	60	3	TO-202
VN67AF	60	3.5	TO-202



BENEFITS

- Reduced Component Count
- Simpler Designs
  — Directly Interfaces CMOS & TTL
- Improved Circuit Performance
- Increased Reliability

ABSOLUTE MAXIMUM RATINGS ($T_A = 25°C$ unless otherwise noted)

Drain-Source Voltage
VN66AF, VN67AF 60V

Drain-Gate Voltage
VN66AF, VN67AF 60V

Gate Current (Peak) . . . . ±1A

Gate-Source Voltage . . . . ± 40V

Drain Current
Continuous[1]
VN66AF . . . . ±1.7A
VN67AF . . . . ±1.6A
Pulsed[2] . . . . ±3A

Maximum Dissipation
at 25°C Case 15W

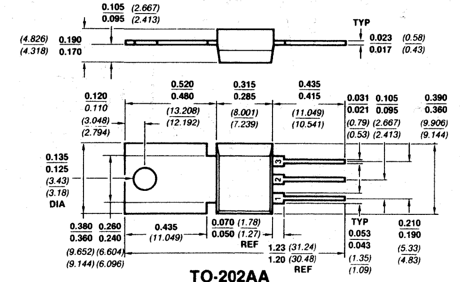
Linear Derating Factor . . . . 120 mW/°C

Operating and Storage
Temperature . . . . −55°C to +150°C

Lead Temperature
(1/16" from Case for 10 secs) . . +300°C

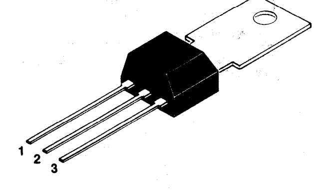
Notes:
1. Limited by package dissipation.
2. Pulse test—80μs to 300μs, 1% duty cycle.

PACKAGE DIMENSIONS



TO-202AA

PIN 1 — Source
PIN 2 — Gate
PIN 3 & TAB — Drain



ELECTRICAL CHARACTERISTICS (T_C=25°C unless otherwise noted)

	Parameter	Part Number	Min	Max	Unit	Test Conditions
			Static			
BV_{DSS}	Drain-Source Breakdown	All	60		V	$V_{GS}=0$, $I_D=10\ \mu A$
$V_{G(th)}$	Gate Threshold Voltage	All	0.8	2.5	V	$V_{DS}=V_{GS}$, $I_D=1$ mA
I_{GSS}	Gate-Body Leakage	All		100	nA	$V_{GS}=15V$, $V_{DS}=0$
I_{DSS}	Zero Gate Voltage Drain Current	All		10	μA	V_{DS} = Max Ratings, $V_{GS}=0$
		All		100		V_{DS} = 0.8 Max Ratings, $V_{GS}=0$, $T_A=125°C$
$V_{DS(on)}$	Drain-Source Saturation Voltage[1]	All		1.5	V	$V_{GS}=5V$, $I_D=0.3A$
		VN66AF		3		$V_{GS}=10V$, $I_D=1A$
		VN67AF		3.5		
$r_{DS(on)}$	Static Drain-Source ON-State Resistance[1]	All		5.0	Ω	$V_{GS}=5V$, $I_D=0.3A$
		VN66AF		3		$V_{GS}=10V$, $I_D=1A$
		VN67AF		3.5		
$I_{D(on)}$	ON-State Drain Current[1]	All	1.5		A	$V_{DS}=25V$, $V_{GS}=10V$
			Dynamic			
g_{fs}	Forward Transconductance[1]	All	170		mS	$V_{DS}=24V$, $I_D=0.5A$
C_{iss}	Input Capacitance	All		50	pF	$V_{DS}=25V$, $V_{GS}=0$, f = 1 MHz
C_{rss}	Reverse Transfer Capacitance	All		10		
C_{oss}	Common Source Output Capacitance	All		50		
t_{ON}	Turn-ON Time	All		10	ns	$V_{DD}=25V$, $I_D\approx 1A$, $R_L=23\Omega$, $R_g=25\Omega$
t_{OFF}	Turn-OFF Time	All		10		
			Drain-Source Diode Characteristics			
			Typ			
V_{SD}	Forward ON Voltage[1]	All	-0.9		V	$I_S=-1A$, $V_{GS}=0$
t_{rr}	Reverse Recovery Time	All	35		ns	$V_{GS}=0$, $I_F=I_R=1A$

Note:
1. Pulse test 80-300 μs, 1% duty cycle

Refer to VNMA Design Curves (See Section 4)

TEST CIRCUITS

FIGURE 1. Switching Test Circuit

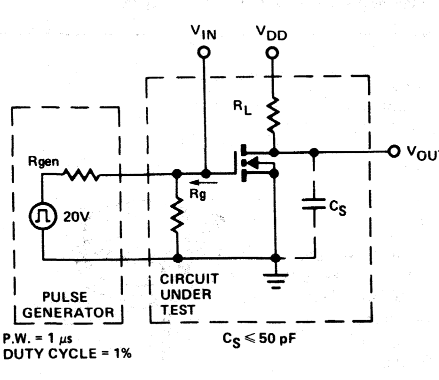
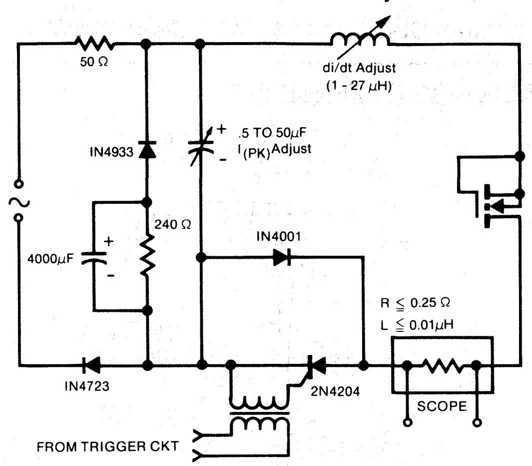


FIGURE 2. JEDEC Reverse Recovery Circuit



2N6657 ■ VN67AA

60V N-Channel Enhancement Mode MOSPOWER

These power FETs are designed especially for low power high frequency inverters, interface to CMOS and TTL logic, and line drivers.

FEATURES

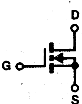
- High Input Impedance
- Extremely Fast Switching
- Rugged — Dissipation Limited SOA
- Internal Drain-Source Diode

BENEFITS

- Reduced Component Count
- Simpler Designs
  — Directly Interfaces CMOS & TTL
- Improved Circuit Performance
- Increased Reliability

Product Summary

Part Number	BV_{DSS} (Volts)	$R_{DS(ON)}$ (Ohms)	Package
2N6657	60	3	TO-3
VN67AA	60	3.5	TO-3



ABSOLUTE MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

Drain-Source Voltage 60V

Drain-Gate Voltage 60V

Gate Current (Peak) .... ±1A

Gate-Source Voltage .... ±40V

Drain Current
  Continuous[1] .... ±2A
  Pulsed[2] .... ±3A

Maximum Dissipation at 25°C Case 25W

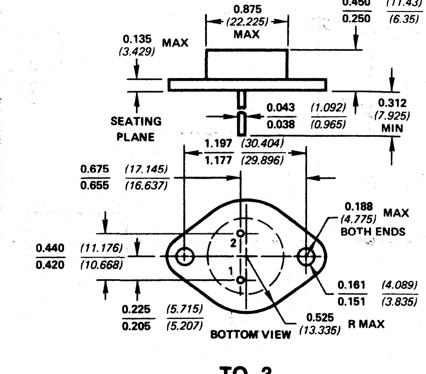
Linear Derating Factor .... 200 mW/°C

Operating and Storage
  Temperature .... −55°C to +150°C

Lead Temperature
  (1/16" from Case for 10 secs) .. +300°C

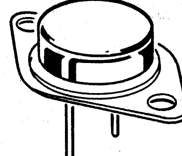
Notes:
1. Limited by package dissipation.
2. Pulse test — 80μs to 300μs, 1% duty cycle.

PACKAGE DIMENSIONS



TO-3

PIN 1 — Gate
PIN 2 — Source
CASE — Drain



ELECTRICAL CHARACTERISTICS ($T_C = 25°C$ unless otherwise noted)

	Parameter	Part Number	Min	Max	Unit	Test Conditions
Static						
BV_{DSS}	Drain-Source Breakdown	All	60		V	$V_{GS} = 0$, $I_D = 10\ \mu A$
$V_{GS(th)}$	Gate Threshold Voltage	All	0.8	2.0	V	$V_{DS} = V_{GS}$, $I_D = 1$ mA
I_{GSS}	Gate-Body Leakage	All		500	nA	$V_{GS} = 15V$, $V_{DS} = 0$, $T_A = 125°C$
I_{DSS}	Zero Gate Voltage Drain Current	All		10	μA	V_{DS} = Max Ratings, $V_{GS} = 0$
				500		V_{DS} = 0.8 Max Ratings, $V_{GS} = 0$, $T_A = 125°C$
$V_{DS(on)}$	Drain-Source Saturation Voltage[1]	All		1.5	V	$V_{GS} = 5V$, $I_D = 0.3A$
		2N6657		3.0		$V_{GS} = 10V$, $I_D = 1A$
		VN67AA		3.5		
$r_{DS(on)}$	Static Drain-Source ON-State Resistance[1]	All		5.0	Ω	$V_{GS} = 5V$, $I_D = 0.3A$
		2N6657		3.0		$V_{GS} = 10V$, $I_D = 1A$
		VN67AA		3.5		
$I_{D(on)}$	ON-State Drain Current[1]	All	1.5		A	$V_{DS} = 25V$, $V_{GS} = 10V$
Dynamic						
$r_{ds(on)}$	Small Signal Drain Source ON-State Resistance[1]	2N6657		3.0	Ω	$I_D = 1A$, $V_{GS} = 10V$, f = 1 kHz
g_{fs}	Forward Transconductance[1]	All	170		mS	$I_D = 0.5A$, $V_{DS} = 25V$
C_{iss}	Input Capacitance	All		50	pF	$V_{DS} = 25V$, $V_{GS} = 0$, f = 1 MHz
C_{rss}	Reverse Transfer Capacitance			10		
C_{oss}	Common Source Output Capacitance			40		
t_{ON}	Turn-ON Time	All		10*	ns	$V_{DD} = 25V$, $I_D \approx 1A$, $R_L = 23\Omega$, $R_g = 25\Omega$
t_{OFF}	Turn-OFF Time	All		10*		
Drain-Source Diode Characteristics						
			Typ			
V_{SD}	Forward ON Voltage[1]	All	−0.9		V	$I_S = -1A$, $V_{GS} = 0$
t_{rr}	Reverse Recovery Time	All	35		ns	$V_{GS} = 0$, $I_F = I_R = 1A$

*JEDEC Device meets $t_{d(on)}$, t_r, $t_{d(off)}$, t_f of 5 ns max each.

Refer to VNMA Design Curves (See Section 4)

Note:
1. Pulse test: 80-300 μs, 1% duty cycle.

TEST CIRCUITS

FIGURE 1. Switching Test Circuit

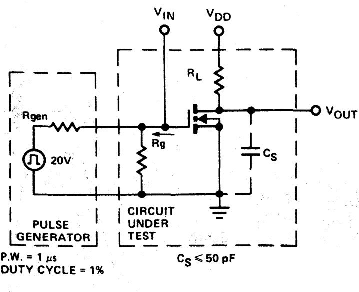
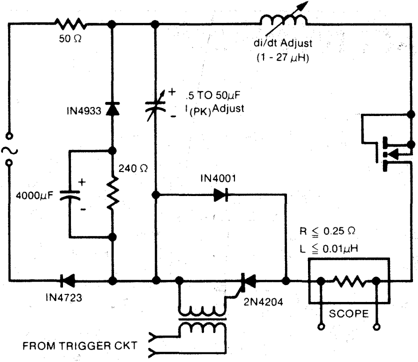


FIGURE 2. JEDEC Reverse Recovery Circuit



2N6660 ■ VN67AB

Siliconix

60V N-Channel Enhancement Mode MOSPOWER

These power FETs are designed especially for low power high frequency inverters, interface to CMOS and TTL logic, and line drivers.

FEATURES

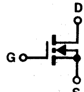
- High Input Impedance
- Extremely Fast Switching
- Rugged — Dissipation Limited SOA
- Internal Drain-Source Diode

BENEFITS

- Reduced Component Count
- Simpler Designs
  — Directly Interfaces CMOS & TTL
- Improved Circuit Performance
- Increased Reliability

Product Summary

Part Number	BV_{DSS} (Volts)	$R_{DS(ON)}$ (Ohms)	Package
2N6660	60	3	TO-39
VN67AB	60	3.5	TO-39



ABSOLUTE MAXIMUM RATINGS ($T_A = 25°C$ unless otherwise noted)

Drain-Source Voltage 60V

Drain-Gate Voltage 60V

Gate Current (Peak) . . . . ±1A

Gate-Source Voltage . . . . ± 40V

Drain Current
  Continuous[1]
    2N6660 . . . . ±1.1A
    VN67AB . . . . ±1A
  Pulsed[2] . . . . ±3A

Maximum Dissipation
  at 25°C Case 6.25W

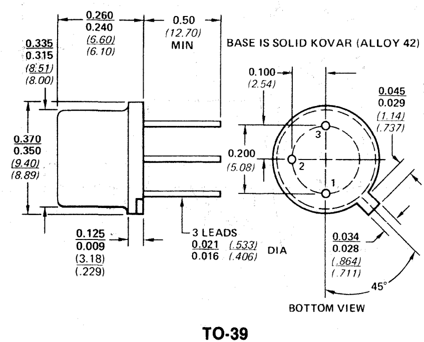
Linear Derating Factor . . . . 50mW/°C

Operating and Storage
  Temperature . . . . −55°C to +150°C

Lead Temperature
  (1/16" from Case for 10 secs) . . +300°C

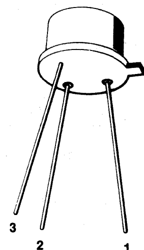
Notes:
1. Limited by package dissipation.
2. Pulse test — 80μs to 300μs, 1% duty cycle.

PACKAGE DIMENSIONS



TO-39

PIN 1 — Source
PIN 2 — Gate
PIN 3 & CASE — Drain



ELECTRICAL CHARACTERISTICS ($T_C = 25°C$ unless otherwise noted)

	Parameter	Part Number	Min	Max	Unit	Test Conditions
			Static			
BV_{DSS}	Drain-Source Breakdown	All	60		V	$V_{GS} = 0$, $I_D = 10\ \mu A$
$V_{GS(th)}$	Gate Threshold Voltage	All	0.8	2.0	V	$V_{DS} = V_{GS}$, $I_D = 1$ mA
I_{GSS}	Gate-Body Leakage	All		100	nA	$V_{GS} = 15V$, $V_{DS} = 0$
				500		$V_{GS} = 15V$, $V_{DS} = 0$, $T_A = 125°C$
I_{DSS}	Zero Gate Voltage Drain Current	All		10	μA	V_{DS} = Max Ratings, $V_{GS} = 0$
		All		500		V_{DS} = 0.8 Max Ratings, $V_{GS} = 0$, $T_A = 125°C$
$V_{DS(on)}$	Drain-Source Saturation Voltage[1]	All		1.5	V	$V_{GS} = 5V$, $I_D = 0.3A$
		2N6660		3.0		$V_{GS} = 10V$, $I_D = 1A$
		VN67AB		3.5		
$r_{DS(on)}$	Static Drain-Source ON-State Resistance[1]	All		5.0	Ω	$V_{GS} = 5V$, $I_D = 0.3A$
		2N6660		3.0		$V_{GS} = 10V$, $I_D = 1A$
		VN67AB		3.5		
$I_{D(on)}$	ON-State Drain Current[1]	All	1.5		A	$V_{DS} = 25V$, $V_{GS} = 10V$
			Dynamic			
$r_{ds(on)}$	Small Signal Drain Source ON-State Resistance	2N6660		3	Ω	$V_{GS} = 10V$, $I_D = 1A$, f = 1 kHz
g_{fs}	Forward Transconductance[1]	All	170		mS	$V_{DS} = 25V$, $I_D = 0.5A$
C_{iss}	Input Capacitance	All		50	pF	$V_{DS} = 25V$, $V_{GS} = 0$, f = 1 MHz
C_{rss}	Reverse Transfer Capacitance			10		
C_{oss}	Common Source Output Capacitance			40		
t_{ON}	Turn-ON Time	All		10*	ns	$V_{DD} = 25V$, $I_D \approx 1A$, $R_L = 23Ω$, $R_g = 25Ω$
t_{OFF}	Turn-OFF Time			10*		
			Drain-Source Diode Characteristics			
			Typ			
V_{SD}	Forward ON Voltage[1]	All	−0.9		V	$I_S = -1A$, $V_{GS} = 0$
t_{rr}	Reverse Recovery Time	All	35		ns	$V_{GS} = 0$, $I_F = I_R = 1A$

*JEDEC Device meets $t_{d(on)}$, t_r, $t_{d(off)}$, t_f of 5 ns max each.

Refer to VNMA Design Curves (See Section 4)

Note:
1. Pulse test 80–300 μs, 1% duty cycle.

TEST CIRCUITS

FIGURE 1. Switching Test Circuit

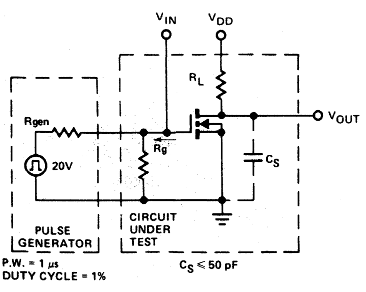
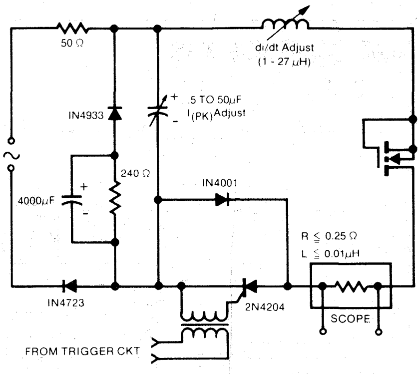


FIGURE 2. JEDEC Reverse Recovery Circuit



VN80AF ■ VN88AF ■ VN89AF

Siliconix

80V N-Channel Enhancement Mode MOSPOWER

These power FETs are designed especially for low power high frequency inverters, interface to CMOS and TTL logic, and line drivers.

FEATURES

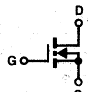
- **High Input Impedance**
- **Extremely Fast Switching**
- **Rugged—Dissipation Limited SOA**
- **Internal Drain-Source Diode**
- **High Free Air Power Dissipation**

BENEFITS

- **Reduced Component Count**
- **Simpler Designs**
  - **Directly Interfaces CMOS & TTL**
- **Improved Circuit Performance**
- **Increased Reliability**

Product Summary

Part Number	BV_{DSS} (Volts)	$R_{DS(ON)}$ (Ohms)	Package
VN80AF	80	5.0	TO-202
VN88AF	80	4.0	TO-202
VN89AF	80	4.5	TO-202



ABSOLUTE MAXIMUM RATINGS ($T_A = 25°C$ unless otherwise noted)

Drain-Source Voltage 80V

Drain-Gate Voltage 80V

Gate Current (Peak) . . . . ±1A

Gate-Source Voltage . . . . ± 40V

Drain Current

Continuous[1]

VN80AF . . . . ±1.3A

VN88AF . . . . ±1.5A

VN89AF . . . . ±1.4A

Pulsed[2] . . . . ±3A

Maximum Dissipation at 25°C Case . . 15W

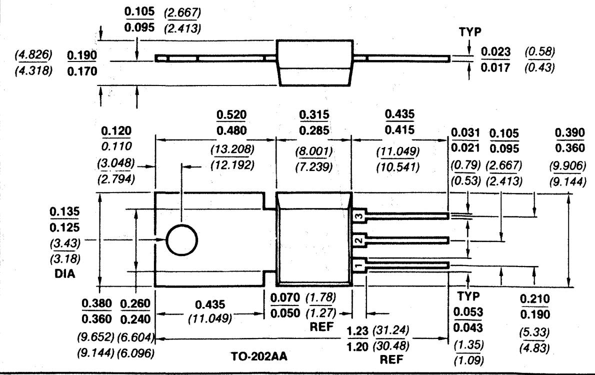
Linear Derating Factor . . . . 120 mW/°C

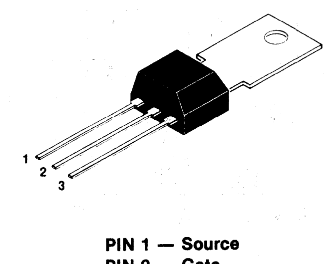
Operating and Storage Temperature . . . . −55°C to +150°C

Lead Temperature (1/16" from Case for 10 secs) . . +300°C

Notes:
1. Limited by package dissipation.
2. Pulse test—80μs to 300μs, 1% duty cycle.

PACKAGE DIMENSIONS





PIN 1 — Source
PIN 2 — Gate
PIN 3 & TAB — Drain

ELECTRICAL CHARACTERISTICS ($T_C = 25°C$ unless otherwise noted)

Parameter		Part Number	Min	Max	Unit	Test Conditions
Static						
BV_{DSS}	Drain-Source Breakdown	All	80		V	$V_{GS} = 0$, $I_D = 10\ \mu A$
$V_{GS(th)}$	Gate Threshold Voltage	All	0.8	2.5	V	$V_{DS} = V_{GS}$, $I_D = 1$ mA
I_{GSS}	Gate-Body Leakage	All		100	nA	$V_{GS} = 10V$, $V_{DS} = 0$
I_{DSS}	Zero Gate Voltage Drain Current	All		10	μA	V_{DS} = Max Ratings, $V_{GS} = 0$
				500		V_{DS} = 0.8 Max Ratings, $V_{GS} = 0$, $T_A = 125°C$
$V_{DS(on)}$	Drain-Source Saturation Voltage[1]	All		1.7	V	$V_{GS} = 5V$, $I_D = 0.3A$
		VN80AF		5.0		$V_{GS} = 10V$, $I_D = 1A$
		VN88AF		4.0		
		VN89AF		4.5		
$r_{DS(on)}$	Static Drain-Source ON-State Resistance[1]	All		5.6	Ω	$V_{GS} = 5V$, $I_D = 0.3A$
		VN80AF		5.0		$V_{GS} = 10V$, $I_D = 1A$
		VN88AF		4.0		
		VN89AF		4.5		
$I_{D(on)}$	ON-State Drain Current[1]	All	1.5		A	$V_{DS} = 25V$, $V_{GS} = 10V$
Dynamic						
g_{fs}	Forward Transconductance[1]	All	170		mS	$V_{DS} = 25V$, $I_D = 0.5A$
C_{iss}	Input Capacitance	All		50	pF	$V_{DS} = 25V$, $V_{GS} = 0$, f = 1 MHz
C_{rss}	Reverse Transfer Capacitance	All		10		
C_{oss}	Common Source Output Capacitance	All		50		
t_{ON}	Turn-ON Time	All		10	ns	$V_{DD} = 25V$, $I_D \approx 1A$, $R_L = 23Ω$, $R_g = 25Ω$
t_{OFF}	Turn-OFF Time	All		10		
Drain-Source Diode Characteristics						
			Typ			
V_{SD}	Forward ON Voltage[1]	All	−0.9		V	$I_S = -1A$, $V_{GS} = 0$
t_{rr}	Reverse Recovery Time	All	35		ns	$V_{GS} = 0$, $I_F = I_R = 1.0A$

Note:
1. Pulse test: 80–300 μs, 1% duty cycle.

Refer to VNMA Design Curves (See Section 4)

TEST CIRCUITS

FIGURE 1. Switching Test Circuit

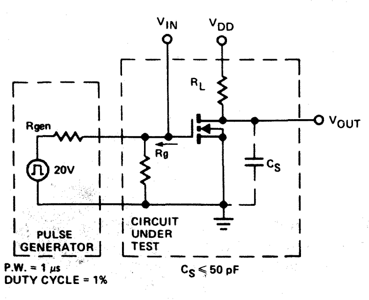
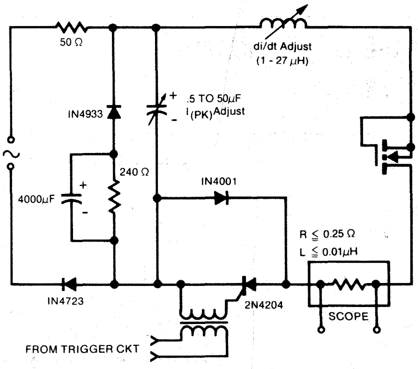


FIGURE 2. JEDEC Reverse Recovery Circuit



VN88AD ■ VN89AD

80V N-Channel Enhancement Mode MOSPOWER

These power FETs are designed especially for low power high frequency inverters, interface to CMOS and TTL logic, and line drivers.

FEATURES

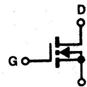
- High Input Impedance
- Extremely Fast Switching
- Rugged—Dissipation Limited SOA
- Internal Drain-Source Diode

Product Summary

Part Number	PRO ELECTRON Part Number	BV_{DSS} (Volts)	$R_{DS(on)}$ (Ohms)	Package
VN88AD	BSR82	80	4	TO-220
VN89AD		80	4.5	TO-220

BENEFITS

- Reduced Component Count
- Simpler Designs
  — Directly Interfaces CMOS & TTL
- Improved Circuit Performance
- Increased Reliability



ABSOLUTE MAXIMUM RATINGS ($T_A = 25°C$ unless otherwise noted)

Drain-Source Voltage 80V

Drain-Gate Voltage 80V

Gate Current (Peak) . . . . ±1A

Gate-Source Voltage . . . . ± 40V

Drain Current
  Continuous[1]
    VN88AD . . . . ±1.7A
    VN89AD . . . . ±1.6A
  Pulsed[2] . . . . ±3A

Maximum Dissipation at 25°C Case . . 20W

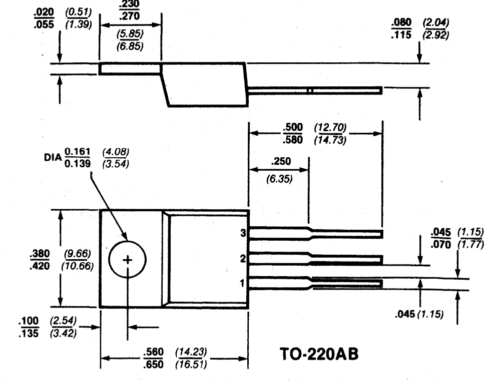
Linear Derating Factor . . . . 0.16W/°C

Operating and Storage
  Temperature . . . . −55°C to +150°C

Lead Temperature
  (1/16" from Case for 10 secs) . . +300°C

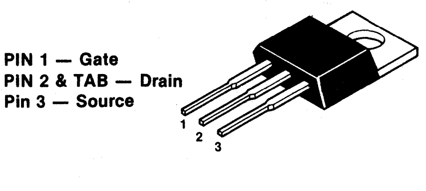
Notes:
1. Limited by package dissipation.
2. Pulse test—80μs to 300μs, 1% duty cycle.

PACKAGE DIMENSIONS



TO-220AB

PIN 1 — Gate
PIN 2 & TAB — Drain
Pin 3 — Source



ELECTRICAL CHARACTERISTICS ($T_C = 25°C$ unless otherwise noted)

	Parameter	Part Number	Min	Max	Unit	Test Conditions
Static						
BV_{DSS}	Drain-Source Breakdown	All	80		V	$V_{GS} = 0$, $I_D = 10\mu A$
$V_{GS(th)}$	Gate Threshold Voltage	All	0.8	2.5	V	$V_{DS} = V_{GS}$, $I_D = 1mA$
I_{GSS}	Gate Body Leakage	All		100	nA	$V_{GS} = 15V$, $V_{DS} = 0$
I_{DSS}	Zero Gate Voltage Drain Current	All		10	μA	V_{DS} = Max Ratings, $V_{GS} = 0$
		All		500	μA	V_{DS} = 0.8 Max Ratings, $V_{GS} = 0$, $T_A = 125°C$
$V_{DS(on)}$	Drain-Source Saturation Voltage[1]	All		1.5	V	$V_{GS} = 5V$, $I_D = 300mA$
		VN88AD		4.0	V	$V_{GS} = 10V$, $I_D = 1mA$
		VN89AD		4.5	V	$V_{GS} = 10V$, $I_D = 1mA$
$r_{DS(on)}$	Drain-Source On Resistance[1]	All		5.0	Ω	$V_{GS} = 5V$, $I_D = 300mA$
		VN88AD		4.0	Ω	$V_{GS} = 10V$, $I_D = 1A$
		VN89AD		4.5	Ω	$V_{GS} = 10V$, $I_D = 1A$
$I_{D(on)}$	On-State Drain Current[1]	All	1.5		A	$V_{DS} = 25V$, $V_{GS} = 10V$
Dynamic						
g_{fs}	Forward Transconductance[1]	All	170		mS	$V_{DS} = 25V$, $I_D = 0.5A$
C_{iss}	Input Capacitance	All		50	pF	$V_{DS} = 25V$, $V_{GS} = 0$, $f = 1MHz$
C_{rss}	Reverse Transfer Capacitance	All		10	pF	$V_{DS} = 25V$, $V_{GS} = 0$, $f = 1MHz$
C_{oss}	Common-Source Output Capacitance	All		50	pF	$V_{DS} = 25V$, $V_{GS} = 0$, $f = 1MHz$
t_{ON}	Turn-ON Time	All		10	ns	$V_{DD} = 25V$, $I_D \approx 1A$, $R_L = 23\Omega$, $R_g = 25\Omega$
t_{OFF}	Turn-OFF Time	All		10	ns	$V_{DD} = 25V$, $I_D \approx 1A$, $R_L = 23\Omega$, $R_g = 25\Omega$
Drain-Source Diode Characteristics						
			Typ			
V_{SD}	Forward ON Voltage[1]	All	−0.9		V	$I_S = -1A$, $V_{GS} = 0$
t_{rr}	Reverse Recovery Time	All	35		ns	$V_{GS} = 0$, $I_F = I_R = 1A$

Note 1: Pulse test — 80μs to 300μs, 1% duty cycle

Refer to VNMA Design Curves (See Section 4)

TEST CIRCUITS

FIGURE 1. Switching Test Circuit

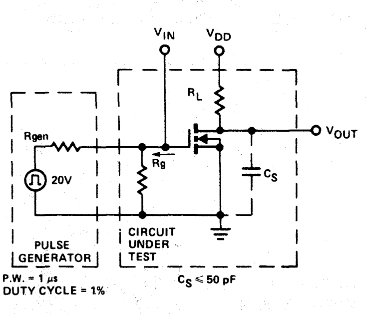
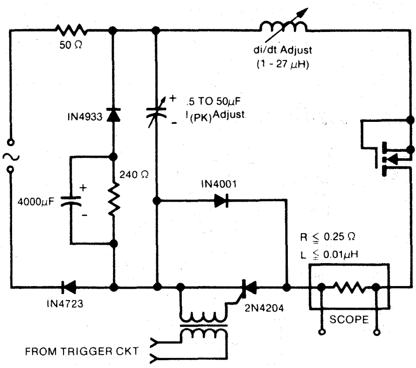


FIGURE 2. JEDEC Reverse Recovery Circuit



2N6658 ■ VN99AA ■ VN90AA

90V N-Channel Enhancement Mode MOSPOWER

Siliconix

These power FETs are designed especially for low power high frequency inverters, interface to CMOS and TTL logic, and line drivers.

FEATURES

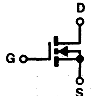
- **High Input Impedance**
- **Extremely Fast Switching**
- **Rugged—Dissipation Limited SOA**
- **Internal Drain-Source Diode**

BENEFITS

- **Reduced Component Count**
- **Simpler Designs**
  - **— Directly Interfaces CMOS & TTL**
- **Improved Circuit Performance**
- **Increased Reliability**

Product Summary

Part Number	BV_{DSS} (Volts)	$R_{DS(ON)}$ (Ohms)	Package
2N6658	90	4.0	TO-3
VN99AA	90	4.5	TO-3
VN90AA	90	5.0	TO-3



ABSOLUTE MAXIMUM RATINGS ($T_A = 25°C$ unless otherwise noted)

Drain-Source Voltage 90V

Drain-Gate Voltage 90V

Gate Current (Peak) . . . . ±1A

Gate-Source Voltage . . . . ± 40V

Drain Current
  Continuous[1]
    2N6658 . . . . ±1.9A
    VN99AA . . . . ±1.8A
    VN90AA . . . . ±1.7A
  Pulsed[2] . . . . ±3A

Maximum Dissipation at 25°C Case . . 25W

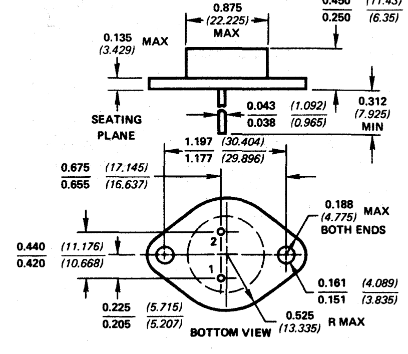
Linear Derating Factor . . . . 200 mW/°C

Operating and Storage
  Temperature . . . . −55°C to +150°C

Lead Temperature
  (1/16" from Case for 10 secs) . . +300°C

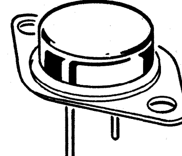
Notes:
1. Limited by package dissipation.
2. Pulse test—80μs to 300μs, 1% duty cycle.

PACKAGE DIMENSIONS



TO-3

PIN 1 — Gate
PIN 2 — Source
CASE — Drain



ELECTRICAL CHARACTERISTICS ($T_C = 25°C$ unless otherwise noted)

Parameter		Part Number	Min	Max	Unit	Test Conditions
Static						
BV_{DSS}	Drain-Source Breakdown	All	90		V	$V_{GS} = 0$, $I_D = 10\ \mu A$
$V_{GS(th)}$	Gate Threshold Voltage	All	0.8	2.0	V	$V_{DS} = V_{GS}$, $I_D = 1$ mA
I_{GSS}	Gate-Body Leakage	All		100	nA	$V_{GS} = 15V$, $V_{DS} = 0$
				500		$V_{GS} = 15V$, $V_{DS} = 0$, $T_A = 125°C$
I_{DSS}	Zero Gate Voltage Drain Current	All		10	μA	V_{DS} = Max Ratings, $V_{GS} = 0$
				500		V_{DS} = 0.8 Max Ratings, $V_{GS} = 0$, $T_A = 125°C$
$V_{DS(on)}$	Drain-Source Saturation Voltage[1]	All		1.6	V	$V_{GS} = 5V$, $I_D = 0.3A$
		2N6658		4.0		$V_{GS} = 10V$, $I_D = 1A$
		VN90AA		5.0		
		VN99AA		4.5		
$r_{DS(on)}$	Static Drain-Source ON-State Resistance[1]	All		5.3	Ω	$V_{GS} = 5V$, $I_D = 0.3A$
		2N6658		4.0		$V_{GS} = 10V$, $I_D = 1A$
		VN90AA		5.0		
		VN99AA		4.5		
$I_{D(on)}$	ON-State Drain Current[1]	All	1.5		A	$V_{DS} = 25V$, $V_{GS} = 10V$
Dynamic						
$r_{ds(on)}$	Small Signal Drain Source ON-State Resistance[1]	2N6658		4	Ω	$I_D = 1A$, $V_{GS} = 10V$, f = 1 kHz
g_{fs}	Forward Transconductance[1]	All	170		mS	$V_{DS} = 25V$, $I_D = 0.5A$
C_{iss}	Input Capacitance	All		50	pF	$V_{DS} = 25V$, $V_{GS} = 0$, f = 1 MHz
C_{rss}	Reverse Transfer Capacitance			10		
C_{oss}	Common Source Output Capacitance			40		
t_{ON}	Turn-ON Time	All		10*	ns	$V_{DD} = 25V$, $I_D \approx 1A$, $R_L = 23\Omega$, $R_g = 25\Omega$
t_{OFF}	Turn-OFF Time			10*		
Drain-Source Diode Characteristics						
			Typ			
V_{SD}	Forward ON Voltage[1]	All	−0.9		V	$I_S = -1A$, $V_{GS} = 0$
t_{rr}	Reverse Recovery Time	All	35		ns	$V_{GS} = 0$, $I_F = I_R = 1A$

*JEDEC Device meets $t_{d(on)}$, t_r, $t_{d(off)}$, t_f of 5 ns max each.

Note:
1. Pulse test 80–300 μs, 1% duty cycle.

Refer to VNMA Design Curves (See Section 4)

TEST CIRCUITS

FIGURE 1. Switching Test Circuit

FIGURE 2. JEDEC Reverse Recovery Circuit

2N6661 ■ VN99AB ■ VN90AB

90V N-Channel Enhancement Mode MOSPOWER

These power FETs are designed especially for low power high frequency inverters, interface to CMOS and TTL logic, and line drivers.

FEATURES

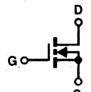
- High Input Impedance
- Extremely Fast Switching
- Rugged—Dissipation Limited SOA
- Internal Drain-Source Diode

BENEFITS

- Reduced Component Count
- Simpler Designs
  — Directly Interfaces CMOS & TTL
- Improved Circuit Performance
- Increased Reliability

Product Summary

Part Number	BV_{DSS} (Volts)	$R_{DS(ON)}$ (Ohms)	Package
2N6661	90	4	TO-39
VN99AB	90	4.5	TO-39
VN90AB	90	5.0	TO-39



ABSOLUTE MAXIMUM RATINGS ($T_A = 25°C$ unless otherwise noted)

Drain-Source Voltage 90V

Drain-Gate Voltage 90V

Gate Current (Peak) . . . . ±1A

Gate-Source Voltage . . . . ± 40V

Drain Current
- Continuous[1]
  - 2N6661 . . . . ±0.9A
  - VN99AB . . . . ±0.9A
  - VN90AB . . . . ±0.8A
- Pulsed[2] . . . . ±3A

Maximum Dissipation at 25°C 6.25W

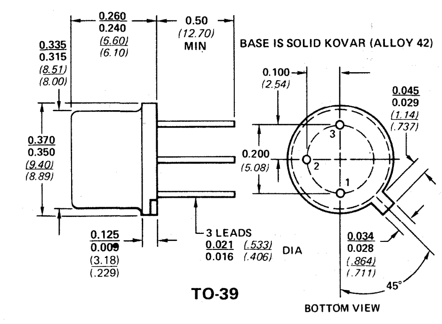
Linear Derating Factor . . . . 50 mW/°C

Operating and Storage Temperature . . . . −55°C to +150°C

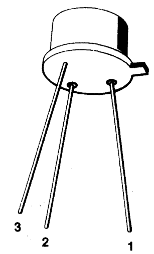
Lead Temperature (1/16" from Case for 10 secs) . . +300°C

Notes:
1. Limited by package dissipation.
2. Pulse test—80μs to 300μs, 1% duty cycle.

PACKAGE DIMENSIONS



PIN 1 — Source
PIN 2 — Gate
PIN 3 & CASE — Drain



ELECTRICAL CHARACTERISTICS ($T_C = 25°C$ unless otherwise noted)

Symbol	Parameter	Part Number	Min	Max	Unit	Test Conditions
			Static			
BV_{DSS}	Drain-Source Breakdown	All	90		V	$V_{GS} = 0$, $I_D = 10\ \mu A$
$V_{GS(th)}$	Gate Threshold Voltage	All	0.8	2.0	V	$V_{GS} = V_{DS}$, $I_D = 1$ mA
I_{GSS}	Gate-Body Leakage	All		0.1	μA	$V_{GS} = 15V$, $V_{DS} = 0$
				0.5		$V_{GS} = 15V$, $V_{DS} = 0$, $T_A = 125°C$
I_{DSS}	Zero Gate Voltage Drain Voltage	All		10	μA	V_{DS} = Max Ratings, $V_{GS} = 0$
				500		V_{DS} = 0.8V Max Ratings, $V_{GS} = 0$, $T_A = 125°C$
$V_{DS(on)}$	Drain-Source Saturation Voltage[1]	All		1.6	V	$V_{GS} = 5V$, $I_D = 0.3A$
		2N6661		4		$V_{GS} = 10V$, $I_D = 1A$
$r_{DS(on)}$	Static-Drain-Source ON-State Resistance[1]	All		5.3	Ω	$V_{GS} = 5V$, $I_D = 0.3A$
		2N6661		4.0		$V_{GS} = 10V$, $I_D = 1A$
		VN90AB		5.0		
		VN99AB		4.5		
$I_{D(on)}$	ON-State Drain Current[1]	All	1.5		A	$V_{DS} = 25V$, $V_{GS} = 10V$
			Dynamic			
$r_{ds(on)}$	Small Signal Drain-Source ON-State Resistance[1]	2N6661		4	Ω	$I_D = 1A$, $V_{GS} = 10V$, f = 1 kHz
g_{fs}	Forward Transconductance[1]	All	170		mS	$V_{DS} = 25V$, $I_D = 0.5A$
C_{iss}	Input Capacitance	All		50	pF	$V_{DS} = 25V$, $V_{GS} = 0$, f = 1 MHz
C_{rss}	Reverse Transfer Capacitance			10		
C_{oss}	Common Source Output Capacitance			40		
t_{ON}	Turn-ON Time	All		10*	ns	$V_{DD} = 25V$, $I_D \approx 1A$, $R_L = 23Ω$, $R_g = 25Ω$
t_{OFF}	Turn-OFF Time			10*		
			Drain-Source Diode Characteristics			
			Typ			
V_{SD}	Forward ON Voltage[1]	All	−0.9		V	$I_S = -1A$, $V_{GS} = 0$
t_{rr}	Reverse Recovery Time	All	35		ns	$V_{GS} = 0$, $I_F = I_R = 1A$

*JEDEC Device meets $t_{d(on)}$, t_r, $t_{d(off)}$, t_f of 5 ns max each.

Note:
1. Pulse test 80–300 μs, 1% duty cycle.

Refer to VNMA Design Curves (See Section 4)

TEST CIRCUITS

FIGURE 1. Switching Test Circuit

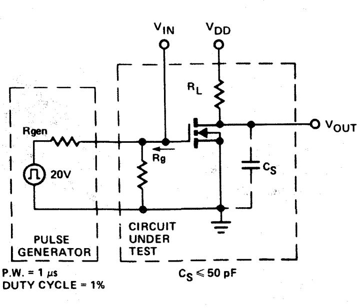
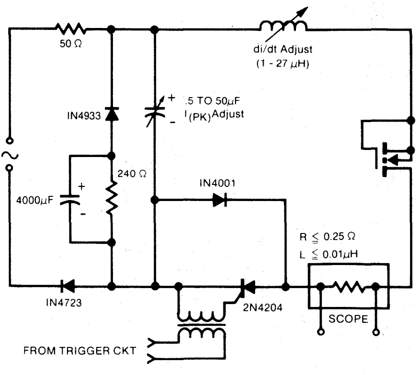


FIGURE 2. JEDEC Reverse Recovery Circuit



VN0300D

Siliconix

30V N-Channel Enhancement Mode MOSPOWER

This power FET is designed especially for low power high frequency inverters, interface to CMOS and TTL logic, and line drivers.

FEATURES

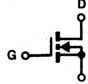
- High Input Impedance
- Extremely Fast Switching
- Rugged—Dissipation Limited SOA
- Internal Drain-Source Diode

BENEFITS

- Reduced Component Count
- Simpler Designs
  — Directly Interfaces CMOS & TTL
- Improved Circuit Performance
- Increased Reliability

Product Summary

Part Number	BV_{DSS} (Volts)	$R_{DS(ON)}$ (Ohms)	Package
VN0300D	30	1.2	TO-220



ABSOLUTE MAXIMUM RATINGS ($T_A = 25°C$ unless otherwise noted)

Drain-Source Voltage 30V

Drain-Gate Voltage 30V

Gate Current (Peak). . . . . ±0.5A

Gate-Source Voltage . . . . ±40V

Drain Current
  Continuous[1] . . . . ±2.5A
  Pulsed[2]. . . . . ±3A

Maximum Dissipation at 25°C Case . . 20W

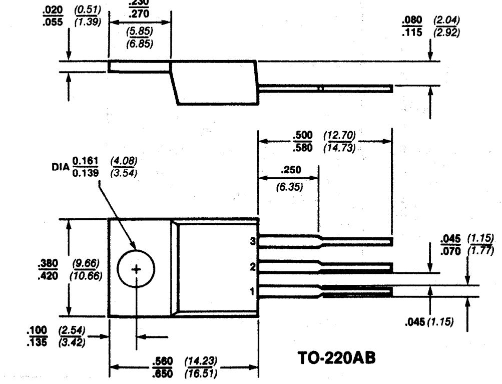
Linear Derating Factor. . . . . . .160 mW/°C

Operating and Storage
  Temperature. . . . .−55°C to +150°C

Lead Temperature
  (1/16" from Case for 10 secs) . . +300°C

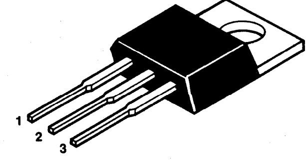
Notes:
1. Limited by package dissipation.
2. Pulse test—80μs to 300μs, 1% duty cycle.

PACKAGE DIMENSIONS



TO-220AB

PIN 1 — Gate
PIN 2 & TAB— Drain
PIN 3 — Source



ELECTRICAL CHARACTERISTICS (T_C=25°C unless otherwise noted)

Parameters		Min	Max	Unit	Test Conditions
Static					
BV_{DSS}	Drain-Source Breakdown	30		V	$V_{GS}=0$, $I_D=10\ \mu A$
$V_{GS(th)}$	Gate-Source Threshold Voltage	0.8	2.5	V	$V_{DS}=V_{GS}$, $I_D=1$ mA
I_{GSS}	Gate-Body Leakage		10	nA	$V_{GS}=15V$, $V_{DS}=0$
			100	nA	$V_{GS}=15V$, $V_{DS}=0$, $T_A=125°C$
I_{DSS}	Zero Gate Voltage Drain Current		10	μA	V_{DS} = Max Rating, $V_{GS}=0$
			500	μA	V_{DS} = Max Rating, $V_{GS}=0$, $T_A=125°C$
$V_{DS(on)}$	Drain-Source ON-State Saturation Voltage[1]		1.0	V	$V_{GS}=5V$, $I_D=300$ mA
			1.2	V	$V_{GS}=10V$, $I_D=1A$
$r_{DS(on)}$	Drain-Source ON-State Resistance[1]		3.3	Ω	$V_{GS}=5V$, $I_D=300$ mA
			1.2	Ω	$V_{GS}=10V$, $I_D=1A$
$I_{D(on)}$	ON-State Drain Current[1]	2.0		A	$V_{DS}=15V$, $V_{GS}=10V$
Dynamic					
g_{fs}	Forward Transconductance[1]	200		mS	$V_{DS}=15V$, $I_D=0.5A$
C_{iss}	Input Capacitance		100	pF	$V_{DS}=15V$, $V_{GS}=0$, f = 1 MHz
C_{rss}	Reverse Transfer Capacitance		80	pF	$V_{DS}=15V$, $V_{GS}=0$, f = 1 MHz
C_{oss}	Common-Source Output Capacitance		55	pF	$V_{DS}=15V$, $V_{GS}=0$, f = 1 MHz
t_{ON}	Turn-ON Time		30	ns	$V_{DD}=15V$, $I_D\approx0.6A$, $R_L=24\Omega$, $R_g=25\Omega$
t_{OFF}	Turn-OFF Time		30	ns	$V_{DD}=15V$, $I_D\approx0.6A$, $R_L=24\Omega$, $R_g=25\Omega$
Drain-Source Diode Characteristics					
		Typ			
V_{SD}	Forward ON Voltage[1]	−0.9		V	$I_S=-1A$, $V_{GS}=0$
t_{rr}	Reverse Recovery Time	90		ns	$V_{GS}=0$, $I_F=I_R=2A$

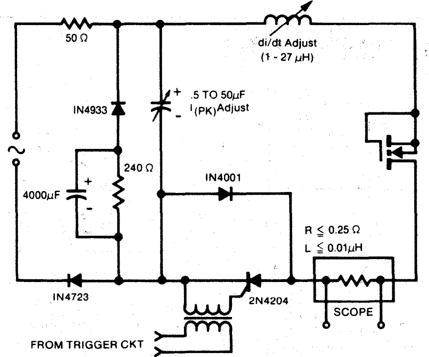
Note:
1. Pulse test 80-300 μs, 1% duty cycle.

Refer to VNMH03 Design Curves (See Section 4)

TEST CIRCUITS

FIGURE 1. Switching Test Circuit

FIGURE 2. JEDEC Reverse Recovery Circuit



VN0300M

Siliconix

30V N-Channel Enhancement Mode MOSPOWER

This power FET is designed especially for low power high frequency inverters, interface to CMOS and TTL logic, and line drivers.

FEATURES

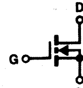
- High Input Impedance
- Extremely Fast Switching
- Rugged — Dissipation Limited SOA
- Internal Drain-Source Diode

Product Summary

Part Number	BV_{DSS} (Volts)	$R_{DS(ON)}$ (Ohms)	Package
VN0300M	30	1.2	TO-237

BENEFITS

- Reduced Component Count
- Simpler Designs
  — Directly Interfaces CMOS & TTL
- Improved Circuit Performance
- Increased Reliability



ABSOLUTE MAXIMUM RATINGS ($T_A = 25°C$ unless otherwise noted)

Drain-Source Voltage 30V

Drain-Gate Voltage 30V

Gate Current (Peak) . . . . ±1A

Gate-Source Voltage . . . . ±40V

Drain Current
  Continuous[1] . . . . ±0.7A
  Pulsed[2] . . . . ±3A

Maximum Dissipation at 25°C Case . . . 1W

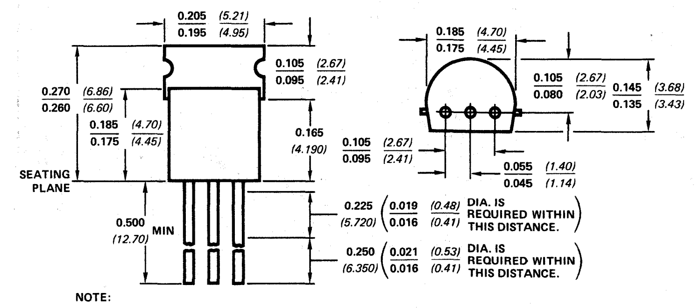
Linear Derating Factor . . . . 8 mW/°C

Operating and Storage
  Temperature . . . . −55°C to +150°C

Lead Temperature
  (1/16" from Case for 10 secs) . . +300°C

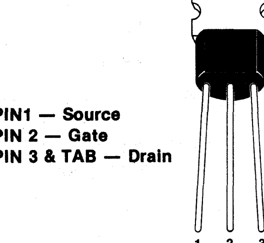
Notes:
1. Limited by package dissipation.
2. Pulse test—80μs to 300μs, 1% duty cycle.

PACKAGE DIMENSIONS



TO-237

PIN1 — Source
PIN 2 — Gate
PIN 3 & TAB — Drain



ELECTRICAL CHARACTERISTICS ($T_C = 25°C$ unless otherwise noted)

Symbol	Parameter	Min	Max	Unit	Test Conditions
	Static				
BV_{DSS}	Drain-Source Breakdown	30		V	$V_{GS} = 0$, $I_D = 10\ \mu A$
$V_{GS(th)}$	Gate-Source Threshold Voltage	0.8	2.5	V	$V_{DS} = V_{GS}$, $I_D = 1$ mA
I_{GSS}	Gate-Body Leakage		0.1	μA	$V_{GS} = 30V$, $V_{DS} = 0$
I_{DSS}	Zero Gate Voltage Drain Current		10	μA	V_{DS} = Max Rating, $V_{GS} = 0$
$V_{DS(on)}$	Drain Source ON-State Voltage[1]		1.0	V	$V_{GS} = 5V$, $I_D = 0.3A$
			1.2	V	$V_{GS} = 10V$, $I_D = 1A$
$r_{DS(on)}$	Drain-Source ON-State Resistance[1]		3.3	Ω	$V_{GS} = 5V$, $I_D = 0.3A$
			1.2	Ω	$V_{GS} = 10V$, $I_D = 1A$
$I_{D(on)}$	ON-State Drain Current[1]	1		A	$V_{DS} = 25V$, $V_{GS} = 10V$
	Dynamic				
g_{fs}	Forward Transconductance[1]	200		mS	$V_{DS} = 15V$, $I_D = 0.5A$
C_{iss}	Input Capacitance		100	pF	$V_{DS} = 15V$, $V_{GS} = 0$, f = 1 MHz
C_{rss}	Reverse Transfer Capacitance		80	pF	$V_{DS} = 15V$, $V_{GS} = 0$, f = 1 MHz
C_{oss}	Common Source Output Capacitance		55	pF	$V_{DS} = 15V$, $V_{GS} = 0$, f = 1 MHz
t_{ON}	Turn-ON Time		30	ns	$V_{DD} = 25V$, $I_D \approx 1A$, $R_L = 24\Omega$, $R_g = 25\Omega$
t_{OFF}	Turn-OFF Time		30	ns	$V_{DD} = 25V$, $I_D \approx 1A$, $R_L = 24\Omega$, $R_g = 25\Omega$
	Drain-Source Diode Characteristics				
		Typ			
V_{SD}	Forward ON Voltage[1]	−0.9		V	$I_S = -1A$, $V_{GS} = 0$
t_{rr}	Reverse Recovery Time	90		ns	$V_{GS} = 0$, $I_F = I_R = 2A$

Note:
1. Pulse test: 80–300 μs, 1% duty cycle.

Refer to VNMH03 Design Curves (See Section 4)

TEST CIRCUITS

FIGURE 1 Switching Test Circuit

P.W. = 1 μs
DUTY CYCLE = 1%
$C_S \leq 50$ pF

FIGURE 2 JEDEC Reverse Recovery Circuit

VN0600A,D ■ VN0601A,D
VN0400A,D ■ VN0401A,D

Siliconix

60V N-Channel Enhancement Mode MOSPOWER

This power FET is designed especially for switching regulators, converters, solenoid and relay drivers, and audio amplifiers.

FEATURES

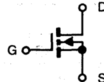
- **Low $r_{DS(on)}$**
- **No Second Breakdown**
- **High Input Impedance**
- **Internal Drain-Source Diode**
- **Very Rugged: Excellent SOA**
- **Extremely Fast Switching**

BENEFITS

- **Reduced Component Count**
- **Improved Performance**
- **Simpler Designs**
- **Improved Reliability**

Product Summary

Part Number	BV_{DSS}	$R_{DS(on)}$	I_D	Package
VN0600A	60V	0.12Ω	18A	TO-3
VN0400A	40V			
VN0601A	60V	0.15Ω	16A	
VN0401A	40V			
VN0600D	60V	0.12Ω	18A	TO-220AB
VN0400D	40V			
VN0601D	60V	0.15Ω	16A	
VN0401D	40V			



ABSOLUTE MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

Drain-Source Voltage
- VN0600A,D; VN0601A,D 60V
- VN0400A,D; VN0401A,D 40V

Drain-Gate Voltage
- VN0600A,D; VN0601A,D 60V
- VN0400A,D; VN0401A,D 40V

Drain Current Continuous
- VN0400A,D; VN0600A,D .... ±18A
- VN0401A,D; VN0601A,D .... ±16A

Drain Current
- Pulsed[1] .... ±60A

Gate Current (Peak) .... ±3A

Gate-Source Voltage .... ±40V

Power Dissipation
- TO-3 .... 100W
- TO-220AB 75W

Linear Derating Factor .... 0.60W/°C

Operating and Storage Temperature
- TO-3 .... −55°C to +175°C
- TO-220AB .... −55°C to +150°C

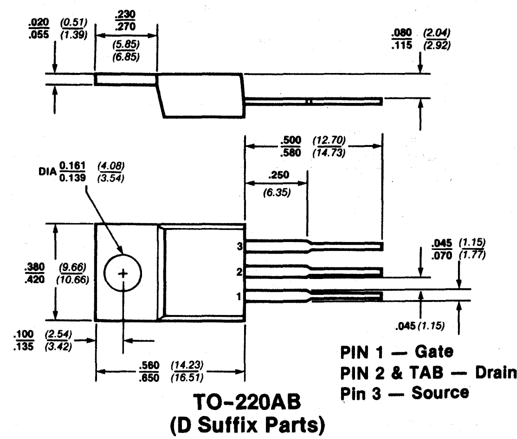
Note 1: Pulse test—80μs to 300μs, 1% duty cycle.

PACKAGE DIMENSIONS

PIN 1 — Gate
PIN 2 — Source
CASE — Drain

0.875 (22.225) MAX
0.135 (3.429) MAX
0.450 (11.43) / 0.250 (6.35)
SEATING PLANE
0.043 (1.092) / 0.038 (0.965)
0.312 (7.925) MIN
1.197 (30.404) / 1.177 (29.896)
0.675 (17.145) / 0.655 (16.637)
0.188 (4.775) MAX BOTH ENDS
0.440 (11.176) / 0.420 (10.668)
0.161 (4.089) / 0.151 (3.835)
0.225 (5.715) / 0.205 (5.207)
0.525 (13.335) R MAX
BOTTOM VIEW

TO-204AA (TO-3)
(A Suffix Parts)



TO-220AB
(D Suffix Parts)

PIN 1 — Gate
PIN 2 & TAB — Drain
Pin 3 — Source

ELECTRICAL CHARACTERISTICS ($T_C = 25°C$ unless otherwise noted)

Parameter		Part Number	Min	Max	Unit	Test Conditions
Static						
BV_{DSS}	Drain-Source Breakdown	VN0600A	60		V	$V_{GS} = 0$, $I_D = 1mA$
		VN0601A	60			
		VN0400A	40			
		VN0401A	40			
		VN0600D	60			
		VN0601D	60			
		VN0400D	40			
		VN0401D	40			
$V_{GS(th)}$	Gate Threshold Voltage	All	2	4.5	V	$V_{DS} = V_{GS}$, $I_D = 1mA$
I_{GSS}	Gate Body Leakage	All		100	nA	$V_{GS} = 30V$, $V_{DS} = 0$
I_{DSS}	Zero Gate Voltage Drain Current	All		1	mA	$V_{GS} = 0$, V_{DS} = Rated V_{DS}
				4		$V_{GS} = 0$, V_{DS} = Rated V_{DS}, $T_C = 150°C$
$V_{DS(on)}$	Drain-Source Saturation Voltage[1]	VN0600A,D		1.44	V	$V_{GS} = 10V$, $I_D = 12A$
		VN0400A,D				
		VN0601A,D		1.8		
		VN0401A,D				
$r_{DS(on)}$	Drain-Source On Resistance[1]	VN0600A,D		0.12	Ω	$V_{GS} = 10V$, $I_D = 12A$
		VN0400A,D				
		VN0601A,D		0.15		
		VN0401A,D				
$I_{D(on)}$	On-State Drain Current[1]	All	18		A	$V_{GS} = 10V$, $V_{DS} = 25V$
Dynamic						
g_{fs}	Forward Transconductance[1]	All	3		mS	$V_{DS} = 25V$, $I_D = 12A$ (Note 1)
C_{iss}	Input Capacitance	All		1200	pF	$V_{DS} = 25V$, $V_{GS} = 0$, $f = 1MHz$
C_{rss}	Reverse Transfer Capacitance	All		200		
C_{oss}	Common-Source Output Capacitance	All		500		
$t_{d(on)}$	Turn-on Time	All		30	ns	$V_{DD} = 30V$, $I_D \approx 12A$, $R_L = 2.4Ω$, $R_g = 10Ω$ (Figure 1)
t_r	Rise Time	All		150		
$t_{d(off)}$	Turn-off Time	All		100		
t_f	Fall Time	All		100		
Drain-Source Diode Characteristics						
			Typ			
V_{SD}	Forward ON Voltage[1]	All	−1.5		V	$I_S = -12A$, $V_{GS} = 0$
t_{rr}	Reverse Recovery Time	All	300		ns	$I_F = 40A$, $V_{GS} = 0$, $di/dt = 100 A/\mu S$ (Figure 2)

Note 1: Pulse test — 80μs to 300μs, 1% duty cycle

TEST CIRCUITS

FIGURE 1. Switching Test Circuit

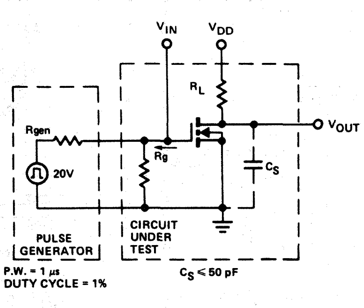
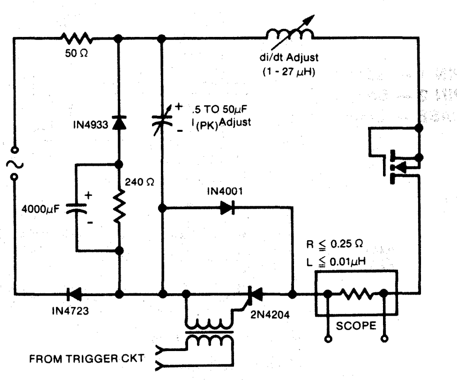


FIGURE 2. Reverse Recovery Test Circuit



VN0606M

Siliconix

60V N-Channel Enhancement Mode MOSPOWER

This power FET is designed especially for low power high frequency inverters, interface to CMOS and TTL logic, and line drivers.

FEATURES

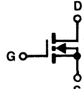
- High Input Impedance
- Extremely Fast Switching
- Rugged—Dissipation Limited SOA
- Internal Drain-Source Diode
- Low Cost Package

BENEFITS

- Reduced Component Count
- Simpler Designs
  — Directly Interfaces CMOS & TTL
- Improved Circuit Performance
- Increased Reliability

Product Summary

Part Number	PRO ELECTRON Part Number	BV_{DSS} (Volts)	$R_{DS(on)}$ (Ohms)	Package
VN0606M	BSR66	3	4	TO-237



ABSOLUTE MAXIMUM RATINGS ($T_A = 25°C$ unless otherwise noted)

Drain-Source Voltage 60V

Drain-Gate Voltage 60V

Gate Current (Peak) . . . . ±1A

Gate-Source Voltage . . . . ±40V

Drain Current
  Continuous[1] . . . . ±0.4A
  Pulsed[2] . . . . ±2A

Maximum Dissipation at 25°C Case . . . 1W

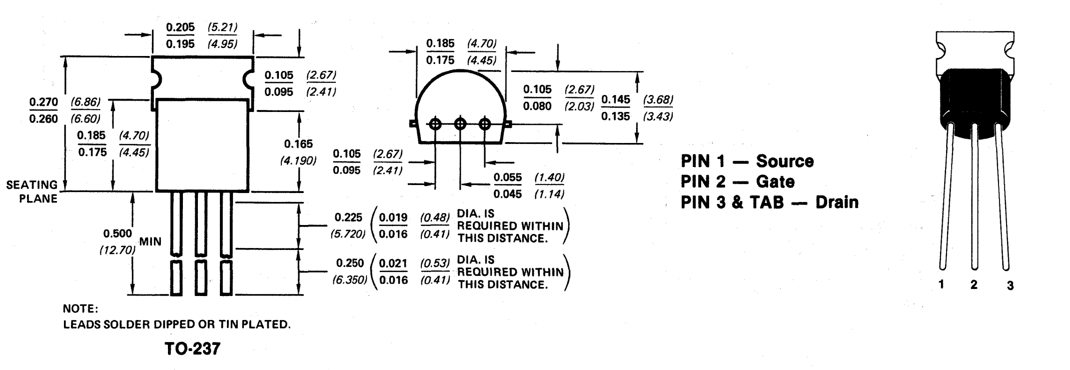
Linear Derating Factor . . . . 8 mW/°C

Operating and Storage
  Temperature . . . . −55°C to +150°C

Lead Temperature
  (1/16" from Case for 10 secs) . . +300°C

Notes:
1. Limited by package dissipation.
2. Pulse test—80μs to 300μs, 1% duty cycle.

PACKAGE DIMENSIONS



ELECTRICAL CHARACTERISTICS ($T_C = 25°C$ unless otherwise noted)

	Parameter	Min	Max	Unit	Test Conditions
	Static				
BV_{DSS}	Drain-Source Breakdown	60		V	$V_{GS} = 0$, $I_D = 10\ \mu A$
$V_{GS(th)}$	Gate Threshold Voltage	0.8	2.0	V	$V_{DS} = V_{GS}$, $I_D = 1$ mA
I_{GSS}	Gate Body Leakage		100	nA	$V_{GS} = 15V$, $V_{DS} = 0$
I_{DSS}	Zero Gate Voltage Drain Current		10	μA	V_{DS} = Max Ratings, $V_{GS} = 0$
$V_{DS(on)}$	Drain-Source Saturation Voltage[1]		3	V	$V_{GS} = 10V$, $I_D = 1A$
$r_{DS(on)}$	Drain-Source ON Resistance[1]		3	Ω	$V_{GS} = 10V$, $I_D = 1A$
$I_{D(on)}$	ON-State Drain Current[1]	1.5		A	$V_{DS} = 25V$, $V_{GS} = 10V$
	Dynamic				
g_{fs}	Forward Transconductance[1]	170		mS	$V_{DS} = 25V$, $I_D = 0.5A$
C_{iss}	Input Capacitance		50	pF	$V_{DS} = 25V$, $V_{GS} = 0$, f = 1 MHz
C_{rss}	Reverse Transfer Capacitance		10	pF	$V_{DS} = 25V$, $V_{GS} = 0$, f = 1 MHz
C_{oss}	Common-Source Output Capacitance		50	pF	$V_{DS} = 25V$, $V_{GS} = 0$, f = 1 MHz
t_{ON}	Turn-ON Time		10	ns	$V_{DD} = 25V$, $I_D \approx 1A$, $R_L = 23\Omega$, $R_g = 25\Omega$
t_{OFF}	Turn-OFF Time		10	ns	$V_{DD} = 25V$, $I_D \approx 1A$, $R_L = 23\Omega$, $R_g = 25\Omega$
	Drain-Source Diode Characteristics				
		Typ			
V_{SD}	Forward ON Voltage[1]	−0.9		V	$I_S = -1A$, $V_{GS} = 0$
t_{rr}	Reverse Recovery Time	35		ns	$V_{GS} = 0$, $I_F = I_R = 1A$

Note:
1. Pulse test 80–300 μs, 1% duty cycle.

Refer to VNMA Design Curves (See Section 4)

TEST CIRCUITS

FIGURE 1 Switching Test Circuit

FIGURE 2 JEDEC Reverse Recovery Circuit

VN0610L ■ VN2222L

Siliconix

60V N-Channel Enhancement Mode MOSPOWER

These power FETs are designed especially for low power high frequency inverters, interface to CMOS and TTL logic, and line drivers.

FEATURES

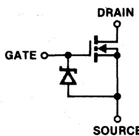
- High Input Impedance
- Extremely Fast Switching
- Rugged — Dissipation Limited SOA
- Internal Drain-Source Diode
- Lowest Cost Package

BENEFITS

- Reduced Component Count
- Simpler Designs
  — Directly Interfaces CMOS & TTL
- Improved Circuit Performance
- Increased Reliability

Product Summary

Part Number	BV_{DSS} (Volts)	$R_{DS(ON)}$ (Ohms)	Package
VN0610L	60	5.0	TO-92
VN2222L	60	7.5	TO-92



ABSOLUTE MAXIMUM RATINGS ($T_A = 25°C$ unless otherwise noted)

Drain-Source Voltage 60V

Drain-Gate Voltage 60V

Gate Current (Peak). . . . . ±400mA

Gate-Source Voltage . . . . . . + 15V, − 0.3V

Drain Current
  Continuous[1]
    VN0610L . . . . ±0.2A
    VN2222L . . . . ±0.15A
  Pulsed[2] . . . . ±1A

Maximum Dissipation
  at 25°C Case . . . . 400 mW

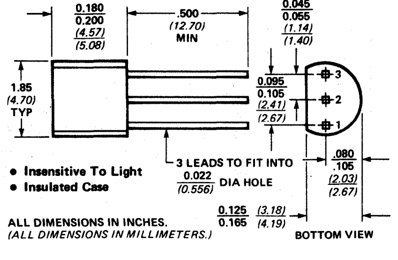
Linear Derating Factor . . . . 3.2 mW/°C

Operating and Storage
  Temperature . . . . −55°C to +150°C

Lead Temperature
  (1/16" from Case for 10 secs) . . +300°C

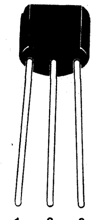
Notes:
1. Limited by package dissipation.
2. Pulse test — 80μs to 300μs, 1% duty cycle.

PACKAGE DIMENSIONS



TO-92

PIN 1 — Source
PIN 2 — Gate
PIN 3 — Drain



ELECTRICAL CHARACTERISTICS ($T_C = 25°C$ unless otherwise noted)

Parameter		Part Number	Min	Max	Unit	Test Conditions
Static						
BV_{DSS}	Drain-Source Breakdown	All	60		V	$V_{GS} = 0$, $I_D = 100\ \mu A$
$V_{GS(th)}$	Gate-Source Threshold Voltage	VN0610L	0.8	2.5	V	$V_{DS} = V_{GS}$, $I_D = 1$ mA
		VN2222L	0.6	2.5		
I_{GSS}	Gate-Body Leakage Current	All		100	nA	$V_{DS} = 0$, $V_{GS} = 15V$
I_{DSS}	Zero Gate Voltage Drain Current	All		10	μA	$V_{DS} = 50V$, $V_{GS} = 0$
$I_{D(on)}$	ON-State Drain Current[1]	All	0.75		A	$V_{GS} = 10V$, $V_{DS} = 15V$
$V_{DS(on)}$	Drain-Source ON-State Voltage[1]	All		1.5	V	$I_D = 200$ mA, $V_{GS} = 5V$
		VN0610L		2.5		$I_D = 500$ mA, $V_{GS} = 10V$
		VN2222L		3.75		
$r_{DS(on)}$	Drain-Source ON-State Resistance[1]	All		7.5	Ω	$I_D = 200$ mA, $V_{GS} = 5V$
		VN0610L		5.0		$I_D = 500$ mA, $V_{GS} = 10V$
		VN2222L		7.5		
Dynamic						
g_{fs}	Forward Transconductance[1]	All	100		mS	$I_D = 500$ mA, $V_{DS} = 15V$
C_{iss}	Input Capacitance	All		60	pF	$V_{DS} = 15V$, $V_{GS} = 0$, f = 1 MHz
C_{rss}	Reverse Transfer Capacitance	All		5.0		
C_{oss}	Common Source Output Capacitance	All		25		
t_{ON}	Turn-ON Time	All		10	ns	$V_{DD} = 15V$, $I_D \approx 0.6A$, $R_L = 23\Omega$, $R_g = 25\Omega$
t_{OFF}	Turn-OFF Time	All		10		
Drain-Source Diode Characteristics						
			Typ			
V_{SD}	Forward ON Voltage[1]	All	−0.85		V	$I_S = -0.5A$, $V_{GS} = 0$
t_{rr}	Reverse Recovery Time	All	160		ns	$V_{GS} = 0$, $I_F = I_R = 0.5A$

Note:
1. Pulse test: 80–300 μs, 1% duty cycle.

Refer to VNML ■ VNMK Design Curves (See Section 4)

TEST CIRCUITS

FIGURE 1. Switching Test Circuit

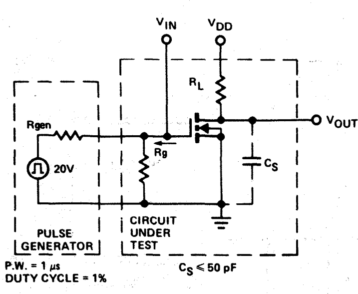
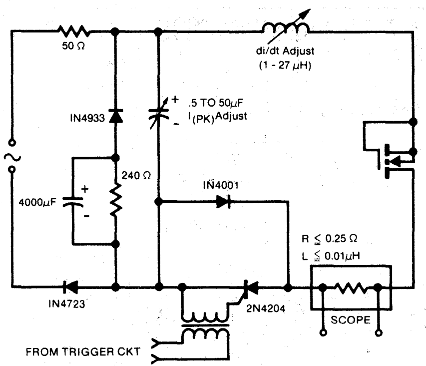


FIGURE 2. JEDEC Reverse Recovery Circuit



VN0800A ■ VN0801A ■ VN1000A ■ VN1001A
VN1200A ■ VN1201A
VN0800D ■ VN0801D ■ VN1000D ■ VN1001D
VN1200D ■ VN1201D

Siliconix

120V N-Channel Enhancement Mode MOSPOWER

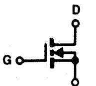
These power FETs are designed especially for audio amplifiers, power converters, and drivers for motors, solenoids and relays.

FEATURES

- No Second Breakdown
- High Input Impedance
- Internal Drain-Source Diode
- Very Rugged: Excellent SOA
- Extremely Fast Switching

BENEFITS

- Reduced Component Count
- Improved Performance
- Simpler Designs
- Improved Reliability



Product Summary

Part Number	BV_{DSS}	$R_{DS(on)}$	I_D	Package
VN0800A	80 V	0.18Ω	14 A	TO-3
VN0800D				TO-220
VN0801A		0.25Ω	12 A	TO-3
VN0801D				TO-220
VN1000A	100 V	0.18Ω	14 A	TO-3
VN1000D				TO-220
VN1001A		0.25Ω	12 A	TO-3
VM1001D				TO-220
VN1200A	120 V	0.18Ω	14 A	TO-3
VN1200D				TO-220
VN1201A		0.25Ω	12 A	TO-3
VN1201D				TO-220

ABSOLUTE MAXIMUM RATINGS ($T_C = 25°C$ unless otherwise noted)

Drain-Source Voltage
- VN0800A,D; VN0801A,D .... 80 V
- VN1000A,D; VN1001A,D .... 100 V
- VN1200A,D; VN1201A,D .... 120 V

Drain-Gate Voltage
- VN0800A,D; VN0801A,D .... 80 V
- VN1000A,D; VN1001A,D .... 100 V
- VN1200A,D; VN1201A,D .... 120 V

Drain Current Continuous
- VN0800A,D; VN1000A,D; VN1200A,D .... ±14 A
- VN0801A,D; VN1001A,D; VN1201A,D .... ±12 A

Drain Current
- Pulsed (80μs to 300μs, 1% duty cycle) .... ±56 A

Gate Current (Peak) .... ±3 A

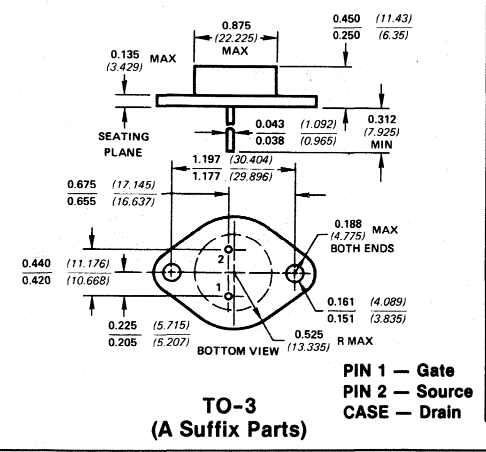
Gate-Source Voltage .... ±40 V

Power Dissipation
- TO-3 .... 100 W
- TO-220AB .... 75 W

Linear Derating Factor .... 0.60W/°C

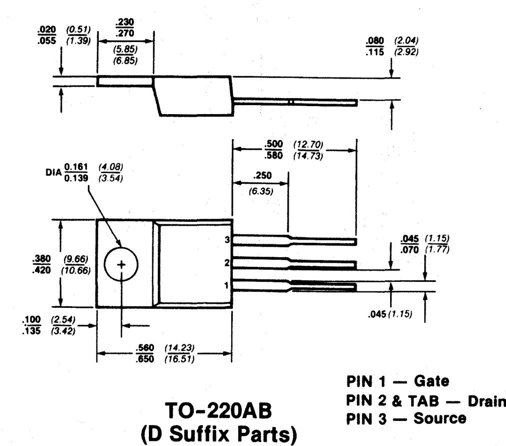
Operating and Storage Temperature
- TO-3 .... −55°C to +175°C
- TO-220AB .... −55°C to +150°C

PACKAGE DIMENSIONS



PIN 1 — Gate
PIN 2 — Source
CASE — Drain

TO-3
(A Suffix Parts)



TO-220AB
(D Suffix Parts)

PIN 1 — Gate
PIN 2 & TAB — Drain
PIN 3 — Source

ELECTRICAL CHARACTERISTICS ($T_C = 25°C$ unless otherwise noted)

Symbol	Parameter	Part Number	Min	Max	Unit	Test Conditions
	Static					
BV_{DSS}	Drain-Source Breakdown Voltage	VN0800A,D VN0801A,D	80		V	$V_{GS} = 0$, $I_D = 1$ mA
		VN1000A,D VN1001A,D	100			
		VN1200A,D VN1201A,D	120			
$V_{GS(th)}$	Gate Threshold Voltage	All	2.0	4.5	V	$V_{GS} = V_{DS}$, $I_D = 1$ mA
I_{GSS}	Gate-Body Leakage	All		100	nA	$V_{GS} = 30V$, $V_{DS} = 0$
I_{DSS}	Zero Gate Voltage Drain Current	All		1.0	mA	V_{DS} = Rated V_{DS}, $V_{GS} = 0$
				4.0		V_{DS} = Rated V_{DS}, $V_{GS} = 0$, $T_C = 150°C$
$V_{DS(on)}$	Drain-Source ON-State Voltage[1]	VN0800A,D VN1000A,D VN1200A,D		2.16	V	$V_{GS} = 10V$, $I_D = 12A$
		VN0801A,D VN1001A,D VN1201A,D		3.0		
$r_{DS(on)}$	Drain-Source On Resistance[1]	VN0800A,D VN1000A,D VN1200A,D		0.18	Ω	$V_{GS} = 10V$, $I_D = 12A$
		VN0801A,D VN1001A,D VN1201A,D		0.25		
$I_{D(on)}$	On-State Drain Current[1]	All	14		A	$V_{DS} = 25V$, $V_{GS} = 10V$
	Dynamic					
g_{fs}	Forward Transconductance[1]	All	3.0		S	$V_{DS} = 25V$, $I_D = 6A$
C_{iss}	Input Capacitance	All		1200	pF	$V_{GS} = 0$, $V_{DS} = 25V$, f = 1 MHz
C_{rss}	Reverse Transfer Capacitance	All		200		
C_{oss}	Output Capacitance	All		600		
$t_{d(on)}$	Turn-On Delay Time	All		30	ns	$V_{DD} = 60V$, $I_D \approx 12A$, $R_L = 5Ω$, $R_g = 10Ω$ (Figure 1)
t_r	Rise Time	All		150		
$t_{d(off)}$	Turn-Off Delay Time	All		100		
t_f	Fall Time	All		100		

Drain-Source Diode Characteristics

Symbol	Parameter	Typ	Unit	Test Conditions
V_{SD}	Forward On Voltage[1]	−1.5	V	$I_S = -30A$, $V_{GS} = 0$
t_{rr}	Reverse Recovery Time	300	ns	$I_F = 30A$, $V_{GS} = 0$, di/dt = 100A/μs (Figure 2)

Note 1: Pulse test — 80 μs to 300 μs, 1% duty cycle

Refer to VNDA12 Design Curves (See Section 4)

TEST CIRCUITS

FIGURE 1 Switching Test Circuit

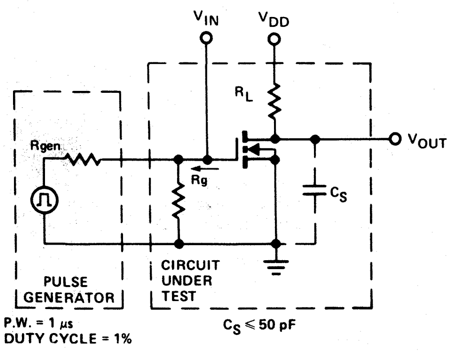
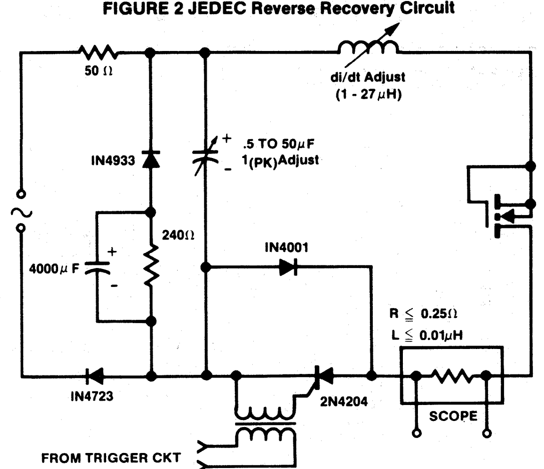


FIGURE 2 JEDEC Reverse Recovery Circuit



VN0808M

Siliconix

80V N-Channel Enhancement Mode MOSPOWER

This power FET is designed especially for low power high frequency inverters, interface to CMOS and TTL logic, and line drivers.

FEATURES

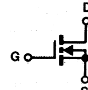
- High Input Impedance
- Extremely Fast Switching
- Rugged — Dissipation Limited SOA
- Internal Drain-Source Diode
- Low Cost Package

Product Summary

Part Number	PRO ELECTRON Part Number	BV_{DSS} (Volts)	$R_{DS(on)}$ (Ohms)	Package
VN0808M	BSR67	80	4	TO-237

BENEFITS

- Reduced Component Count
- Simpler Designs
  — Directly Interfaces CMOS & TTL
- Improved Circuit Performance
- Increased Reliability



ABSOLUTE MAXIMUM RATINGS ($T_A = 25°C$ unless otherwise noted)

Drain-Source Voltage 80V

Drain-Gate Voltage 80V

Gate Current (Peak). . . . . ±1A

Gate-Source Voltage . . . . ±40V

Drain Current
Continuous[1] . . . . ±0.35A
Pulsed[2] . . . . ±2A

Maximum Dissipation at 25°C Case . . . 1W

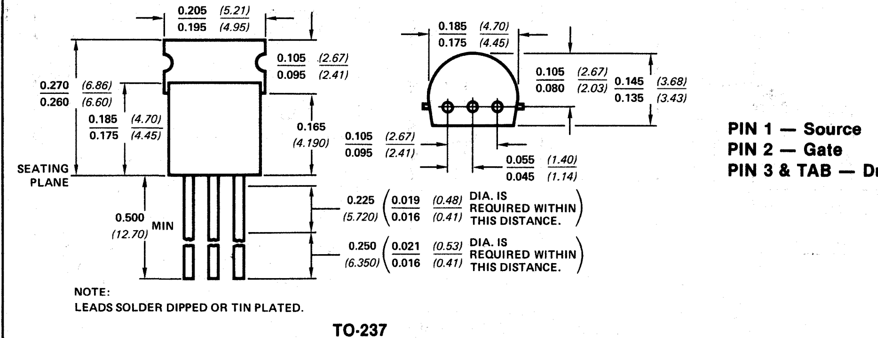
Linear Derating Factor. . . . . 8 mW/°C

Operating and Storage
Temperature. . . . . –55°C to +150°C

Lead Temperature
(1/16" from Case for 10 secs) . . +300°C

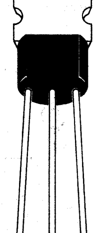
Notes:
1. Limited by package dissipation.
2. Pulse test — 80μs to 300μs, 1% duty cycle.

PACKAGE DIMENSIONS



TO-237

PIN 1 — Source
PIN 2 — Gate
PIN 3 & TAB — Drain



ELECTRICAL CHARACTERISTICS ($T_C = 25°C$ unless otherwise noted)

Symbol	Parameter	Min	Max	Unit	Test Conditions
	Static				
BV_{DSS}	Drain-Source Breakdown	80		V	$V_{GS} = 0$, $I_D = 10\ \mu A$
$V_{GS(th)}$	Gate Threshold Voltage	0.8	2	V	$V_{DS} = V_{GS}$, $I_D = 1$ mA
I_{GSS}	Gate Body Leakage		100	nA	$V_{GS} = 15V$, $V_{DS} = 0$
I_{DSS}	Zero Gate Voltage Drain Current		10	μA	V_{DS} = Max Ratings, $V_{GS} = 0$
$V_{DS(on)}$	Drain-Source Saturation Voltage[1]		4.0	V	$V_{GS} = 10V$, $I_D = 1A$
$r_{DS(on)}$	Drain-Source ON Resistance[1]		4.0	Ω	$V_{DS} = 10V$, $I_D = 1A$
$I_{D(on)}$	ON-State Drain Current[1]	1.5		A	$V_{DS} = 25V$, $V_{GS} = 10V$
	Dynamic				
g_{fs}	Forward Transconductance[1]	170		mS	$V_{DS} = 25V$, $I_D = 0.5A$
C_{iss}	Input Capacitance		50	pF	$V_{DS} = 25V$, $V_{GS} = 0$, f = 1 MHz
C_{rss}	Reverse Transfer Capacitance		10	pF	$V_{DS} = 25V$, $V_{GS} = 0$, f = 1 MHz
C_{oss}	Common-Source Output Capacitance		40	pF	$V_{DS} = 25V$, $V_{GS} = 0$, f = 1 MHz
t_{ON}	Turn-ON Time		10	ns	$V_{DD} = 25V$, $I_D \approx 1A$, $R_L = 23\Omega$, $R_g = 25\Omega$
t_{OFF}	Turn-OFF Time		10	ns	$V_{DD} = 25V$, $I_D \approx 1A$, $R_L = 23\Omega$, $R_g = 25\Omega$
	Drain-Source Diode Characteristics				
		Typ			
V_{SD}	Forward ON Voltage[1]	−0.9		V	$I_S = -1A$, $V_{GS} = 0$
t_{rr}	Reverse Recovery Time	35		ns	$V_{GS} = 0$, $I_F = I_R = 1A$

Note:
1. Pulse test 80-300 μS, 1% duty cycle.

Refer to VNMA Design Curves (See Section 4)

TEST CIRCUITS

FIGURE 1 Switching Test Circuit

P.W. = 1 μs
DUTY CYCLE = 1%
$C_S \leq 50$ pF

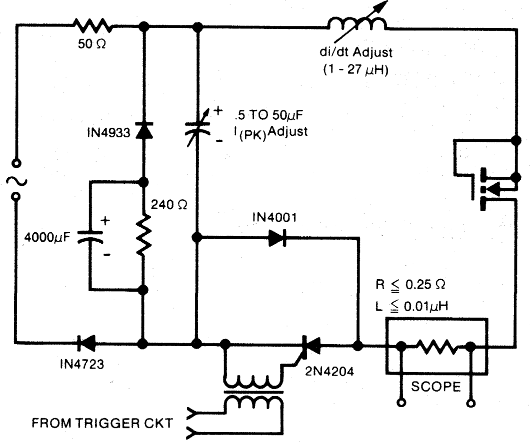


FIGURE 2 JEDEC Reverse Recovery Circuit

VN2406B ■ VN1706B ■ VN1206B
VN2406D ■ VN1706D ■ VN1206D

240V N-Channel Enhancement Mode MOSPOWER

These power FETs are designed especially for off-line switching regulators, converters, solenoid and relay drivers.

Product Summary

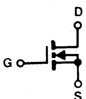
Part Number	BV_{DSS}	$R_{DS(ON)}$	I_D	Package
VN2406B	240V	6Ω	0.8A	TO-39
VN1706B	170V			
VN1206B	120V			
VN2406D	240V	6Ω	1.4A	TO-220AB
VN1706D	170V			
VN1206D	120V			

FEATURES

- High Voltage
- No Second Breakdown
- High Input Impedance
- Internal Drain-Source Diode
- Very Rugged: Excellent SOA
- Extremely Fast Switching

BENEFITS

- Reduced Component Count
- Improved Performance
- Simpler Designs
- Improved Reliability



ABSOLUTE MAXIMUM RATINGS (T_C = 25°C unless otherwise noted)

Drain-Source Voltage
- VN1210B, D 120V
- VN1710B, D 170V
- VN2410B, D 240V

Drain-Gate Voltage
- VN1210B, D 120V
- VN1710B, D 170V
- VN2410B, D 240V

Gate Current (Peak) .... ±1A

Gate Source Voltage .... ±40V

Drain Current
- Continuous[1]
  - B Suffix .... ±0.8A
  - D Suffix .... ±1.4A
- Pulsed[2] .... ±3A

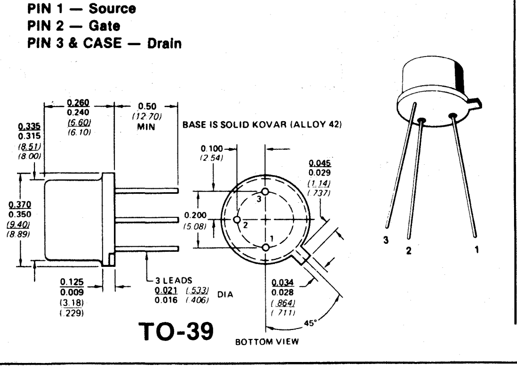
	TO-39	TO-220AB
Total Power Dissipation	6.25W	20W
Linear Derating Factor	50mW/°C	160mW/°C

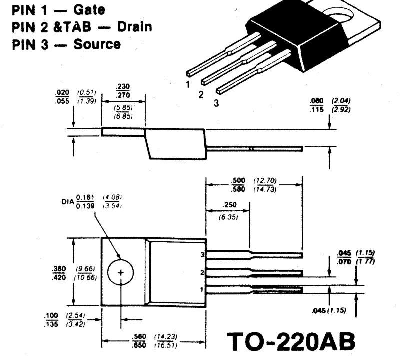
Operating and Storage Temperature .... −55°C to +150°C

Lead Temperature (1 1/16" from Case for 10 secs) .... +300°C

Notes:
1. Limited by package dissipation.
2. Pulse test—80μs to 300μs, 1% duty cycle.

PACKAGE DIMENSIONS





ELECTRICAL CHARACTERISTICS ($T_C = 25°C$ unless otherwise noted)

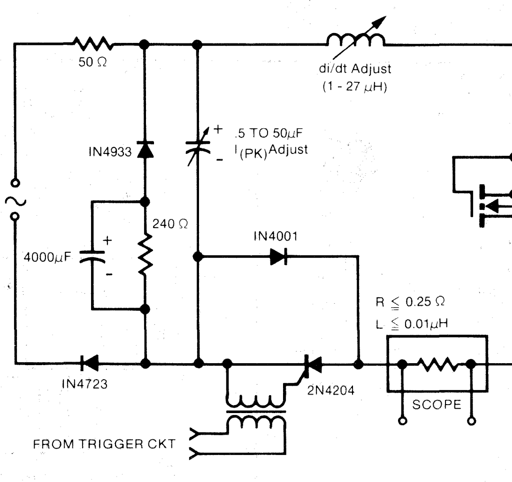
Symbol	Characteristics	Type	Min	Max	Unit	Test Conditions
		Static				
BV_{DSS}	Drain-Source Breakdown	VN2406B VN1706B VN1206B	240 170 120		V	$V_{GS} = 0$, $I_D = 100 \mu A$
		VN2406D VN1706D VN1206D	240 170 120			
$V_{GS(th)}$	Gate Threshold Voltage	All	0.8	2.0	V	$V_{DS} = V_{GS}$, $I_D = 1mA$
I_{GSS}	Gate Body Leakage	All		100	nA	$V_{DS} = 0$, $V_{GS} = 15V$
				500		$V_{DS} = 0$, $V_{GS} = 15V$, $T_A = 125°C$
I_{DSS}	Zero Gate Voltage Drain Current	All		10	μA	$V_{DS} = 120V$, $V_{GS} = 0$
				500		$V_{DS} = 120V$, $V_{GS} = 0$, $T_A = 125°C$
$V_{DS(on)}$	**Drain-Source Saturation Voltage**[1]			1.0	V	$V_{GS} = 2.5V$, $I_D = 0.1A$
				3.0		$V_{GS} = 10V$, $I_D = 0.5A$
$r_{DS(on)}$	**Drain-Source On Resistance**[1]			10	Ω	$V_{GS} = 2.5V$, $I_D = 0.1A$
				6		$V_{GS} = 10V$, $I_D = 0.5A$
$I_{D(on)}$	**On-State Drain Current**[1]	All	1.0		A	$V_{DS} = 25V$, $V_{GS} = 10V$
		Dynamic				
g_{fs}	**Forward Transconductance**[1]	All	300		mS	$V_{DS} = 25V$, $I_D = 0.5A$
C_{iss}	Input Capacitance	All		125	pF	$V_{GS} = 0$, $V_{DS} = 25V$, $f = 1$ MHz
C_{rss}	Reverse Transfer Capacitance	All		20		
C_{oss}	Common-Source Output Capacitance	All		50		
		Drain-Source Diode Characteristics				
			Typ			
V_{SD}	**Forward ON Voltage**[1]		−1.2		V	$I_S = -1.0A$, $V_{GS} = 0$
t_{rr}	Reverse Recovery Time		100		ns	$I_F = I_R = 1.0A$, $V_{GS} = 0$ (Figure 1)

Note 1: Pulse test — 80 μs to 300 μs, 1% duty cycle

Refer to VNDB24 Design Curves (See Section 4)

TEST CIRCUIT

Reverse Recovery Test Circuit



VN2406L ■ VN1706L ■ VN1206L
VN2406M ■ VN1706M ■ VN1206M

240V N-Channel Enhancement Mode MOSPOWER

These power FETs are designed especially for off-line switching regulators, converters, solenoid and relay drivers.

FEATURES

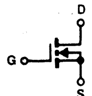
- High Voltage
- No Second Breakdown
- High Input Impedance
- Internal Drain-Source Diode
- Very Rugged: Excellent SOA
- Extremely Fast Switching

BENEFITS

- Reduced Component Count
- Improved Performance
- Simpler Designs
- Improved Reliability

Product Summary

Part Number	BV_{DSS}	$R_{DS(ON)}$	I_D	Package
VN2406L	240V	6Ω	0.21A	TO-92
VN1706L	170V			
VN1206L	120V			
VN2406M	240V	6Ω	0.33A	TO-237
VN1706M	170V			
VN1206M	120V			



ABSOLUTE MAXIMUM RATINGS ($T_C = 25°C$ unless otherwise noted)

Drain-Source Voltage
- VN2406L,VN1706M 240V
- VN1706L,VN1706M 170V
- VN1206L,VN1206M 120V

Drain-Gate Voltage
- VN2406L,VN1206M 120V
- VN1706L,VN1706M 170V
- VN1206L,VN1206M 120V

Drain Current Continuous[1]
- VN1206L,VN1706L,VN2406L .... ±0.21A
- VN1206M,VN1706M,VN2406M .... ±0.33A

Pulsed[2]
- TO-92 .... ±1.0A
- TO-237 .... ±1.0A

Gate Current (Peak) .... ±1A

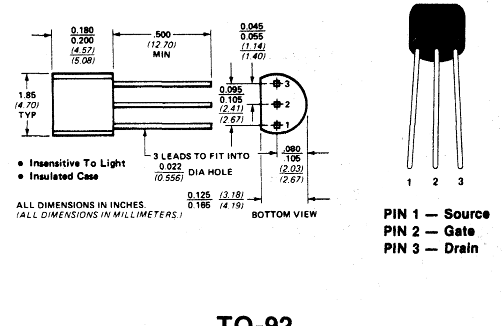
Gate Source Voltage .... ±40V

	TO-92	TO-237
Total Power Dissipation	0.4W	1.0W
Linear Derating Factor	3.2mW/°C	8mW/°C

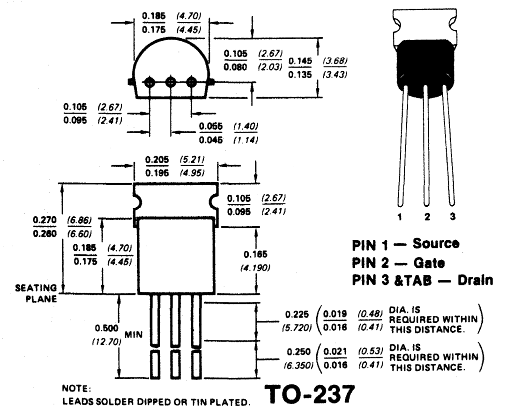
Operating and Storage Temperature .... −55°C to +150°C

Notes:
1. Limited by package dissipation.
2. Pulse test: 80μs - 300μs, 1% duty cycle.

PACKAGE DIMENSIONS



TO-92



TO-237

ELECTRICAL CHARACTERISTICS ($T_C = 25°C$ unless otherwise noted)

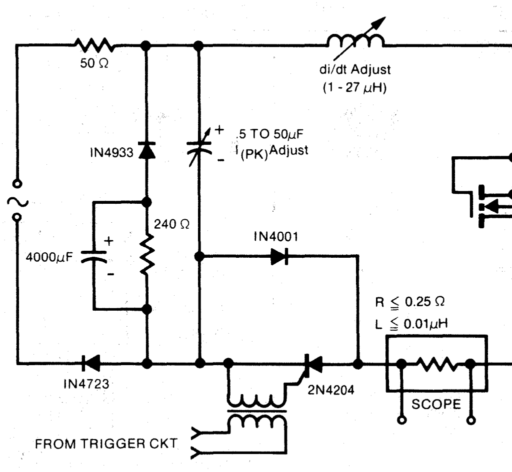
Symbol	Characteristics	Type	Min	Max	Unit	Test Conditions
			Static			
BV_{DSS}	Drain-Source Breakdown	VN2406L VN1706L VN1206L	240 170 120		V	$V_{GS} = 0$, $I_D = 100\mu A$
		VN2406M VN1706M VN1206M	240 170 120			
$V_{GS(th)}$	Gate Threshold Voltage	All	0.8	2.0	V	$V_{DS} = V_{GS}$, $I_D = 1mA$
I_{GSS}	Gate Body Leakage	All		100	nA	$V_{DS} = 0$, $V_{GS} = 15V$
				500		$V_{GS} = 15V$, $V_{DS} = 0$, $T_A = 125°C$
I_{DSS}	Zero Gate Voltage Drain Current	All		10	μA	$V_{DS} = 120V$, $V_{GS} = 0$
				500		$V_{DS} = 120V$, $V_{GS} = 0$, $T_C = 125°C$
$V_{DS(on)}$	Drain-Source Saturation Voltage[1]			1.0	V	$V_{GS} = 2.5V$, $I_D = 0.1A$
				3.0		$V_{GS} = 10V$, $I_D = 0.5A$
$r_{DS(on)}$	Drain-Source On Resistance[1]			10	Ω	$V_{GS} = 2.5V$, $I_D = 0.1A$
				6		$V_{GS} = 10V$, $I_D = 0.5A$
$I_{D(on)}$	On-State Drain Current[1]	All	1.0		A	$V_{DS} = 25V$, $V_{GS} = 10V$
			Dynamic			
g_{fs}	Forward Transconductance[1]	All	300		mS	$V_{DS} = 25V$, $I_D = 0.5A$
C_{iss}	Input Capacitance	All		125	pF	$V_{GS} = 0$, $V_{DS} = 25V$, f= I MHz
C_{rss}	Reverse Transfer Capacitance	All		20		
C_{oss}	Common-Source Output Capacitance	All		50		
			Drain-Source Diode Characteristics			
			Typ			
V_{SD}	Forward ON Voltage[1]		−1.2		V	$I_S = -1.0A$, $V_{GS} = 0$
t_{rr}	Reverse Recovery Time		100		ns	$I_F = I_R = 1.0A$, $V_{GS} = 0$ (Figure 1)

Note 1: Pulse test — 80 μs to 300 μs, 1% duty cycle

Refer to VNDB24 Design Curves (See Section 4)

TEST CIRCUIT

Reverse Recovery Test Circuit



VN2410L ■ VN1710L ■ VN1210L
VN2410M ■ VN1710M ■ VN1210M

240V N-Channel Enhancement Mode MOSPOWER

Siliconix

These power FETs are designed especially for off-line switching regulators, converters, telephony, solenoid and relay drivers.

FEATURES

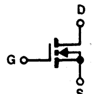
- High Voltage
- No Second Breakdown
- High Input Impedance
- Internal Drain-Source Diode
- Very Rugged: Excellent SOA
- Extremely Fast Switching

BENEFITS

- Reduced Component Count
- Improved Performance
- Simpler Designs
- Improved Reliability

Product Summary

Part Number	PRO ELECTRON Part Number	BV_{DSS}	$R_{DS(on)}$	I_D	Package
VN2410L		240V	10Ω	0.15	TO-92
VN1710L		170V			
VN1210L		120V			
VN2410M	BSR76	240V	10Ω	0.25	TO-237
VN1710M	BSR72	170V			
VN1210M	BSR70	120V			



ABSOLUTE MAXIMUM RATINGS (T_C = 25°C unless otherwise noted)

Drain-Source Voltage
- VN2410L,VN2410M 240V
- VN1710L,VN1710M 170V
- VN1210L,VN1210M 120V

Drain-Gate Voltage
- VN2410L,VN2410M 240V
- VN1710L,VN1710M 170V
- VN1210L,VN1210M 120V

Drain Current Continuous[1]
- VN2410L,VN1710L,VN1210L .... ± 0.16A
- VN2410M,VN1710M,VN1210M .... ± 0.25A

Pulsed[2]
- VN2410L,VN1710L,VN1210L .... ± 1.0A
- VN2410M,VN1710M,VN1210M .... ± 1.0A

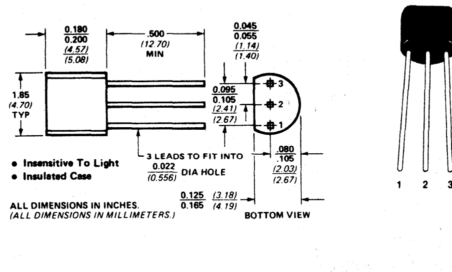
Gate Current (Peak) .... ± 1.0A
Gate-Source Voltage .... ± 40V

	TO-237	TO-92
Total Power Dissipation	1W	0.4W
Linear Derating Factor	8mW/°C	3.2mW/°C

Operating and Storage Temperature .... -55°C to +150°C

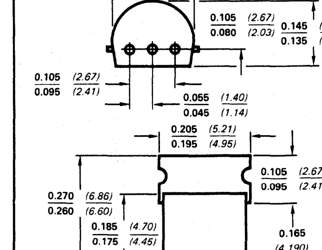
Notes:
1. Limited by package dissipation.
2. Pulse test: 80μs - 300μs, 1% duty cycle.

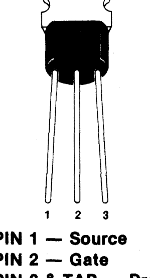
PACKAGE DIMENSIONS



PIN 1 — Source
PIN 2 — Gate
PIN 3 — Drain

TO-92
(L Suffix Parts)





PIN 1 — Source
PIN 2 — Gate
PIN 3 & TAB — Drain

NOTE:
LEADS SOLDER DIPPED OR TIN PLATED.

TO-237 (M Suffix Parts)

ELECTRICAL CHARACTERISTICS ($T_C = 25°C$ unless otherwise noted)

Symbol	Parameter	Part Number	Min	Max	Unit	Test Conditions
			Static			
BV_{DSS}	Drain-Source Breakdown	VN2410L VN1710L VN1210L	240 170 120		V	$V_{GS} = 0$, $I_D = 100\ \mu A$
		VN2410M VN1710M VN1210M	240 170 120			
$V_{GS(th)}$	Gate Threshold Voltage	All	0.8	2.0	V	$V_{GS} = V_{DS,}\ 1_D = 1$ mA
I_{GSS}	Gate Body Leakage	All		100	nA	$V_{GS} = 15V$, $V_{DS} = 0$
I_{DSS}	Zero Gate Voltage Drain Current	All		10	μA	$V_{DS} = 120V\ V_{DS,} V_{GS} = 0$
				500		$V_{DS} = 120V\ V_{DS,} V_{GS} = 0$, $T_C = 125°C$
$V_{DS(on)}$	Drain-Source Saturation Voltage	All		1.0	V	$V_{GS} = 2.5V$, $I_D = 0.10A$ (Note 1)
		All		5.0		$V_{GS} = 10V$, $I_D = 0.50A$ (Note 1)
$r_{DS(on)}$	Drain-Source On Resistance			10	Ω	$V_{GS} = 2.5V$, $I_D = 0.1A$ (Note 1)
				10		$V_{GS} = 10V$, $I_D = 0.5A$ (Note 1)
$I_{D(on)}$	On-State Drain Current	All	1.0		A	$V_{DS} = 25V$, $V_{GS} = 10V$ (Note 1)
			Dynamic			
g_{fs}	Forward Transconductance	All	300		mS	$V_{DS} = 25V$, $I_D = 0.5A$ (Note 1)
C_{iss}	Input Capacitance	All		125	pF	$V_{GS} = 0$, $V_{DS} = 25V$, f = 1 MHz
C_{rss}	Reverse Transfer Capacitance	All		20		
C_{oss}	Common-Source Output Capacitance	All		50		

Drain-Source Diode Characteristics

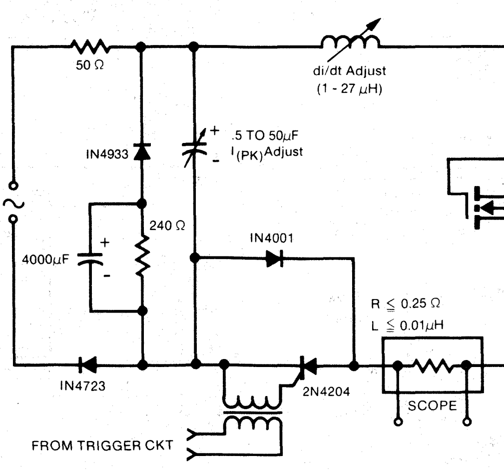
Symbol	Parameter	Part Number	Typ	Unit	Test Conditions
V_{SD}	Forward On Voltage	All	−1.2	V	$I_S = -1.0A$, $V_{GS} = 0$ (Note 1)
t_{rr}	Reverse Recovery Time	All	100	ns	$I_F = I_R = 1.0A$, $V_{GS} = 0$ (Figure 1)

Note 1: Pulse test — 80 μs to 300 μs, 1% duty cycle

Refer to VNDB24 Design Curves (See Section 4)

TEST CIRCUIT

Reverse Recovery Test Circuit



VN3500A ■ VN3501A ■ VN4000A ■ VN4001A
VN3500D ■ VN3501D ■ VN4000D ■ VN4001D

Siliconix

400V N-Channel Enhancement Mode MOSPOWER

These power FETs are designed especially for offline switching regulators, converters, solenoid and relay drivers.

FEATURES

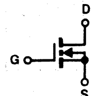
- High Voltage
- No Second Breakdown
- High Input Impedance
- Internal Drain-Source Diode
- High Threshold for Noise Immunity
- Very Rugged: Excellent SOA
- Extremely Fast Switching

BENEFITS

- Reduced Component Count
- Improved Performance
- Simpler Designs
- Improved Reliability

Product Summary

Part Number	PRO ELECTRON Part Number	BV_{DSS}	$R_{DS(on)}$	I_D	Package
VN3500A	BUP60	350V	1Ω	6A	TO-3
VN3500D					TO-220
VN3501A	BUP61		1.5Ω	5A	TO-3
VN3501D					TO-220
VN4000A	BUP62	400V	1.0Ω	6A	TO-3
VN4000D					TO-229
VN4001A	BUP63		1.5Ω	5A	TO-3
VN4001D					TO-220



ABSOLUTE MAXIMUM RATINGS ($T_C = 25°C$ unless otherwise noted)

Drain-Source Voltage
- VN3500A, D; VN3501A, D 350V
- VN0400A, D; VN4001A, D 400V

Drain-Gate Voltage
- VN3500A, D; VN3501A, D 350V
- VN4000A, D; VN4001A, D 400V

Drain Current
- Continuous[1]
  - VN3500A, D; VN4000A, D .... ±6A
  - VN3501A, D; VN4001A, D .... ±5A
- Pulsed[2]
  - A Suffix .... ±16A
  - D Suffix .... ±10A

Gate Current (Peak) .... ±3A

Gate-Source Voltage .... ±40V

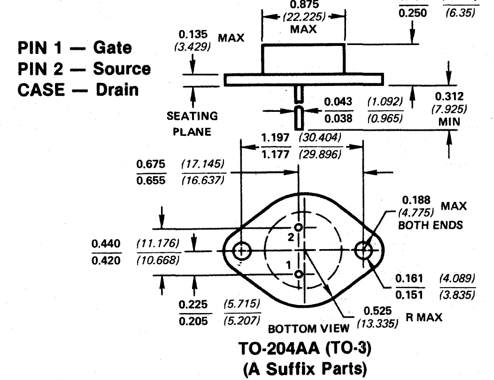
Total Power Dissipation, A Suffix 125W
- Linear Derating Factor .... 0.833W/°C

Total Power Dissipation, D Suffix 75W
- Linear Derating Factor .... 0.6W/°C

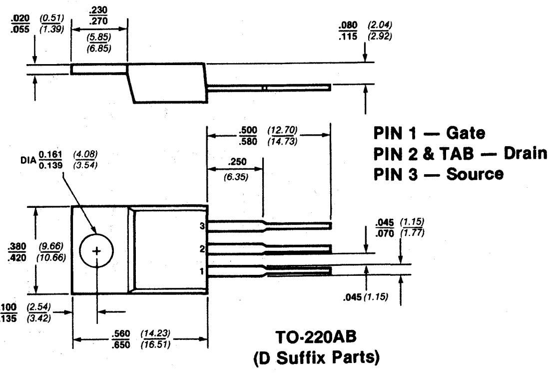
Storage and Junction Temperature
- A Suffix .... −55°C to +175°C
- D Suffix .... −55°C to +150°C

Notes:
1. Limited by package dissipation.
2. Pulse test—80μs to 300μs, 1% duty cycle.

PACKAGE DIMENSIONS



TO-204AA (TO-3)
(A Suffix Parts)



TO-220AB
(D Suffix Parts)

ELECTRICAL CHARACTERISTICS ($T_C = 25°C$ unless otherwise noted)

Parameter		Part Number	Min	Max	Unit	Test Conditions
Static						
BV_{DSS}	Drain-Source Breakdown	VN3500A, D VN3501A, D	350		V	$V_{GS} = 0$, $I_D = 1$ mA
		VN4000A, D VN4001A, D	400			
$V_{GS(th)}$	Gate Threshold Voltage	All	3	6	V	$V_{GS} = V_{DS}$, $I_D = 1$ mA,
I_{GSS}	Gate Body Leakage	All		100	nA	$V_{GS} = 30V$, $V_{DS} = 0$
I_{DSS}	Zero Gate Voltage Drain Current	All		1	mA	V_{DS} = Rated, V_{DS}, $V_{GS} = 0$
				2.5		V_{DS} = Rated V_{DS}, $V_{GS} = 0$, $T_C = 150°C$
$V_{DS(on)}$	Drain-Source Saturation Voltage	VN3500A, D VN4000A, D		3	V	$V_{GS} = 10V$, $I_D = 3A$ (Note 1)
		VN3501A, D VN4001A, D		4.5		
$r_{DS(on)}$	Drain-Source On Resistance	VN3500A, D VN4000A, D		1	Ω	$V_{GS} = 10V$, $I_D = 3A$ (Note 1)
		VN3501A, D VN4001A, D		1.5		
$I_{D(on)}$	On-State Drain Current	All	8		A	$V_{DS} = 25V$, $V_{GS} = 10V$ (Note 1)
Dynamic						
g_{fs}	Forward Transconductance	All	2.5		mS	$V_{DS} = 25V$, $I_D = 3A$ (Note 1)
C_{iss}	Input Capacitance	All		1000	pF	$V_{GS} = 0$, $V_{DS} = 25V$, f = 1 MHz
C_{rss}	Reverse Transfer Capacitance	All		40		
C_{oss}	Common-Source Output Capacitance	All		220		
$t_{d(on)}$	Turn-On Delay Time	All		50	ns	$V_{DD} = 200V$, $I_D \approx 1A$, $R_L = 67Ω$, $R_g = 10Ω$ (Figure 1)
t_r	Rise Time	All		50		
$t_{d(off)}$	Turn-Off Delay Time	All		100		
t_f	Fall Time	All		80		
Drain-Source Diode Characteristics						
			Typ			
V_{SD}	Forward ON Voltage	All	−1.2		V	$I_S = -4A$, $V_{GS} = 0$ (Note 1)
t_{rr}	Reverse Recovery Time	All	400		ns	$I_F = I_R = 4A$, $V_{GS} = 0$ (Figure 2)

Note:
1. Pulse test: 80 μs to 300 μs, 1% duty cycle.

Refer to VNDA40 Design Curves (See Section 4)

TEST CIRCUITS

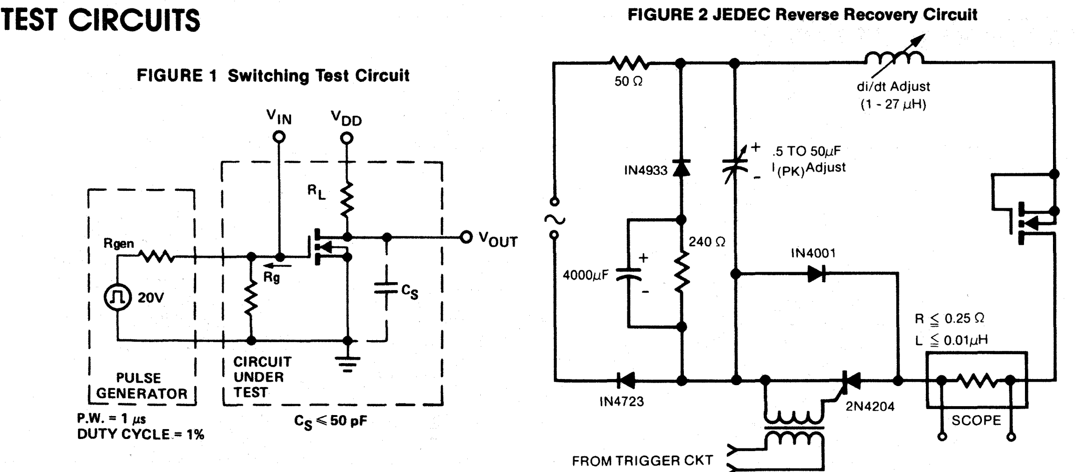


FIGURE 1 Switching Test Circuit

FIGURE 2 JEDEC Reverse Recovery Circuit

VN4501A ■ VN4501D ■ VN4502A ■ VN4502D
VN5001A ■ VN5001D ■ VN5002A ■ VN5002D

Siliconix

500V N-Channel Enhancement Mode MOSPOWER

These power FETs are designed especially for offline switching regulators, converters, solenoid and relay drivers.

FEATURES

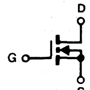
- High Voltage
- No Second Breakdown
- High Input Impedance
- Internal Drain-Source Diode
- High Threshold for Noise Immunity
- Very Rugged: Excellent SOA
- Extremely Fast Switching

BENEFITS

- Reduced Component Count
- Improved Performance
- Simpler Designs
- Improved Reliability

Product Summary

Part Number	PRO ELECTRON Part Number	BV_{DSS}	$R_{DS(on)}$	I_D	Package
VN4501A	BUP64	450V	1.5Ω	4.5A	TO-3
VN4501D					TO-220
VN4502A	BUP65		2Ω	4A	TO-3
VN4502D					TO-220
VN5001A	BUP66	500V	1.5Ω	4.5A	TO-3
VN5001D					TO-220
VN5002A	BUP67		2Ω	4A	TO-3
VN5002D					TO-220



ABSOLUTE MAXIMUM RATINGS (T_C=25°C unless otherwise noted)

Drain-Source Voltage
- VN4501, VN4502 . . . 450V
- VN5001, VN5002 . . . 500V

Drain-Gate Voltage
- VN4501, VN4502 . . . 450V
- VN5001, VN5002 . . . 500V

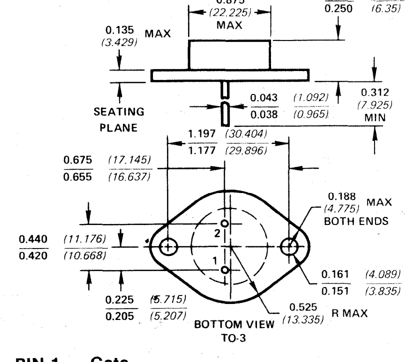
Drain Current Continuous
- VN4501A,D; VN5001A,D . . . ±4.5A
- VN4502A,D; VN5001A,D . . . ±4A
- Pulsed (80 μs-300 μs, 1% duty cycle) . . . ± 10A

Gate Current (Peak) . . . ± 3A

Gate-Source Voltage . . . ±40V

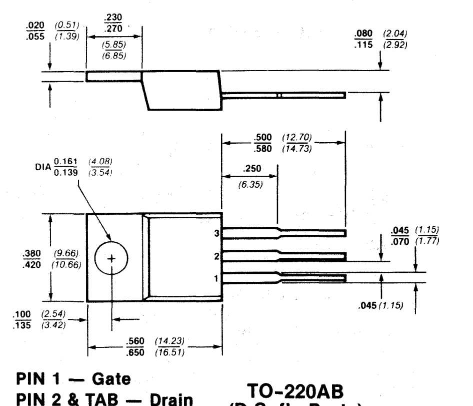
	TO-3	TO-220AB
Maximum Power Dissipation	100W	75W
Linear Derating Factor	0.67W/°C	0.6W/°C
Operating and Storage Temperature	− 55°C to +175°C	− 40°C to +150°C

PACKAGE DIMENSIONS



PIN 1 — Gate
PIN 2 — Source
CASE — Drain

TO-204AA (TO-3)
(A Suffix Parts)



PIN 1 — Gate
PIN 2 & TAB — Drain
PIN 3 — Source

TO-220AB
(D Sufix Parts)

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Parameter		Part Number	Min	Max	Unit	Test Conditions
Static						
BV_{DSS}	Drain-Source Breakdown	VN4501A, D VN4502A, D	450		V	$V_{GS} = 0$, $I_D = 1.0$ mA
		VN5001A, D VN5002A, D	500			
$V_{GS(th)}$	Gate Threshold Voltage	All	3.0	6.0		$V_{DS} = V_{GS}$, $I_D = 1$ mA
I_{GSS}	Gate-Body Leakage	All		100	nA	$V_{GS} = 30V$, $V_{DS} = 0$
I_{DSS}	Zero Gate Voltage Drain Current	All		1.0	mA	V_{DS} = Rated V_{DS}, $V_{GS} = 0$
				4.0		V_{DS} = Rated V_{DS}, $V_{GS} = 0$, $T_C = 150°C$
$I_{D(on)}$	On-State Drain Current[1]	All	6.0		A	$V_{DS} = 25V$, $V_{GS} = 10V$
$V_{DS(on)}$	Drain-Source Saturation Voltage[1]	VN4501A, D VN5001A, D		3.0	V	$V_{GS} = 10V$, $I_D = 2.0A$
		VN4502A, D VN5002A, D		4.0		
$r_{DS(on)}$	Static Drain-Source On-State Resistance[1]	VN4501A, D VN5001A, D		1.5	Ω	$V_{GS} = 10V$, $I_D = 2.0A$
		VN4502A, D VN5002A, D		2.0		
Dynamic						
g_{fs}	Forward Transconductance[1]	All	2.5		S	$V_{DS} = 25V$, $I_D = 2.0A$
C_{iss}	Input Capacitance	All		1000	pF	$V_{GS} = 0$, $V_{DS} = 25V$, f = 1 MHz
C_{oss}	Output Capacitance			220		
C_{rss}	Reverse Transfer Capacitance			40		
$t_{d(on)}$	Turn-On Delay Time	All		50	ns	$V_{DD} = 200V$, $I_D \approx 2A$, $R_L = 100\Omega$, $R_g = 10\Omega$ (Fig 1)
t_r	Rise Time	All		50		
$t_{d(off)}$	Turn-Off Delay Time	All		100		
t_f	Fall Time	All		100		
Drain-Source Diode Characteristics						
			Typ			
V_{SD}	Forward On Voltage[1]	All	−1.2		V	$I_S = -4A$, $V_{GS} = 0$
t_{rr}	Reverse Recovery Time	All	400		ns	$I_F = I_R = 4A$, $V_{GS} = 0$ (Fig 2)

Note:
1. Pulse test: 80 μs-300 μs, 1% duty cycle.

Refer to VNDA50 Design Curves (See Section 4)

TEST CIRCUITS

FIGURE 1 Switching Test Circuit

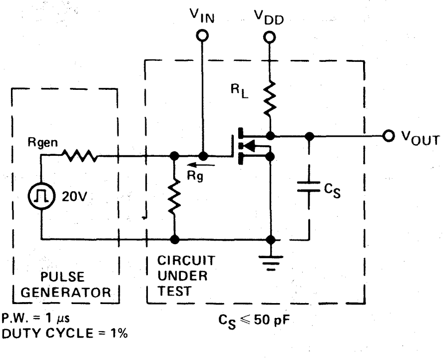
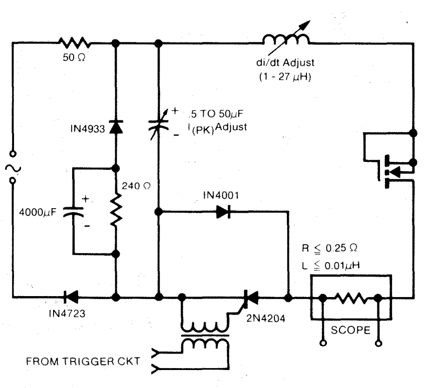


FIGURE 2 Reverse Recovery Test Circuit



VP0300M ■ VP0300B

30V P-Channel Enhancement Mode MOSPOWER

This power FET is designed especially for low power high frequency inverters, interface to CMOS and TTL logic, line drivers.

FEATURES

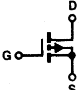
- **High Input Impedance**
- **Extremely Fast Switching**
- **Rugged — Dissipation Limited SOA**
- **Internal Drain-Source Diode**

BENEFITS

- **Reduced Component Count**
- **Simpler Designs**
- **Improved Circuit Performance**
- **Increased Reliability**

Product Summary

Part Number	PRO ELECTRON Part Number	BV_{DSS} (Volts)	$R_{DS(on)}$ (Ohms)	Package
VN0300M	BSR78	−30	2.5	TO-237
VP0300B		−30	2.5	TO-39



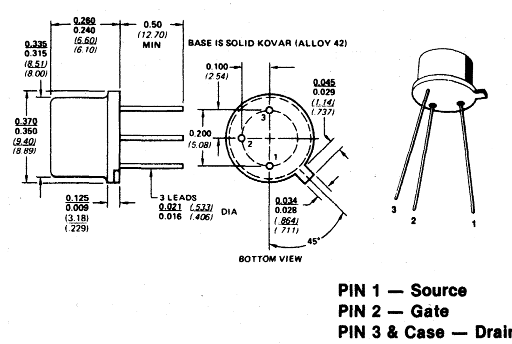
ABSOLUTE MAXIMUM RATINGS (T_A=25°C unless otherwise noted)

Drain-Source Voltage .... −30V
Drain-Gate Voltage .... −30V
Gate Current (Peak) .... ±1A
Gate-Source Voltage .... ±40V
Drain Current
  Continuous[1]
    M Suffix .... ±0.48A
    B Suffix .... ±1.5A
  Pulsed[2] .... ±3A
Power Dissipation
  TO-39 .... 6.25W
  TO-237 .... 1W

Linear Derating Factor
  TO-39 .... 50mW/°C
  TO-237 .... 8mW/°C
Operating and Storage
  Temperature .... −55°C to +150°C
Lead Temperature
  (1/16″ from case for 10 secs) .... +300°C

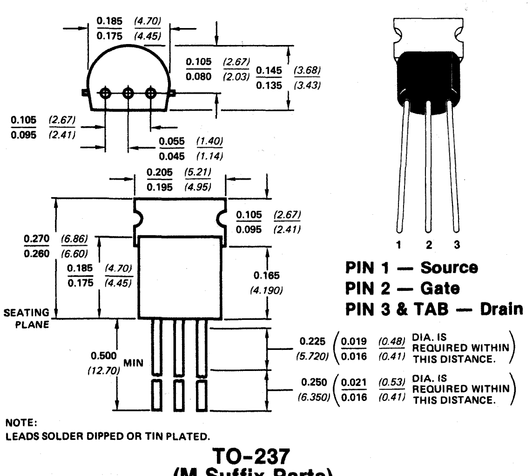
Notes:
1. Limited by package dissipation.
2. Pulse test — 80μs to 300μs, 1% duty cycle.

PACKAGE DIMENSIONS



PIN 1 — Source
PIN 2 — Gate
PIN 3 & Case — Drain

TO-39
(B Suffix Parts)



PIN 1 — Source
PIN 2 — Gate
PIN 3 & TAB — Drain

NOTE:
LEADS SOLDER DIPPED OR TIN PLATED.

TO-237
(M Suffix Parts)

ELECTRICAL CHARACTERISTICS ($T_C = 25°C$ unless otherwise noted)

	Parameter	Min	Max	Unit	Test Conditions
		Static			
BV_{DSS}	Drain-Source Breakdown	−30		V	$V_{GS} = 0$; $I_D = -10\mu A$
$V_{GS(th)}$	Gate Threshold Voltage	−2	−4.5	V	$V_{DS} = V_{GS}$, $I_D = -1\,mA$
I_{GSS}	Gate Body Leakage		−0.1	μA	$V_{GS} = -30V$, $V_{DS} = 0$
I_{DSS}	Zero Gate Voltage Drain Current		−10	μA	$V_{GS} = 0$, $V_{DS} = -25V$
$V_{DS(on)}$	Drain-Source Saturation Voltage[1]		−2.5	V	$V_{GS} = -10V$, $I_D = -1A$
$r_{DS(on)}$	Drain-Source On Resistance[1]		2.5	Ω	$V_{GS} = -10V$, $I_D = -1A$
$I_{D(on)}$	On-State Drain Current[1]	−1.5		A	$V_{GS} = -10V$, $V_{DS} = -15V$
		Dynamic			
g_{fs}	Forward Transconductance[1]	200		mS	$V_{DS} = -15V$, $I_D = -0.5A$
C_{iss}	Input Capacitance		150	pF	$V_{DS} = -15V$, $V_{GS} = 0$, $f = 1\,MHz$
C_{rss}	Reverse Transfer Capacitance		60		
C_{oss}	Common-Source Output Capacitance		100		
t_{ON}	Turn-ON Time		30	ns	$V_{DD} = -25V$, $R_L = 23\Omega$, $R_g = 25\Omega$, $I_D \approx -1A$
t_{OFF}	Turn-OFF Time		30		
		Drain-Source Diode Characteristics			
		Typ			
V_{SD}	Forward ON Voltage[1]	−1.2		V	$V_{GS} = 0$, $I_S = -0.5A$
t_{rr}	Reverse Recovery Time	52		ns	$V_{GS} = 0$, $I_F = I_R = -0.5A$

Note 1: Pulse test — 80μs to 300μs, 1% duty cycle

Refer to VPMH03 Design Curves (See Section 4)

TEST CIRCUITS

FIGURE 1. Switching Test Circuit

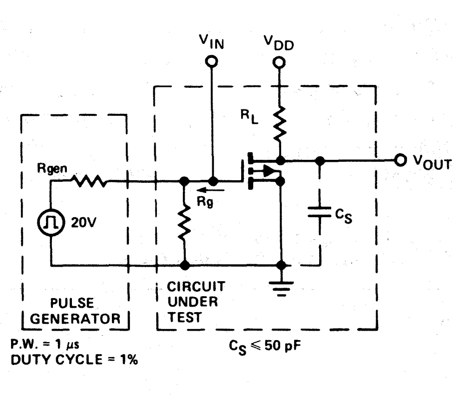
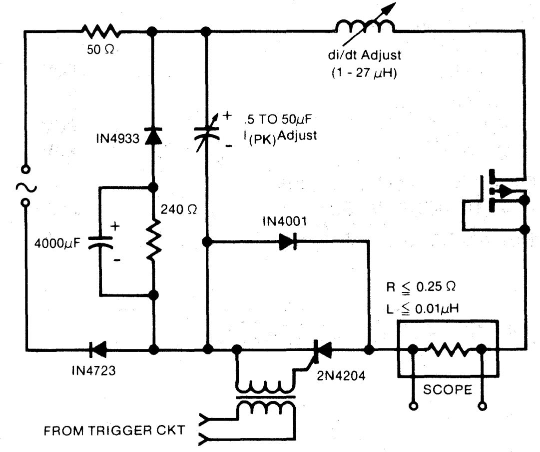


FIGURE 2. Reverse Recovery Test Circuit



VP1008B ■ VP0808B

Siliconix

100V P- Channel Enhancement Mode MOSPOWER

These power FET's are designed especially for low power, high frequency inverters, and interfaces to C-MOS and line drivers.

FEATURES

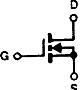
- High Voltage
- No Second Breakdown
- High Input Impedance
- Internal Drain-Source Diode
- Very Rugged: Excellent SOA
- Extremely Fast Switching

BENEFITS

- Reduced Component Count
- Improved Performance
- Simpler Designs
- Improved Reliability

Product Summary

Part Number	BV_{DSS}	$R_{DS(ON)}$	I_D	Package
VP1008B	100V	5.0Ω	0.9A	TO-39
VP0808B	80V			



ABSOLUTE MAXIMUM RATINGS (T_C = 25°C unless otherwise noted)

Drain-Source Voltage
- VP1008B .... -100V
- VP0808B .... -80V

Drain-Gate Voltage
- VP1008B .... -100V
- VP0808B .... -80V

Drain Current Continuous[1]
- VP1008B,VP0808B .... ± 0.9A

Pulsed[2] .... ± 3.0A

Gate Current (Peak) .... ± 1.0A

Gate Source Voltage .... ±40V

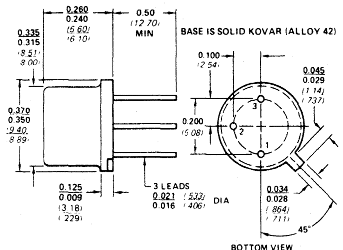
Total Power Dissipation 6.25W

Linear Derating Factor .... 50mW/°C

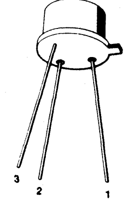
Operating and Storage Temperature .... –55°C to +150°C

Notes:
1. Limited by package dissipation.
2. Pulse test—80μs to 300μs, 1% duty cycle.

PACKAGE DIMENSIONS



PIN 1 — Source
PIN 2 — Gate
PIN 3 & CASE — Drain



TO-39

ELECTRICAL CHARACTERISTICS ($T_C = 25°C$ unless otherwise noted)

	Parameter	Part Number	Min	Max	Unit	Test Conditions
Static						
BV_{DSS}	Drain-Source Breakdown	VP1008B	−100		V	$V_{GS} = 0$, $I_D = -10\mu A$
		VP0808B	−80			
$V_{GS(th)}$	Gate-Source Threshold Voltage	All	−2	−4.5	V	$V_{DS} = V_{GS}$, $I_D = -1\,mA$
I_{GSS}	Gate Body Leakage	All		100	nA	$V_{GS} = -15V$, $V_{DS} = 0$
I_{DSS}	Zero Gate Voltage Drain Current	All		−10	μA	V_{DS} = Rated V_{DS}, $V_{GS} = 0$
				−500		V_{DS} = Rated V_{DS}, $V_{GS} = 0$, $T_C = 150°C$
$V_{DS(on)}$	Drain-Source Saturation Voltage	All		−5	V	$V_{GS} = -10V$, $I_D = -1A$ (Note 1)
$r_{DS(on)}$	Drain-Source On Resistance	All		5	Ω	$V_{GS} = -10V$, $I_D = -1A$ (Note 1)
$I_{D(on)}$	On-State Drain Current	All	−1.1		A	$V_{DS} = -25V$, $V_{GS} = -10V$ (Note 1)
Dynamic						
g_{fs}	Forward Transconductance	All	200		mS	$V_{DS} = -25V$, $I_D = -0.5A$ (Note 1)
C_{iss}	Input Capacitance	All		150	pF	$V_{DS} = -25V$, $V_{GS} = 0$, $f = 1\,MHz$
C_{rss}	Reverse Transfer Capacitance	All		60		
C_{oss}	Common-Source Output Capacitance	All		60		
$t_{d(on)}$	Turn-ON Delay Time	All		10	ns	$V_{DD} = -25V$, $I_D \approx -0.5A$, $R_L = 47\Omega$, $R_g = 25\Omega$ Figure 1
t_r	Rise Time	All		10		
$t_{d(off)}$	Turn-OFF Delay Time	All		10		
t_f	Fall Time	All		10		
Drain-Source Diode Characteristics						
			Typ			
V_{SD}	Forward ON Voltage	All	−1.2		V	$V_{GS} = 0$, $I_S = -1A$ (Note 1)
t_{rr}	Reverse Recovery Time	All	65		ns	$V_{GS} = 0$, $I_F = I_R = 0.5A$ (Figure 2)

Note 1: Pulse test — 80μs to 300μs, 1% duty cycle

Refer to VPMH10 Design Curves (See Section 4)

TEST CIRCUITS

FIGURE 1. Switching Test Circuit

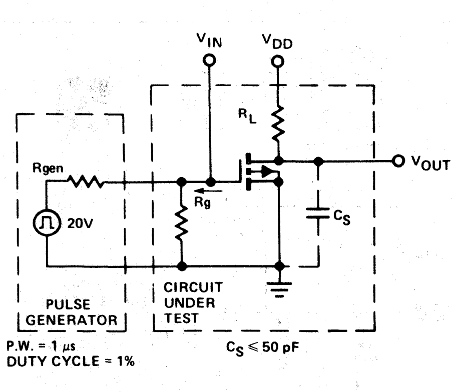
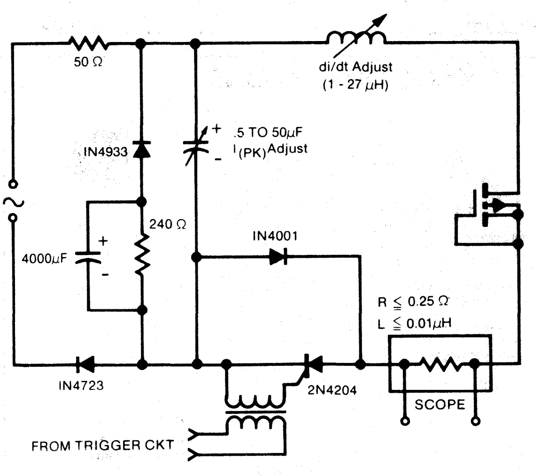


FIGURE 2. Reverse Recovery Test Circuit



VP1008L ■ VP0808L ■ VP1008M ■ VP0808M

Siliconix

100V P-Channel Enhancement Mode MOSPOWER

These power FETs are designed especially for low power, high frequency inverters and interfaces to CMOS and line drivers.

FEATURES

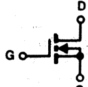
- High Voltage
- No Second Breakdown
- High Input Impedance
- Internal Drain-Source Diode
- Very Rugged: Excellent SOA
- Extremely Fast Switching

BENEFITS

- Reduced Component Count
- Improved Performance
- Simpler Designs
- Improved Reliability

Product Summary

Part Number	BV_{DSS}	$R_{DS(on)}$	I_D	Package
VP1008L	100V	5Ω	0.23	TO-92
VP0808L	80V			
VP1008M	100V	5Ω	0.37	TO-237
VP0808M	80V			



ABSOLUTE MAXIMUM RATINGS (T_C = 25°C unless otherwise noted)

Drain-Source Voltage
- VP1008L,VP1008M .... -100V
- VP0808L,VP0808M .... -80V

Drain-Gate Voltage
- VP1008L,VP1008M .... -100V
- VP0808L,VP0808M .... -80V

Drain Current Continuous[1]
- VP1008L,VP0808L .... ± 0.23A
- VP1008M,VP0808M .... ± 0.37A

Pulsed[2] .... ± 3.0A

Gate Current (Peak) .... ± 1.0A

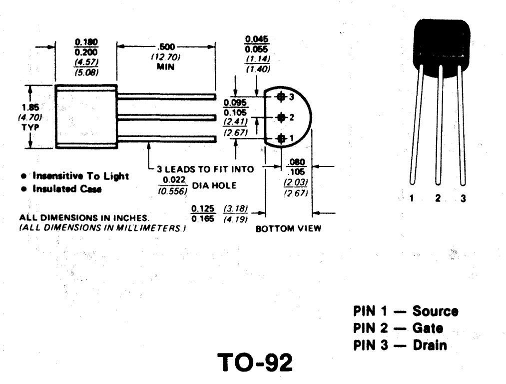
Gate Source Voltage .... ±40V

	To-92	To-237
Total Power Dissipation	0.4W	1.0W
Linear Derating Factor ..	3mW/°C	8mW/°C

Storage and Junction Temperature .... -55°C to +150°C

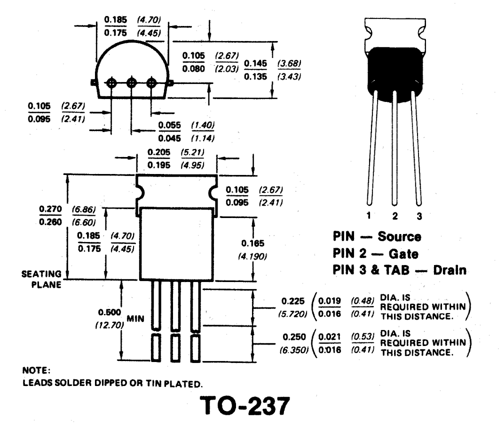
Notes:
1. Limited by package dissipation.
2. Pulse test—80μs to 300μs, 1% duty cycle.

PACKAGE DIMENSIONS



PIN 1 — Source
PIN 2 — Gate
PIN 3 — Drain

TO-92



TO-237

ELECTRICAL CHARACTERISTICS ($T_C = 25°C$ unless otherwise noted)

Parameter		Part Number	Min	Max	Unit	Test Conditions
Static						
BV_{DSS}	Drain-Source Breakdown	VP1008L VP0808L	100 80		V	$V_{GS} = 0$, $I_D = -10 \mu A$
		VP1008M VP0808M	100 80			
$V_{GS(th)}$	Gate-Source Threshold Voltage	All	−2	−4.5	V	$V_{DS} = V_{GS}$, $I_D = -1 mA$
I_{GSS}	Gate Body Leakage	All		100	nA	$V_{GS} = -30 V$, $V_{DS} = 0$
I_{DSS}	Zero Gate Voltage Drain Current	All		−10	μA	V_{DS} = Rated V_{DS}, $V_{GS} = 0$
				−500		V_{DS} = Rated V_{DS}, $V_{GS} = 0$, $T_C = 125°C$
$V_{DS(on)}$	Drain-Source Saturation Voltage[1]	All		−5	V	$V_{GS} = -10 V$, $I_D = -1 A$ (Note 1)
$r_{DS(on)}$	Drain-Source On Resistance	All		5	Ω	$V_{GS} = -10 V$, $I_D = -1 A$ (Note 1)
$I_{D(on)}$	On-State Drain Current	All	−1.1		A	$V_{DS} = -25 V$, $V_{GS} = -10 V$ (Note 1)
Dynamic						
g_{fs}	Forward Transconductance	All	200		mS	$V_{DS} = -25 V$, $I_D = -0.5 A$ (Note 1)
C_{iss}	Input Capacitance	All		150	pF	$V_{GS} = 0$, $V_{DS} = 25 V$, $f = 1 MHz$
C_{rss}	Reverse Transfer Capacitance	All		60		
C_{oss}	Common-Source Output Capacitance	All		60		
$t_{d(on)}$	Turn-On Delay Time	All		30	ns	$V_{DD} = -25 V$, $I_D \approx -0.5 A$, $R_L = 45 \Omega$, $R_g = 25 \Omega$ (Figure 1)
t_r	Rise Time	All		30		
$t_{d(off)}$	Turn-OFF Delay Time	All		30		
t_f	Fall Time	All		30		
Drain-Source Diode Characteristics						
			Typ			
V_{SD}	Forward ON Voltage	All	1.2		V	$V_{GS} = 0$, $I_S = 1 A$ (Note 1)
t_{rr}	Reverse Recovery Time	All	65		ns	$V_{GS} = 0$, $I_F = I_R = 0.5 A$ (Figure 2)

Note 1: Pulse test — 80μs to 300μs, 1% duty cycle

Refer to VPMH10 Design Curves (See Section 4)

TEST CIRCUITS

FIGURE 1. Switching Test Circuit

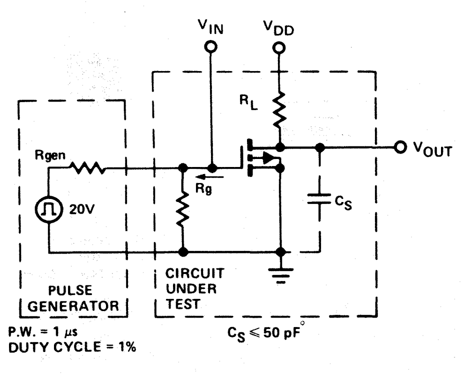


FIGURE 2. Reverse Recovery Test Circuit

50 Ω
di/dt Adjust (1 - 27 μH)
.5 TO 50μF
$I_{(PK)}$ Adjust
IN4933
240 Ω
4000μF
IN4001
R ≤ 0.25 Ω
L ≤ 0.01μH
IN4723
2N4204
SCOPE
FROM TRIGGER CKT

MOSPOWER

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N-/P-Channel 2
Multi-Channel 3
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Worldwide Sales Offices 8

VQ1000P ■ VQ1000J

60V N-Channel Enhancement Mode Quad MOSPOWER Array

This power FET is designed especially for low power high frequency inverters, interface to CMOS and TTL logic, line drivers and Analog Switching.

FEATURES

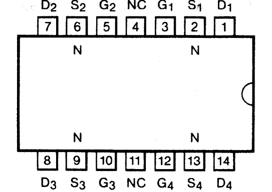
- High Input Impedance
- Extremely Fast Switching
- Rugged
- Internal Drain-Source Diode
- Dual-In-Line Package for Packing Density and Automatic Insertion

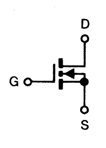
BENEFITS

- Reduced Component Count
- Simpler Designs
  — Directly Interfaces CMOS & TTL
- Improved Circuit Performance
- Increased Reliability

Product Summary

Part Number	BV_{DSS} (Volts)	$R_{DS(ON)}$ (Ohms)	Package
VQ1000P	60	5.5	Side Braze
VQ1000J	60	5.5	Plastic





TOP VIEW
ORDER NUMBER: VQ1000P, VQ1000J

ABSOLUTE MAXIMUM RATINGS (T_A=25°C unless otherwise noted)

Drain-Source Voltage 60V

Drain-Gate Voltage 60V

Drain Current
- Continuous[1] .... ±225mA
- Pulsed[1,2] .... ±1A

Gate-Source Voltage .... ±40V

Gate Current Peak .... ±1A

Power Dissipation
- Single 1.30W
- Quad 2W

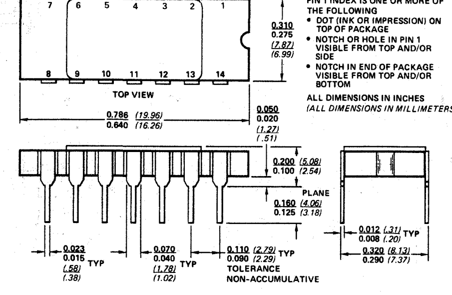
Linear Derating Factor
- Single .... 10.4mW/°C
- Quad .... 16mW/°C

Operating and Storage Temperature .... −55°C to +150°C

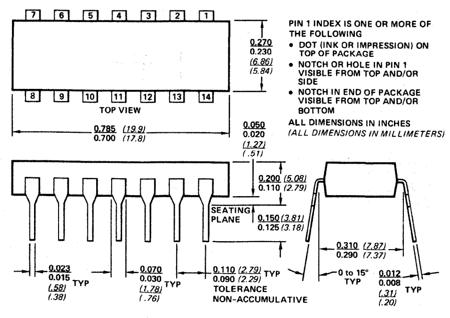
Lead Temperature (1/16″ from case for 10 secs) .... +300°C

Note: 1: Single device alone. Package limited.
Note: 2: Pulse test: 80μs to 300μs, 1% duty cycle.

PACKAGE DIMENSIONS



14-LEAD DUAL-IN-LINE PACKAGE (P) (SIDE BRAZE)



14-LEAD DUAL-IN-LINE PACKAGE (J) (PLASTIC)

ELECTRICAL CHARACTERISTICS ($T_A = 25°C$ unless otherwise noted)

	Parameter	Min	Max	Unit	Test Conditions
		Static			
BV_{DSS}	Drain-Source Breakdown	60		V	$V_{GS}=0$, $I_D=100\mu A$
$V_{GS(th)}$	Gate Threshold Voltage	0.8	2.5	V	$V_{DS}=V_{GS}$, $I_D=1mA$
I_{GSS}	Gate Body Leakage		100	nA	$V_{GS}=10V$, $V_{DS}=0$
			500		$V_{GS}=10V$, $V_{DS}=0$, $T_A=125°C$
I_{DSS}	Zero Gate Voltage Drain Current		10	μA	$V_{GS}=0$, $V_{DS}=48V$
			500		$V_{GS}=0$, $V_{DS}=48V$, $T_A=125°C$
$V_{DS(on)}$	Drain-Source Saturation Voltage[1]		1.5	V	$V_{GS}=5V$, $I_D=0.2A$
			1.65		$V_{GS}=10V$, $I_D=0.3A$
$r_{DS(on)}$	Drain-Source On Resistance[1]		7.5	Ω	$V_{GS}=5V$, $I_D=0.2A$
			5.5		$V_{GS}=10V$, $I_D=0.3A$
$I_{D(on)}$	On-State Drain Current[1]	0.2		A	$V_{DS}=15V$, $V_{GS}=5V$
		0.5			$V_{DS}=15V$, $V_{GS}=10V$
		Dynamic			
g_{fs}	Forward Transconductance[1]	100		mS	$V_{DS}=15V$, $I_D=0.5A$
C_{iss}	Input Capacitance		60	pF	$V_{DS}=25V$, $V_{GS}=0$, $f=1MHz$
C_{rss}	Reverse Transfer Capacitance		5		
C_{oss}	Common-Source Output Capacitance		25		
t_{ON}	Turn-ON Time		10	ns	$V_{DD}=15V$, $R_L=23\Omega$, $R_g=25\Omega$, $I_D \approx 0.6A$ (Figure 1)
t_{OFF}	Turn-OFF Time		10		
		Drain-Source Diode Characteristics			
		Typ			
V_{SD}	Forward ON Voltage[1]	−0.85		V	$I_S=-0.5A$, $V_{GS}=0$
t_{rr}	Reverse Recovery Time	165		ns	$I_F=I_R=0.3A$, $V_{GS}=0$ (Figure 2)

Note 1: Pulse test — 80μs to 300μs, 1% duty cycle

Refer to VNML Design Curves (See Section 4)

TEST CIRCUITS

FIGURE 1. Switching Test Circuit

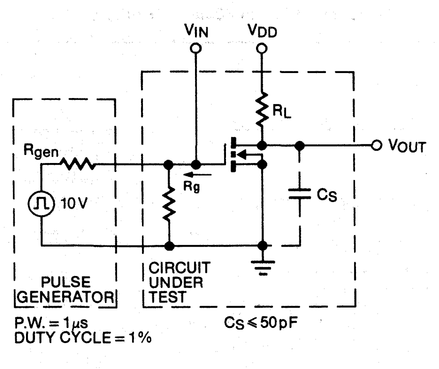
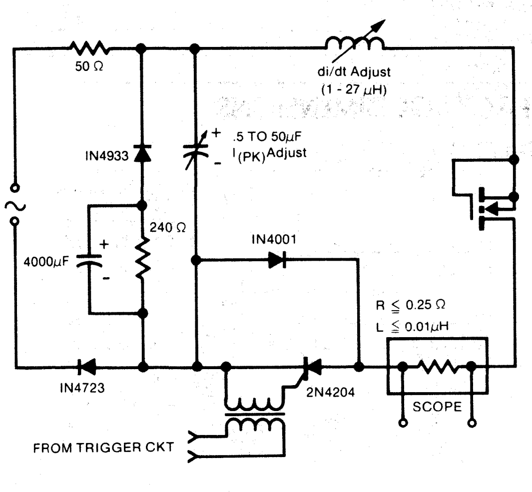


FIGURE 2. JEDEC Reverse Recovery Circuit



VQ1001P ■ VQ1001J

Siliconix

30V N-Channel Enhancement Mode Quad MOSPOWER Array

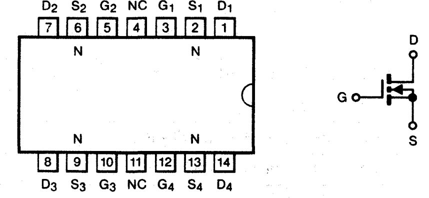
This power FET is designed especially for low power high frequency inverters, interface to CMOS and TTL logic, line drivers and Analog Switching.

FEATURES
- High Input Impedance
- Extremely Fast Switching
- Rugged
- Internal Drain-Source Diode
- Dual-In-Line Package for Packing Density and Automatic Insertion

BENEFITS
- Reduced Component Count
- Simpler Designs
  — Directly Interfaces CMOS & TTL
- Improved Circuit Performance
- Increased Reliability

Product Summary

Part Number	BV_{DSS} (Volts)	$R_{DS(ON)}$ (Ohms)	Package
VQ1001P	30	1	Side Braze
VQ1001J	30	1	Plastic



TOP VIEW
ORDER NUMBER: VQ1001P, VQ1001J

ABSOLUTE MAXIMUM RATINGS (T_A=25°C unless otherwise noted)

Drain-Source Voltage....................30V

Drain-Gate Voltage......................30V

Drain Current
 Continuous[1]..................... ±850mA
 Pulsed[1,2]............................ ±3A

Gate-Source Voltage.................. ±40V

Power Dissipation
 Single.............................1.30W
 Quad..................................2W

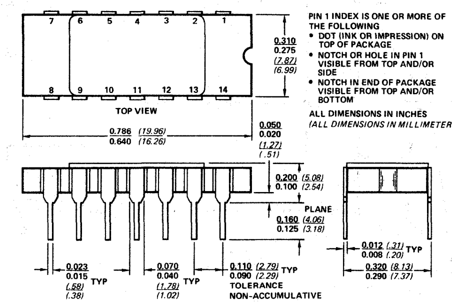
Linear Derating Factor
 Single.........................10.4mW/°C
 Quad.............................16mW/°C

Operating and Storage
 Temperature.................−55°C to +150°C

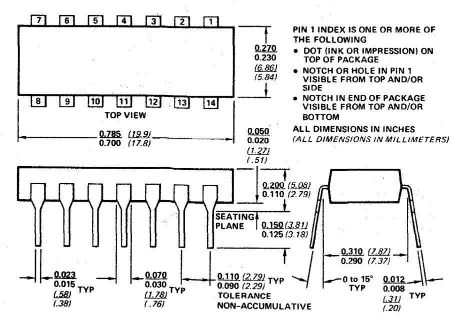
Lead Temperature
 (1/16″ from case for 10 secs)..........+300°C

Note 1: Single device alone. Package limited.
Note 2: Pulse test: 80μs to 300μs, 1% duty cycle.

PACKAGE DIMENSIONS



14-LEAD DUAL-IN-LINE PACKAGE (P)
(SIDE BRAZE)



14-LEAD DUAL-IN-LINE PACKAGE (J)
(PLASTIC)

ELECTRICAL CHARACTERISTICS ($T_A = 25°C$ unless otherwise noted)

Symbol	Parameter	Min	Max	Unit	Test Conditions
Static					
BV_{DSS}	Drain-Source Breakdown	30		V	$V_{GS} = 0$, $I_D = 10\mu A$
$V_{GS(th)}$	Gate Threshold Voltage	0.8	2.5	V	$V_{DS} = V_{GS}$, $I_D = 1mA$
I_{GSS}	Gate Body Leakage		100	nA	$V_{GS} = 16V$, $V_{DS} = 0$
			500	nA	$V_{GS} = 16V$, $V_{DS} = 0$, $T_A = 125°C$
I_{DSS}	Zero Gate Voltage Drain Current		10	μA	$V_{GS} = 0$, $V_{DS} = 30V$
			500	μA	$V_{GS} = 0$, $V_{DS} = 30V$, $T_A = 125°C$
$V_{DS(on)}$	Drain-Source Saturation Voltage[1]		0.35	V	$V_{GS} = 5V$, $I_D = 0.2A$
			1.0	V	$V_{GS} = 12V$, $I_D = 1A$
$r_{DS(on)}$	Drain-Source On Resistance[1]		1.0	Ω	$V_{GS} = 12V$, $I_D = 1A$
$I_{D(on)}$	On-State Drain Current[1]	2.0		A	$V_{GS} = 12V$, $V_{DS} = 15V$
Dynamic					
g_{fs}	Forward Transconductance[1]	250		mS	$V_{DS} = 15V$, $I_D = 500mA$
C_{iss}	Input Capacitance		100	pF	$V_{DS} = 15V$, $V_{GS} = 0$, $f = 1MHz$
C_{rss}	Reverse Transfer Capacitance		55	pF	$V_{DS} = 15V$, $V_{GS} = 0$, $f = 1MHz$
C_{oss}	Common-Source Output Capacitance		80	pF	$V_{DS} = 15V$, $V_{GS} = 0$, $f = 1MHz$
t_{ON}	Turn-ON Time		30	ns	$V_{DD} = 15V$, $R_L = 24\Omega$, $R_g = 25\Omega$, $I_D \approx 0.6A$ (Figure 1)
t_{OFF}	Turn-OFF Time		30	ns	$V_{DD} = 15V$, $R_L = 24\Omega$, $R_g = 25\Omega$, $I_D \approx 0.6A$ (Figure 1)
Drain-Source Diode Characteristics					
		Typ			
V_{SD}	Forward ON Voltage[1]	−0.9		V	$V_{GS} = 0$, $I_S = -0.5A$
t_{rr}	Reverse Recovery Time	50		ns	$I_F = I_R = 0.5A$ (Figure 2)

Note 1: Pulse test — 80μs to 300μs, 1% duty cycle

Refer to VNMH03 Design Curves (See Section 4)

TEST CIRCUITS

FIGURE 1. Switching Test Circuit

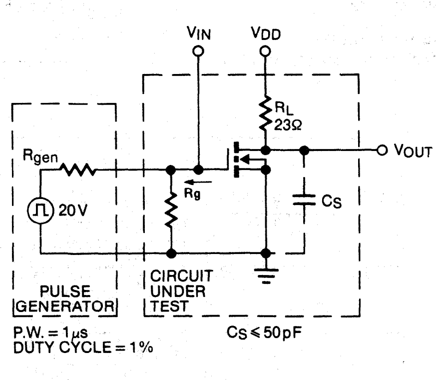
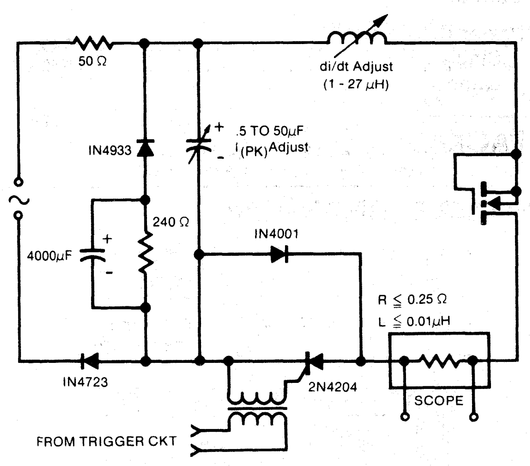


FIGURE 2. JEDEC Reverse Recovery Circuit



VQ1004P ■ VQ1004J ■ VQ1006P ■ VQ1006J

90V N-Channel Enhancement Mode Quad MOSPOWER Array

This power FET is designed especially for low power high frequency inverters, interface to CMOS and TTL logic, line drivers and Analog Switching.

FEATURES

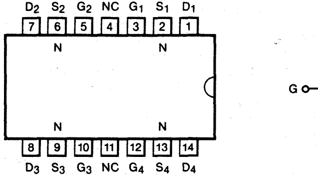
- High Input Impedance
- Extremely Fast Switching
- Rugged — Dissipation Limited SOA
- Internal Drain-Source Diode
- Dual-In-Line Package for Packing Density and Automatic Insertion

BENEFITS

- Reduced Component Count
- Simpler Designs
  — Directly Interfaces CMOS & TTL
- Improved Circuit Performance
- Increased Reliability

Product Summary

Part Number	Package	$R_{DS(on)}$	I_D	BV_{DSS}
VQ1004P	14 Pin DIP, Side Braze	3.5Ω	0.46A	60V
VQ1004J	14 Pin DIP, Plastic			
VQ1006P	14 Pin DIP, Side Braze	4.5Ω	0.40A	90V
VQ1006J	14 Pin DIP, Plastic			



TOP VIEW

ORDER NUMBER: VQ1004P, VQ1004J, VQ1006P, VQ1006J

ABSOLUTE MAXIMUM RATINGS (T_A=25°C unless otherwise noted)

Drain-Source Voltage
- VQ1004P, J 60V
- VQ1006P, J 90V

Drain-Gate Voltage
- VQ1004P, J 60V
- VQ1006P, J 90V

Gate Current (Peak) .... ±1A

Gate-Source Voltage .... ±40V

Drain Current Continuous[1]
- VQ1004P, J .... ±0.46A
- VQ1006P, J .... ±0.40A

Drain Current Pulsed[2] .... ±2A

Power Dissipation
- Single 1.30W
- Quad 2W

Linear Derating Factor
- Single .... 10.4mW/°C
- Quad .... 16mW/°C

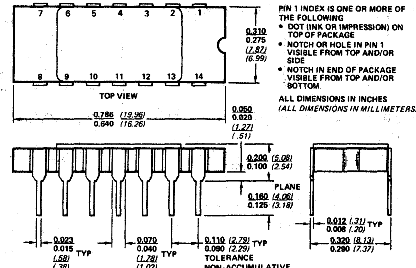
Thermal Resistance
- Single .... 96.2°C/W
- Quad .... 62.5°C/W

Operating and Storage Temperature .... −55°C to +150°C

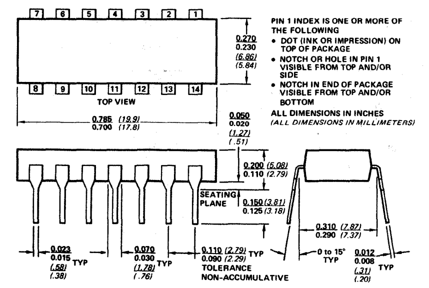
Lead Temperature (1/16″ from case for 10 secs) .... +300°C

Note 1: Single device alone. Package limited.
Note 2: Pulse test: 80μs to 300μs, 1% duty cycle.

PACKAGE DIMENSIONS



14-LEAD DUAL-IN-LINE PACKAGE (P) (SIDE BRAZE)



14-LEAD DUAL-IN-LINE PACKAGE (J) (PLASTIC)

ELECTRICAL CHARACTERISTICS ($T_A = 25°C$ unless otherwise noted)

Symbol	Parameter	Part Number	Min	Max	Unit	Test Conditions
		Static				
BV_{DSS}	Drain-Source Breakdown	VQ1004	60		V	$V_{GS} = 0$, $I_D = 10\mu A$
		VQ1006	90			
$V_{GS(th)}$	Gate-Source Threshold Voltage	All	0.8	2.5	V	$V_{DS} = V_{GS}$, $I_D = 1 mA$
I_{GSS}	Gate Body Leakage	All		100	nA	$V_{GS} = 15V$, $V_{DS} = 0$
				500		$V_{GS} = 15V$, $V_{DS} = 0$, $T_A = 125°C$
I_{DSS}	Zero Gate Voltage Drain Current	All		1	μA	$V_{GS} = 0$, $V_{DS} = 0.8$ Max Rating
				500		$V_{GS} = 0$, $V_{DS} = 0.8$ Max Rating, $T_A = 125°C$
$V_{DS(on)}$	Drain-Source Saturation Voltage[1]	All		1.5	V	$V_{GS} = 5V$, $I_D = 0.3A$
		VQ1004		3.5		$V_{GS} = 10V$, $I_D = 1A$
		VQ1006		4.5		
$r_{DS(on)}$	Drain-Source On Resistance[1]	All		5	Ω	$V_{GS} = 5V$, $I_D = 0.3A$
		VQ1004		3.5		$V_{GS} = 10V$, $I_D = 1A$
		VQ1006		4.5		
$I_{D(on)}$	On-State Drain Current[1]	All	1.5		A	$V_{GS} = 10V$, $V_{DS} = 25V$
		Dynamic				
g_{fs}	Forward Transconductance[1]	All	170		mS	$V_{DS} = 25V$, $I_D = 0.5A$
C_{iss}	Input Capacitance	All		60	pF	$V_{DS} = 25V$, $V_{GS} = 0$, $f = 1 MHz$
C_{rss}	Reverse Transfer Capacitance	All		10		
C_{oss}	Common-Source Output Capacitance	All		50		
t_{ON}	Turn-ON Time	All		10	ns	$V_{DD} = 25V$, $R_L = 23Ω$, $R_g = 25Ω$, $I_D \approx 1A$
t_{OFF}	Turn-OFF Time	All		10		
		Drain-Source Diode Characteristics				
			Typ			
V_{SD}	Forward ON Voltage[1]	All	−0.9		V	$V_{GS} = 0$, $I_S = -1A$
t_{rr}	Reverse Recovery Time	All	35		ns	$V_{GS} = 0$, $I_F = I_R = 1A$

Note 1: Pulse test — 80μs to 300μs, 1% duty cycle

TEST CIRCUITS

FIGURE 1. Switching Test Circuit

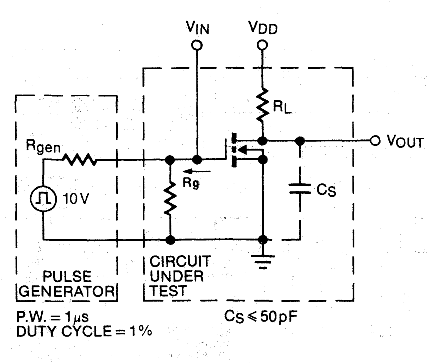
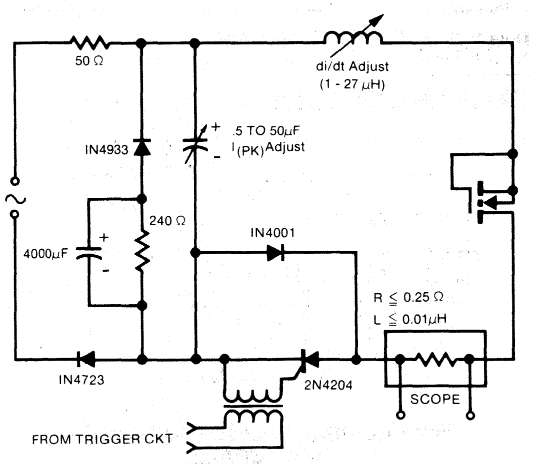


FIGURE 2. JEDEC Reverse Recovery Circuit



VQ2001P ■ VQ2001J

Siliconix

30V P-Channel Enhancement Mode Quad MOSPOWER Array

This power FET is designed especially for low power high frequency inverters, interface to CMOS and TTL logic, line drivers and Analog Switching.

FEATURES

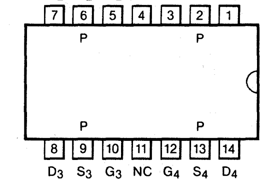
- **High Input Impedance**
- **Extremely Fast Switching**
- **Rugged**
- **Internal Drain-Source Diode**
- **Dual-In-Line Package for Packing Density and Automatic Insertion**

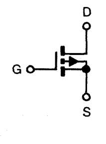
BENEFITS

- **Reduced Component Count**
- **Simpler Designs**
- **Improved Circuit Performance**
- **Increased Reliability**

Product Summary

Part Number	BV_{DSS} (Volts)	$R_{DS(ON)}$ (Ohms)	Package
VQ2001P	−30	2	Side Braze
VQ2001J	−30	2	Plastic





TOP VIEW
ORDER NUMBER: VQ2001P, VQ2001J

ABSOLUTE MAXIMUM RATINGS ($T_A = 25°C$ unless otherwise noted)

Drain-Source Voltage . . . . −30V

Drain-Gate Voltage . . . . −30V

Drain Current
- Continuous[1] . . . . ±600mA
- Pulsed[1,2] . . . . ±2A

Gate-Source Voltage . . . . ±40V

Power Dissipation
- Single 1.30W
- Quad 2W

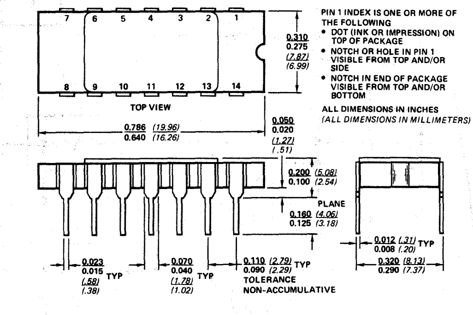
Linear Derating Factor
- Single . . . . 10.4mW/°C
- Quad . . . . 16mW/°C

Operating and Storage Temperature . . . . −55°C to +150°C

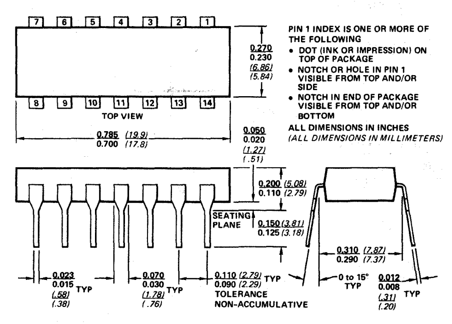
Lead Temperature (1/16″ from case for 10 secs) . . . . +300°C

Note 1: Single device alone. Package limited.
Note 2: Pulse test: 80μs to 300μs, 1% duty cycle.

PACKAGE DIMENSIONS



14-LEAD DUAL-IN-LINE PACKAGE (P) (SIDE BRAZE)



14-LEAD DUAL-IN-LINE PACKAGE (J) (PLASTIC)

ELECTRICAL CHARACTERISTICS ($T_A = 25°C$ unless otherwise noted)

	Parameter	Min	Max	Unit	Test Conditions
	Static				
BV_{DSS}	Drain-Source Breakdown	−30		V	$V_{GS} = 0$, $I_D = -10\mu A$
$V_{GS(th)}$	Gate Threshold Voltage	−2	−4.5	V	$V_{DS} = V_{GS}$, $I_D = -1mA$
I_{GSS}	Gate Body Leakage		−100	nA	$V_{GS} = -16V$, $V_{DS} = 0$
			−500		$V_{GS} = -16V$, $V_{DS} = 0$, $T_A = 125°C$
I_{DSS}	Zero Gate Voltage Drain Current		−10	μA	$V_{GS} = 0$, $V_{DS} = -30V$
			−500		$V_{GS} = 0$, $V_{DS} = -30V$, $T_A = 125°C$
$V_{DS(on)}$	Drain-Source Saturation Voltage[1]		−2	V	$V_{GS} = -12V$, $I_D = -1A$
$r_{DS(on)}$	Drain-Source On Resistance[1]		2	Ω	$V_{GS} = -12V$, $I_D = -1A$
$I_{D(on)}$	On-State Drain Current[1]	−1.5		A	$V_{GS} = -12V$, $V_{DS} = -15V$
	Dynamic				
g_{fs}	Forward Transconductance[1]	200		mS	$V_{DS} = -15V$, $I_D = -500mA$
C_{iss}	Input Capacitance		150	pF	$V_{DS} = -15V$, $V_{GS} = 0$, $f = 1MHz$
C_{rss}	Reverse Transfer Capacitance		60		
C_{oss}	Common-Source Output Capacitance		100		
t_{ON}	Turn-ON Time		30	ns	$V_{DD} = -15V$, $R_L = 23\Omega$, $R_g = 25\Omega$, $I_D \approx -0.6A$ (Figure 1)
t_{OFF}	Turn-OFF Time		30		
	Drain-Source Diode Characteristics				
		Typ			
V_{SD}	Forward ON Voltage[1]	0.9		V	$V_{GS} = 0$, $I_S = 0.5A$
t_{rr}	Reverse Recovery Time	65		ns	$V_{GS} = 0$, $I_F = I_R = 0.5A$ (Figure 2)

Note 1: Pulse test — 80μs to 300μs, 1% duty cycle

Refer to VPMH03 Design Curves (See Section 4)

TEST CIRCUITS

FIGURE 1. Switching Test Circuit

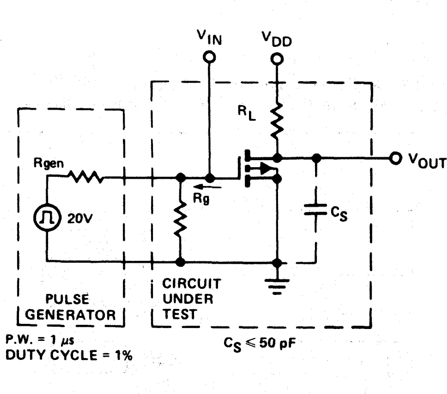
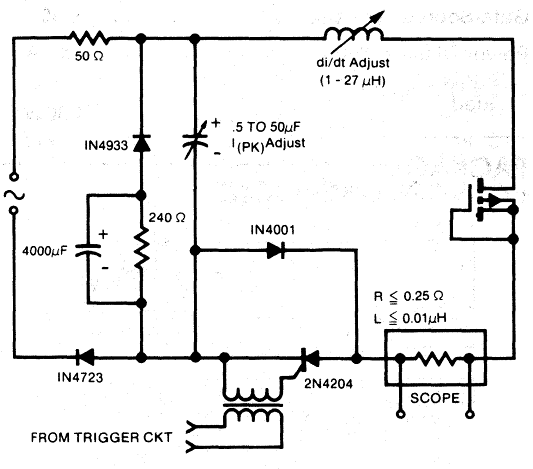


FIGURE 2. Reverse Recovery Test Circuit



VQ2006P ■ VQ2006J

90V P-Channel Enhancement Mode Quad MOSPOWER Array

This power FET is designed especially for low power high frequency inverters, interface to CMOS and TTL logic, line drivers and Analog Switching.

FEATURES

- High Input Impedance
- Extremely Fast Switching
- Rugged
- Internal Drain-Source Diode
- Dual-In-Line Package for Packing Density and Automatic Insertion

BENEFITS

- Reduced Component Count
- Simpler Designs
- Improved Circuit Performance
- Increased Reliability

Product Summary

Part Number	BV_{DSS} (Volts)	$R_{DS(ON)}$ (Ohms)	Package
VQ2006P	−90	5	Side Braze
VQ2006J	−90	5	Plastic

D_2 S_2 G_2 NC G_1 S_1 D_1
7 6 5 4 3 2 1
P P
P P
8 9 10 11 12 13 14
D_3 S_3 G_3 NC G_4 S_4 D_4
D G S

TOP VIEW

ORDER NUMBER: VQ2006P, VQ2006J

ABSOLUTE MAXIMUM RATINGS (T_A=25°C unless otherwise noted)

Drain-Source Voltage . . . . −90 V

Drain-Gate Voltage . . . . −90 V

Drain Current
- Continuous[1] . . . . ±410 mA
- Pulsed[1,2] . . . . ±3.0 A

Gate-Source Voltage . . . . ±40 V

Gate Current Peak . . . . ±1 A

Power Dissipation
- Single . . . . 1.30 W
- Quad . . . . 2 W

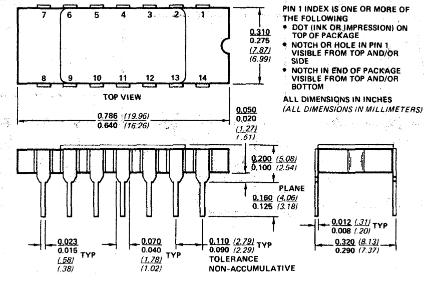
Linear Derating Factor
- Single . . . . 10.4 mW/°C
- Quad . . . . 16 mW/°C

Operating and Storage Temperature . . . . −55°C to +150°C

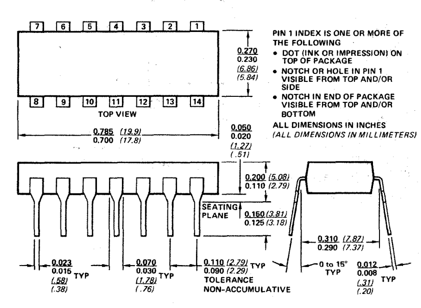
Lead Temperature (1/16″ from case for 10 secs) . . . . +300°C

Note 1: Single device alone. Package limited.
Note 2: Pulse test: 80μs to 300μs, 1% duty cycle.

PACKAGE DIMENSIONS



14-LEAD DUAL-IN-LINE PACKAGE (P) (SIDE BRAZE)



14-LEAD DUAL-IN-LINE PACKAGE (J) (PLASTIC)

ELECTRICAL CHARACTERISTICS (T_A=25°C unless otherwise noted)

	Parameter	Min	Max	Unit	Test Conditions
	Static				
BV_{DSS}	Drain-Source Breakdown	−90		V	$V_{GS}=0$, $I_D=-10\mu A$
$V_{GS(th)}$	Gate Threshold Voltage	−2.0	−4.5	V	$V_{DS}=V_{GS}$, $I_D=-1mA$
I_{GSS}	Gate Body Leakage		−100	nA	$V_{GS}=-30V$, $V_{DS}=0$
			−500	nA	$V_{GS}=-30V$, $V_{DS}=0$, $T_A=125°C$
I_{DSS}	Zero Gate Voltage Drain Current		−10	μA	$V_{GS}=0$, $V_{DS}=-90V$
			−500	μA	$V_{GS}=0$, $V_{DS}=-90V$, $T_A=125°C$
$V_{DS(on)}$	Drain-Source Saturation Voltage[1]		−5.0	V	$V_{GS}=-10V$, $I_D=-1A$
$r_{DS(on)}$	Drain-Source On Resistance[1]		5.0	Ω	$V_{GS}=-10V$, $I_D=-1A$
$I_{D(on)}$	On-State Drain Current[1]	−1.0		A	$V_{GS}=-10V$, $V_{DS}=-15V$
	Dynamic				
g_{fs}	Forward Transconductance[1]	200		mS	$V_{DS}=-25V$, $I_D=-500mA$
C_{iss}	Input Capacitance		150	pF	$V_{DS}=-25V$, $V_{GS}=0$, $f=1MHz$
C_{rss}	Reverse Transfer Capacitance		20	pF	$V_{DS}=-25V$, $V_{GS}=0$, $f=1MHz$
C_{oss}	Common-Source Output Capacitance		60	pF	$V_{DS}=-25V$, $V_{GS}=0$, $f=1MHz$
t_{ON}	Turn-ON Time		15	ns	$V_{DD}=-25V$, $R_L=23\Omega$, $R_g=25\Omega$, $I_D\approx-1A$ (Figure 1)
t_{OFF}	Turn-OFF Time		15	ns	$V_{DD}=-25V$, $R_L=23\Omega$, $R_g=25\Omega$, $I_D\approx-1A$ (Figure 1)
	Drain-Source Diode Characteristics				
		Typ			
V_{SD}	Forward ON Voltage[1]	0.9		V	$V_{GS}=0$, $I_S=0.5A$
t_{rr}	Reverse Recovery Time	65		ns	$V_{GS}=0$, $I_F=I_R=0.5A$ (Figure 2)

Note 1: Pulse test — 80μs to 300μs, 1% duty cycle

Refer to VPMH10 Design Curves (See Section 4)

TEST CIRCUITS

FIGURE 1. Switching Test Circuit

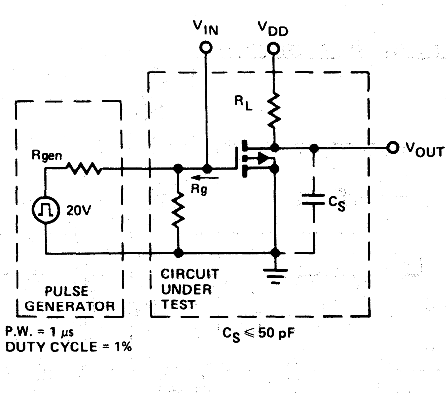
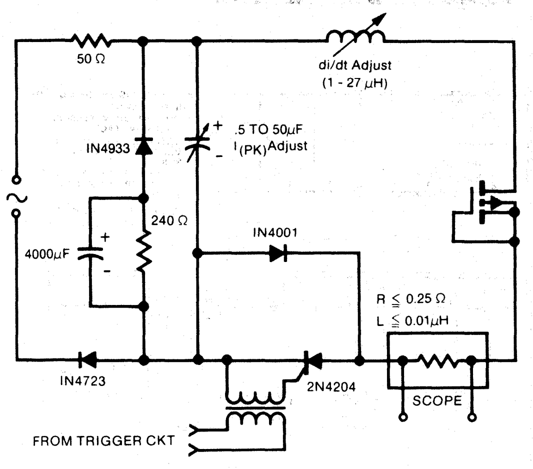


FIGURE 2. JEDEC Reverse Recovery Circuit



VQ7254P ■ VQ7254J

Siliconix

20V Quad N- and P-Channel Enhancement Mode MOSPOWER

This power FET is designed especially for low power high frequency inverters, interface to CMOS and TTL logic, line drivers, Analog Switching and X and Y coils of bubble memories.

FEATURES

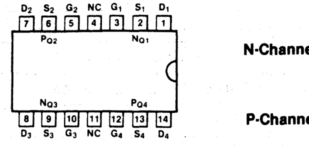
- High Input Impedance
- Extremely Fast Switching
- Rugged
- Internal Drain-Source Diode

BENEFITS

- Reduced Component Count
- Simpler Designs
  - — Directly Interfaces CMOS & TTL
- Improved Circuit Performance
- Increased Reliability

Product Summary

Part Number	BV_{DSS} (Volts)	$R_{DS(ON)}$ Sum	Package
VQ7254P	20	3Ω	Side Braze
VQ7254J	20	3Ω	Plastic



TOP VIEW
ORDER NUMBER: VQ7254P, VQ7254J

ABSOLUTE MAXIMUM RATINGS (T_C=25°C unless otherwise noted)

Drain-Source Voltage[2] 20V

Drain-Gate Voltage[2] 15V

Drain Current
- Continuous[1,2] 2A
- Pulsed 3A

Gate-Source Voltage[2] .... ±40V

Total Power Dissipation @T_A=25°C 1.75W

Total Power Dissipation @T_A=80°C 1.05W

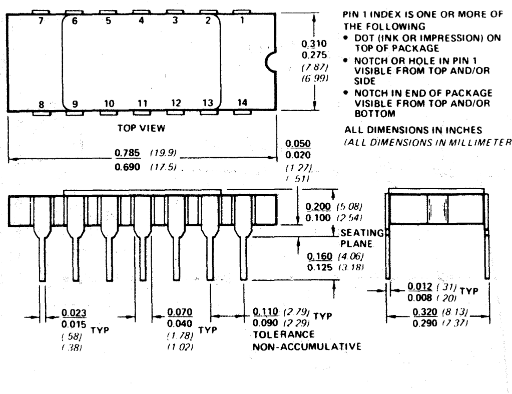
Storage Temperature .... −40°C to +150°C

Temperature Under Bias .... −40°C to +100°C

Lead Temperature
(1/16″ from case for 10 secs) .... +300°C

Note 1: Single device alone. Limited by package dissipation.
Note 2: Reverse polarities for P-Channel.

PACKAGE DIMENSIONS



14-LEAD DUAL-IN-LINE PACKAGE (P) (SIDE BRAZE)

TOP VIEW
0.270 0.230 (6.86) (5.84)
0.785 (19.9) 0.700 (17.8)
0.050 0.020 (1.27) (.51)
0.200 (5.08) 0.110 (2.79)
SEATING PLANE
0.150 (3.81) 0.125 (3.18)
0.310 (7.87) 0.290 (7.37)
0 to 15° TYP
0.012 0.008 (.31) (.20) TYP
0.023 0.015 (.58) (.38) TYP
0.070 0.030 (1.78) (.76) TYP
0.110 (2.79) 0.090 (2.29) TYP
TOLERANCE NON-ACCUMULATIVE

14-LEAD DUAL-IN-LINE PACKAGE (J) (PLASTIC)

ELECTRICAL CHARACTERISTICS ($T_A = 25°C$ unless otherwise noted)

Parameter		N-Channel		P-Channel		Unit	Test Conditions (Reverse Polarity for P-Channel)
		Min	Max	Min	Max		
Static							
BV_{DSS}	Drain-Source Breakdown	20		20		V	$V_{GS} = 0$, $I_D = 10\mu A$
$V_{GS(th)}$	Gate-Source Threshold Voltage	0.80		0.80		V	$V_{DS} = V_{GS}$, $I_D = 1mA$, $T_A = 25°C$
$V_{GS(th)}$	Gate-Source Threshold Voltage	0.65		0.65		V	$V_{DS} = V_{GS}$, $I_D = 1mA$, $T_A = 85°C$
I_{GSS}	Gate Body Leakage		100		100	nA	$V_{GS} = 12V$, $V_{DS} = 0$, $T_A = 25°C$
I_{DSS}	Zero Gate Voltage Drain Current		0.5		0.5	μA	$V_{GS} = 0$, $V_{DS} = 20V$, $T_A = 25°C$
$r_{DS(on)}$	On-State Resistance[1]		3 Q_1+Q_2		3 Q_3+Q_4	Ω	$V_{GS} = 11.4V$, $I_D = 1A$
Dynamic							
C_{iss}	Input Capacitance		175		190	pF	$V_{DS} = 12V$, $V_{GS} = 0$, $f = 1MHz$, $T_A = 25°C$
t_{ON}	Turn-ON Time		20		30	ns	$V_{DD} = 17V$, $R_L = 15Ω$, $R_S = 25Ω$, $T_A = 25°C$ (Figure 1)
t_{OFF}	Turn-OFF Time		20		30	ns	$V_{DD} = 17V$, $R_L = 15Ω$, $R_S = 25Ω$, $T_A = 25°C$ (Figure 1)
Drain-Source Diode Characteristics							
		Max		Max			
V_{SD}	Forward ON Voltage	−0.75		0.75		V	$V_{GS} = 0$, $I_F = 50mA$, $T_A = 25°C$
V_{SD}	Forward ON Voltage	−1.20		1.20		V	$V_{GS} = 0$, $I_F = 1A$, $T_A = 25°C$

Note 1: r_{DS} increases 0.6%/°C
Note 2: Pulse test — 80μs to 300μs, 1% duty cycle

TEST CIRCUITS (Reverse Polarity for P-Channel)

FIGURE 1. Switching Time Test Circuit

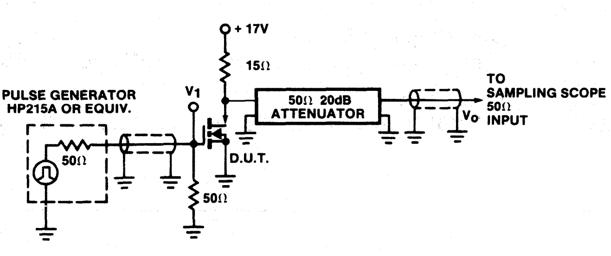
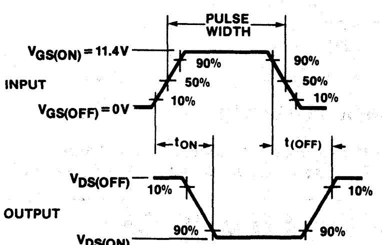


FIGURE 2. Switching Time Test Waveforms



VQ3001P ■ VQ3001J

30V Quad N- and P-Channel Enhancement Mode MOSPOWER

This power FET is designed especially for low power high frequency inverters, interface to CMOS and TTL logic, line drivers and Analog Switching.

FEATURES

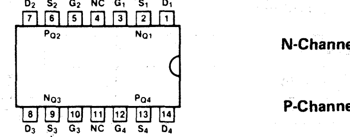
- High Input Impedance
- Extremely Fast Switching
- Rugged
- Internal Drain-Source Diode

BENEFITS

- Reduced Component Count
- Simpler Designs
  - Directly Interfaces CMOS & TTL
- Improved Circuit Performance
- Increased Reliability

Product Summary

Part Number	BV_{DSS} (Volts)	$R_{DS(ON)}$ (Ohms)	Package
VQ3001P	30	1 & 2	Side Braze
VQ3001J	30	1 & 2	Plastic



TOP VIEW
ORDER NUMBER: VQ3001P, VQ3001J

ABSOLUTE MAXIMUM RATINGS (T_C=25°C unless otherwise noted)

Drain-Source Voltage . . . . −30V

Drain-Gate Voltage 30V

Drain Current
- Continuous[1]
  - P-Channel . . . . ±600mA
  - N-Channel . . . . ±850mA
- Pulsed[2]
  - P-Channel . . . . ±2A
  - N-Channel . . . . ±3A

Gate-Source Voltage . . . . ±40V

Power Dissipation
- Single 1.30W
- Quad 2W

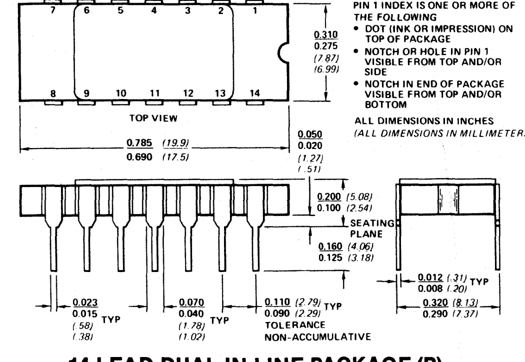
Linear Derating Factor
- Single . . . . 10.4mW/°C
- Quad . . . . 16mW/°C

Operating and Storage Temperature . . . . −55°C to +150°C

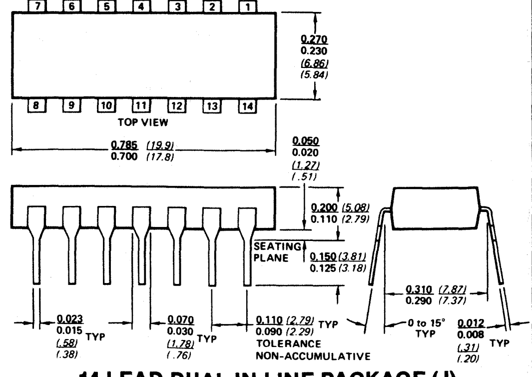
Lead Temperature (1/16″ from case for 10 secs) . . . . +300°C

Note 1: Single device alone. Package limited.
Note 2: Pulse test: 80μs to 300μs, 1% duty cycle.

PACKAGE DIMENSIONS



14-LEAD DUAL-IN-LINE PACKAGE (P) (SIDE BRAZE)



14-LEAD DUAL-IN-LINE PACKAGE (J) (PLASTIC)

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Parameter		N-Channel Min	N-Channel Max	P-Channel Min	P-Channel Max	Unit	Test Conditions (Reverse Polarity for P-Channel)
Static							
BV_{DSS}	Drain-Source Breakdown	30		−30		V	V_{GS} = 0, I_D = 10μA
$V_{GS(th)}$	Gate-Source Threshold Voltage	0.8	2.5	−2	−4.5	V	V_{DS} = V_{GS}, I_D = 1 mA
I_{GSS}	Gate Body Leakage		100		−100	nA	V_{GS} = 16 V, V_{DS} = 0
			500		−500		V_{GS} = 16 V, V_{DS} = 0, T_A = 125°C
I_{DSS}	Zero Gate Voltage Drain Current		10		−10	μA	V_{GS} = 0, V_{DS} = 24 V
			500		−500		V_{GS} = 0, V_{DS} = 24 V, T_A = 125°C
$I_{D(on)}$	On-State Drain Current[1]	2		−1.5		A	V_{GS} = 12 V, V_{DS} = 15 V
V_{DS}	Drain-Source On-State Voltage[1]		0.35			V	V_{GS} = 5 V, I_D = 200 mA
			1		−2		V_{GS} = 12 V, I_D = 1 A
Dynamic							
g_{fs}	Forward Transconductance[1]	250		200		mS	V_{DS} = 15 V, I_D = 500 mA
C_{iss}	Input Capacitance		100		150	pF	V_{DS} = 15 V, V_{GS} = 0, f = 1 MHz
C_{rss}	Reverse Transfer Capacitance		55		60		
C_{oss}	Common-Source Output Capacitance		80		100		
t_{ON}	Turn-ON Time		30		30	ns	V_{DD} = 15 V, R_L = 23Ω, R_g = 25Ω, I_D≈0.6 A (Figure 1)
t_{OFF}	Turn-OFF Time		30		30		
Drain-Source Diode Characteristics							
		N-Channel Typ		P-Channel Typ			
V_{SD}	Forward ON Voltage	−0.72		0.72		V	V_{GS} = 0, I_F = 50 mA
t_{rr}	Reverse Recovery Time	50		65		ns	V_{GS} = 0, I_F = I_R = 0.5 A (Figure 2)

Note 1: Pulse test — 80μs to 300μs, 1% duty cycle

TEST CIRCUITS (Reverse Polarity for P-Channel)

FIGURE 1. Switching Test Circuit

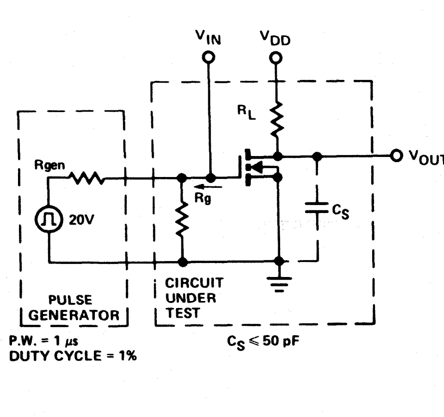
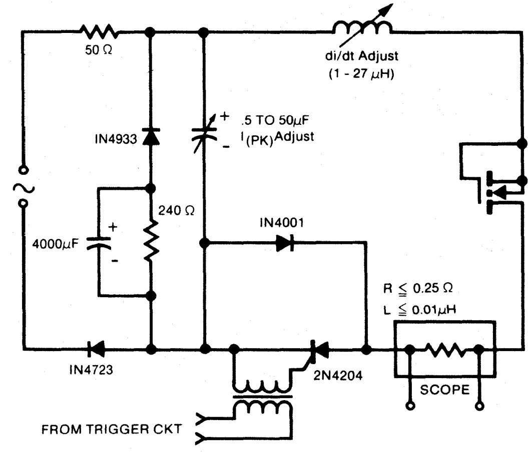
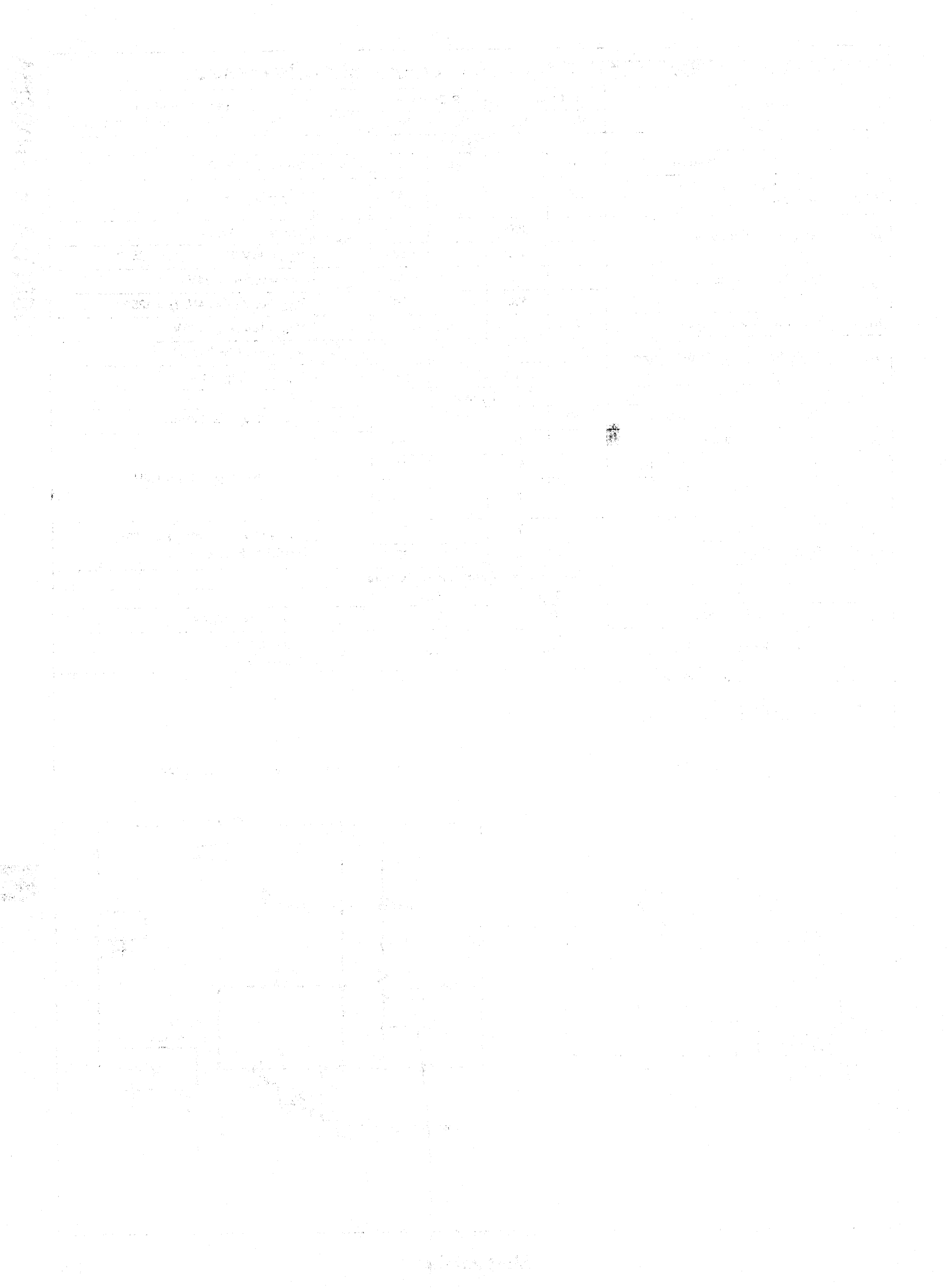


FIGURE 2. Reverse Recovery Test Circuit





MOSPOWER

Introduction 1
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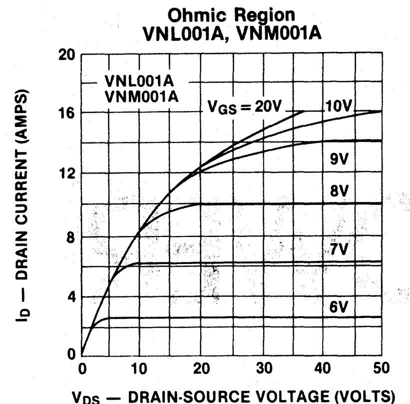
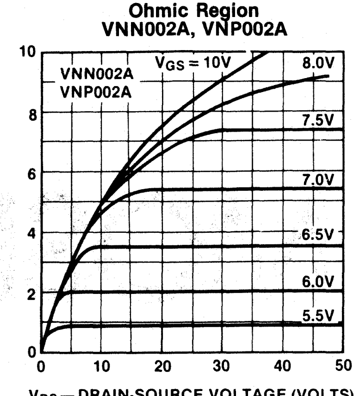
TYPICAL STATIC CHARACTERISTICS

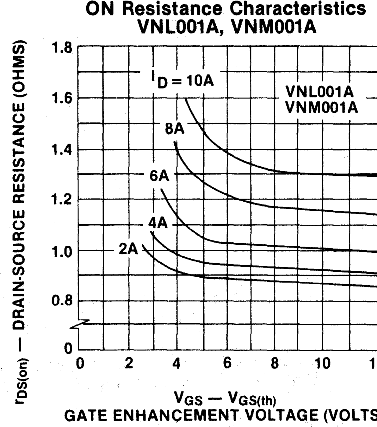
VNDA / 200°C

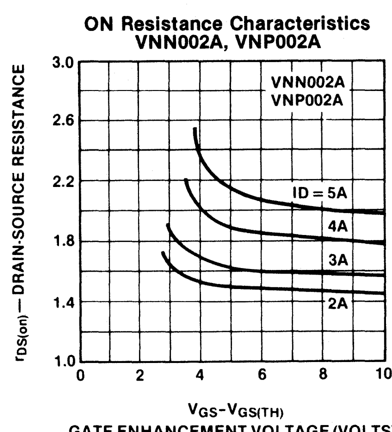
(Pulse width 80μs—300μs, Duty cycle 1%, T_C=25°C)

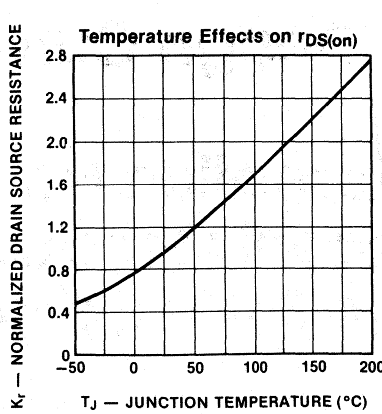
Part Numbers: VNL001A, VNM001A, VNN002A, VNP002A

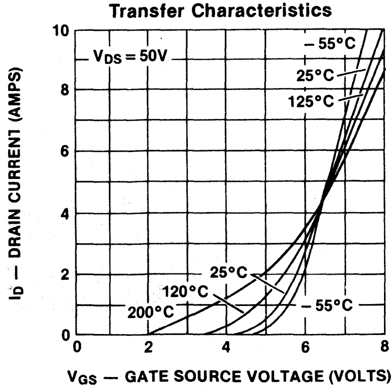






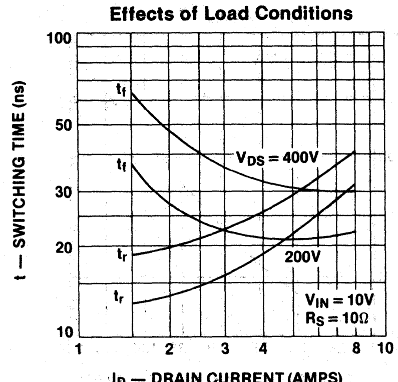




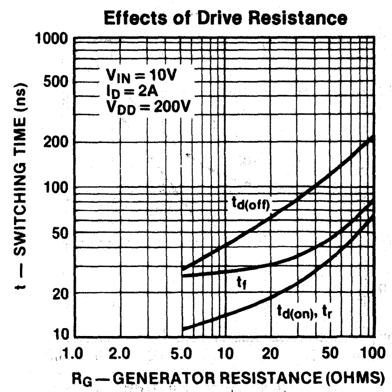


01/83

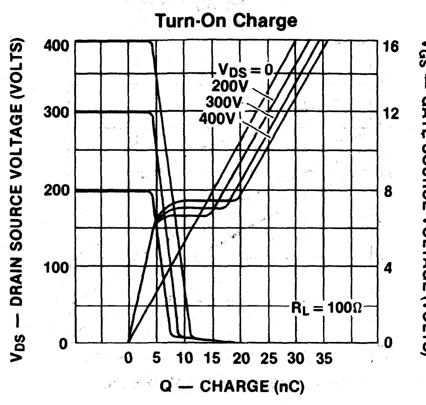
Effects of Load Conditions



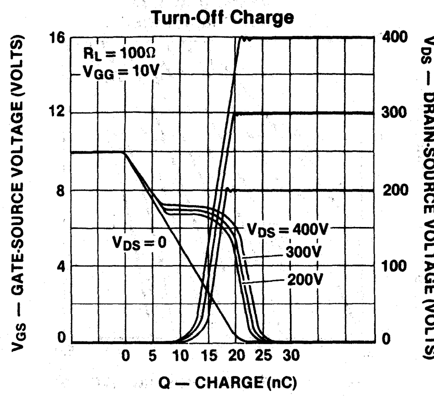
Effects of Drive Resistance



Turn-On Charge



Turn-Off Charge



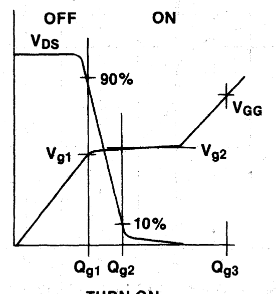
Switching Time Equations

$$t_{d(on)} = \frac{Q_{g1}}{V_{g1}} R_{gen} \ln\left(\frac{V_{GG}}{V_{GG} - V_{g1}}\right)$$

$$t_{d(off)} = \frac{Q_{g3} - Q_{g2}}{V_{GG} - V_{g2}} R_{gen} \ln\left(\frac{V_{GG}}{V_{g2}}\right)$$

$$t_r = \frac{Q_{g2} - Q_{g1}}{V_{g2} - V_{g1}} R_{gen} \ln\left(\frac{V_{GG} - V_{g1}}{V_{GG} - V_{g2}}\right)$$

$$t_f = \frac{Q_{g2} - Q_{g1}}{V_{g2} - V_{g1}} R_{gen} \ln\left(\frac{V_{g2}}{V_{g1}}\right)$$



ON OFF

V_{GG} 90% V_{DS}

V_{g2}

V_{g1}

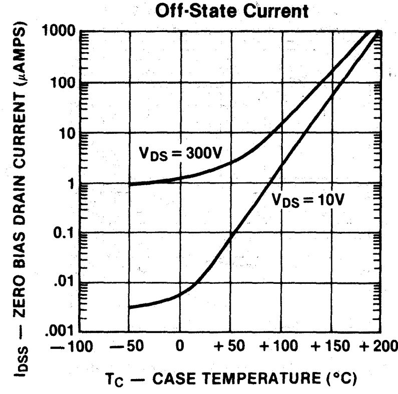
10%

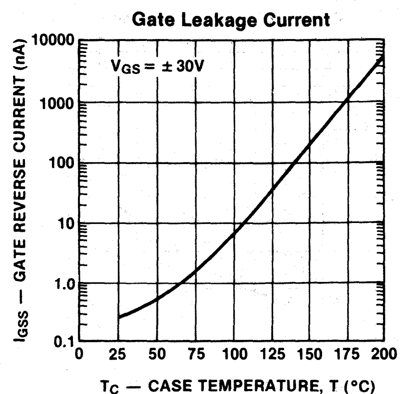
Q_{g3} Q_{g2} Q_{g1}

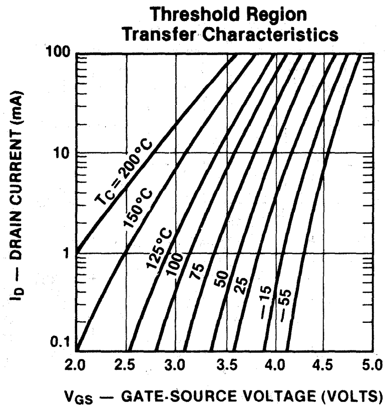
TURN-OFF

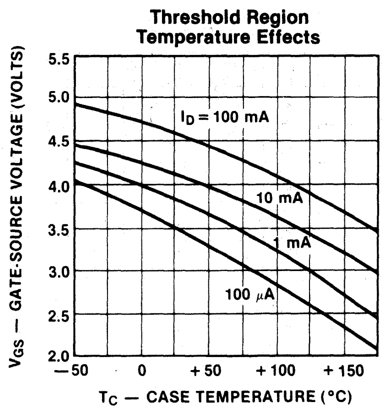
TYPICAL CHARACTERISTICS (Cont'd)

Part Numbers: VNL001A, VNM001A, VNN002A, VNP002A

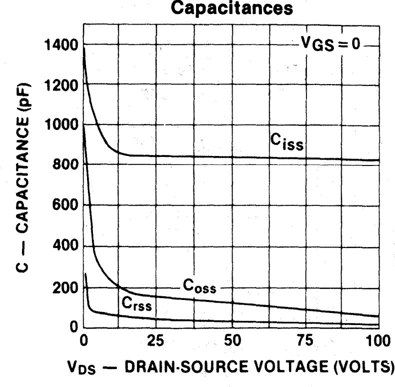


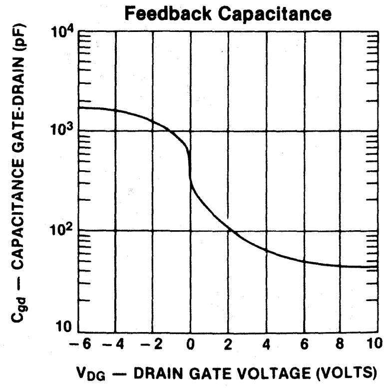






CAPACITANCES (T_C=25°C)



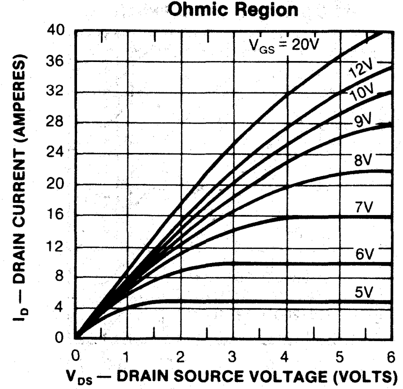


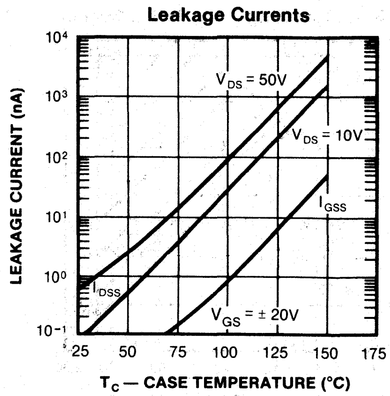
TYPICAL STATIC CHARACTERISTICS

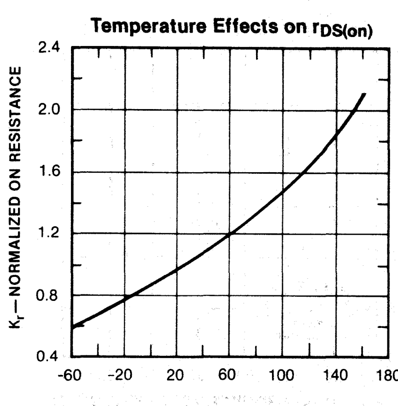
VNDA12

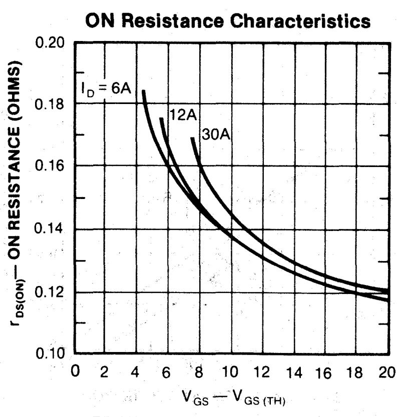
(Pulse width 80μs—300μs, Duty cycle 1%, $T_C = 25°C$)

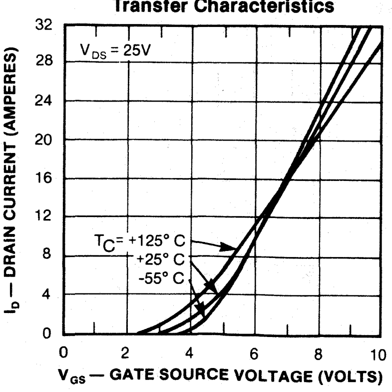
Part Numbers: VN0800A, VN0801A, VN1000A, VN1001A, VN1200A, VN1201A, VN0800D, VN0801D, VN1000D, VN1001D, VN1200D, VN1201D, IRF130, IRF131, IRF132, IRF133, IRF530, IRF531, IRF532, IRF533

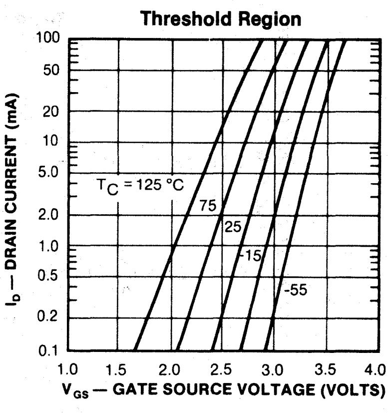












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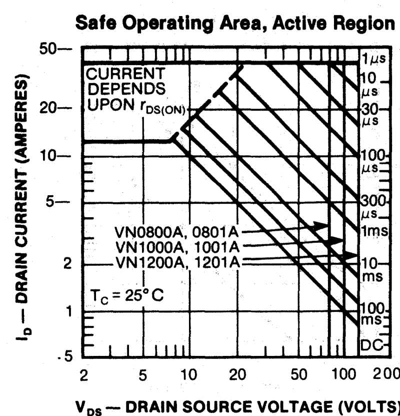
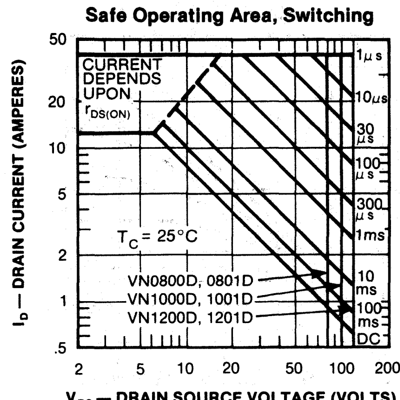
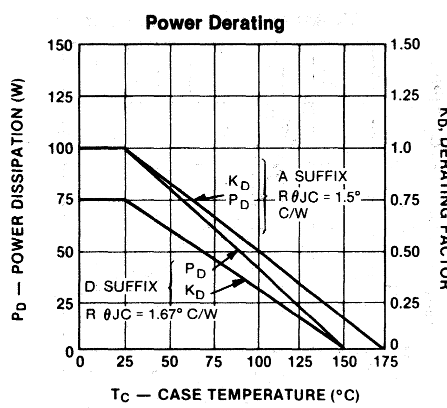
TYPICAL CHARACTERISTICS (Cont'd)

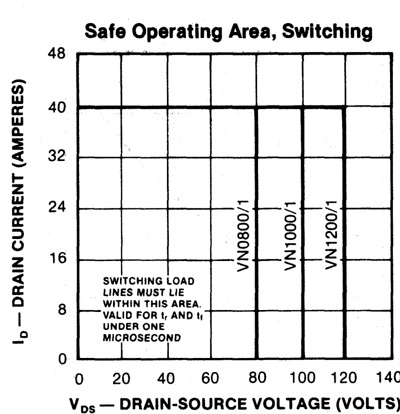
Part Numbers: VN0800A, VN0801A, VN1000A, VN1001A, VN1200A, VN1201A, VN0800D, VN0801D, VN1000D, VN1001D, VN1200D, VN1201D, IRF130, IRF131, IRF132, IRF133, IRF530, IRF531, IRF532, IRF533

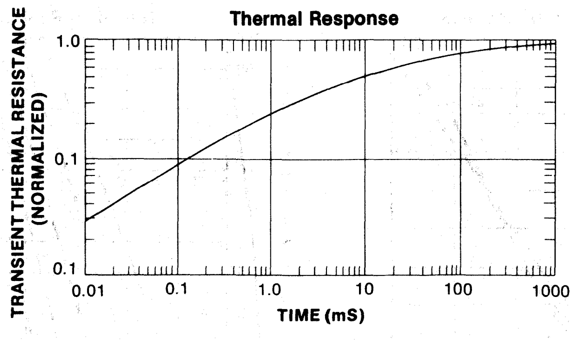
SAFE OPERATING AREA







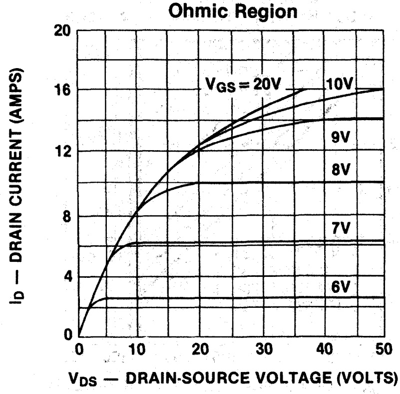


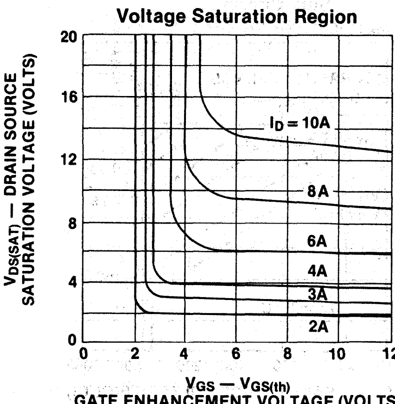


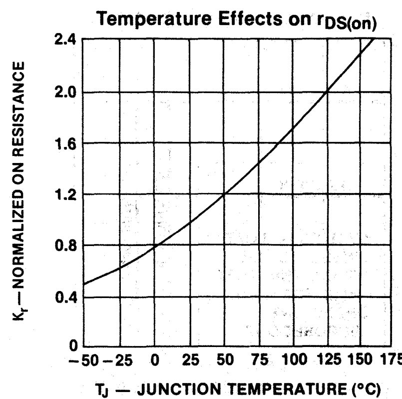
TYPICAL STATIC CHARACTERISTICS

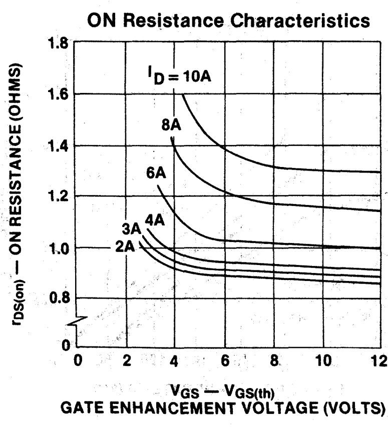
(Pulse width 80μs—300μs, Duty cycle 1%, $T_C = 25°C$)

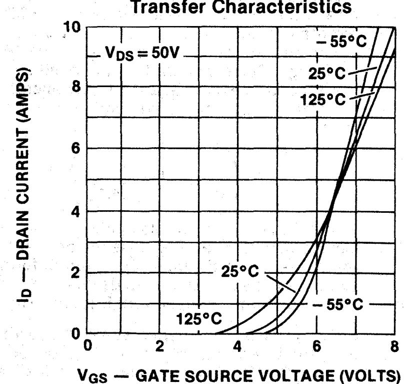
Part Numbers: VN3500A, VN3500D, VN3501A, VN3501D, VN4000A, VN4000D, VN4001A, VN4001D, IRF330, IRF331, IRF332, IRF333, IRF730, IRF731, IRF732, IRF733

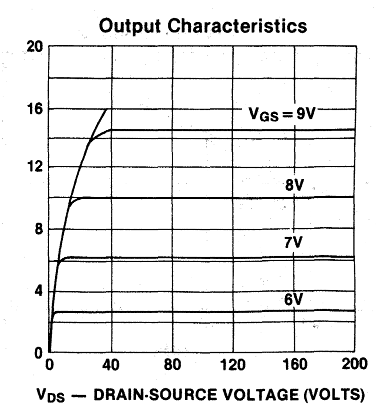












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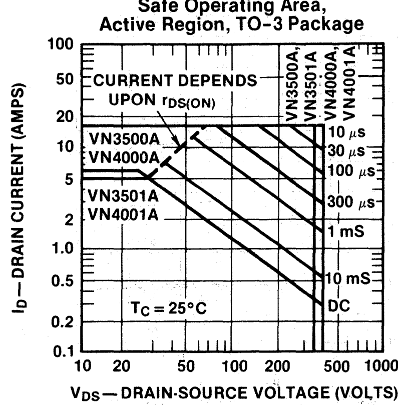
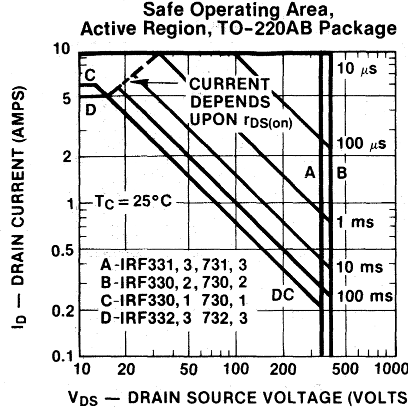
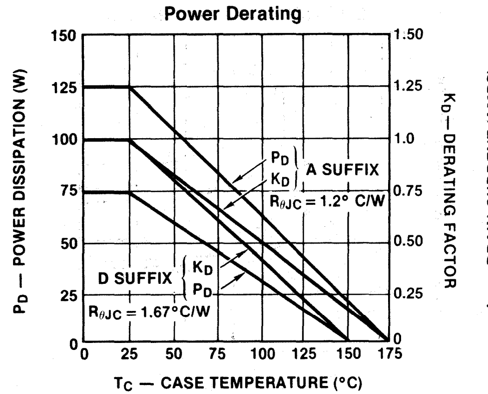
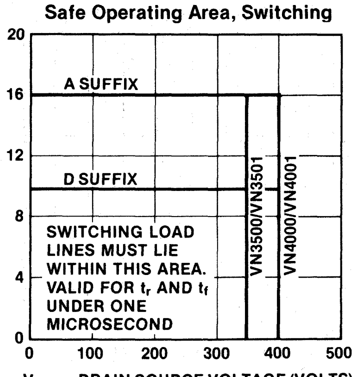
TYPICAL CHARACTERISTICS (Cont'd) VNDA40

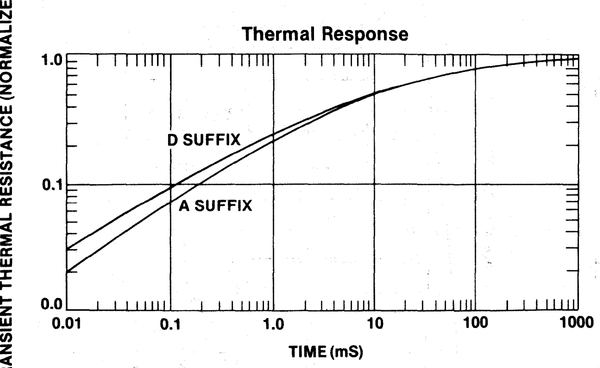
Part Numbers: VN3500A, VN3500D, VN3501A, VN3501D, VN4000A, VN4000D, VN4001A, VN4001D, IRF330, IRF331, IRF332, IRF333, IRF730, IRF731, IRF732, IRF733











The safe operating area data of "Active Region, TO-3 Package" and "Active Region, TO-220AB Package" indicates maximum operating current as a function of voltage and time at $T_C = 25°C$. At elevated temperatures, power must be derated using the derating factor, K_D from "Power Derating". Current limitations imposed by $r_{DS(on)}$ are not shown except at 25°C. When operating in the ohmic region, the maximum current is found from:

$$I_D = \left(\frac{P_D}{K_r \, r_{DS(on)} @ 25°C} \right)^{1/2}$$

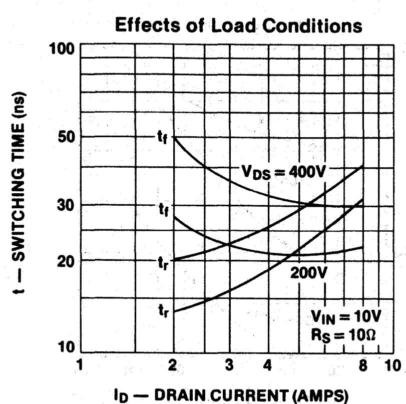
where P_D is the power dissipation at operating case temperature and $r_{DS(on)}$ is the on resistance for the part. K_r is the multiplying factor for on-resistance at the maximum rated junction temperature taken from "Temperature Effects on $r_{DS(on)}$".

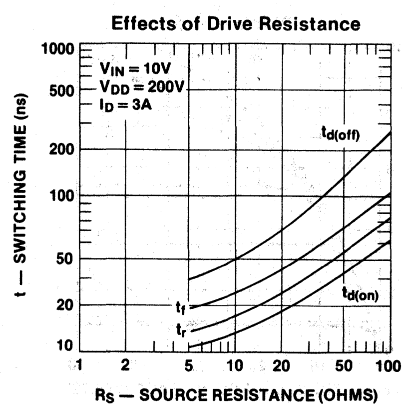
Since on-resistance varies somewhat with current, some iteration of I_D and $r_{DS(on)}$ must be done using "ON Resistance Characteristics" as a guide.

TYPICAL CHARACTERISTICS (Cont'd)

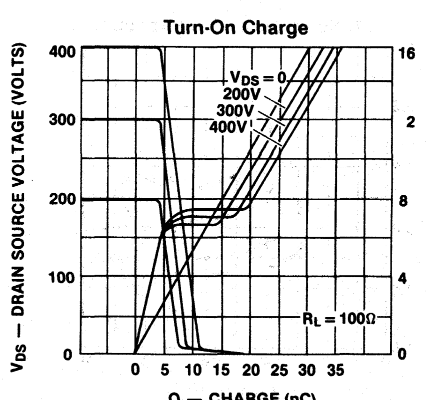
Part Numbers: VN3500A, VN3500D, VN3501A, VN3501D, VN4000A, VN4000D, VN4001A, VN4001D, IRF330, IRF331, IRF332, IRF333, IRF730, IRF731, IRF732, IRF733

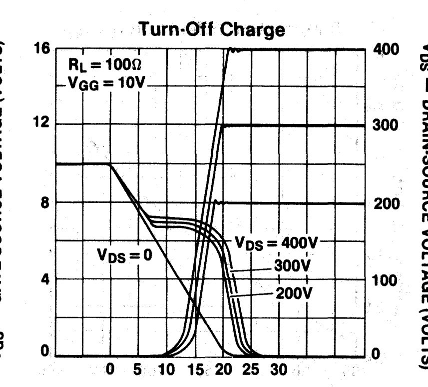
SWITCHING TIME





CHARGE





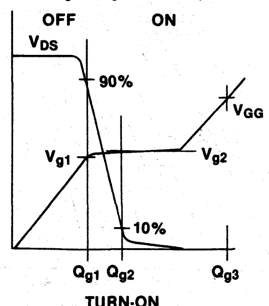
Switching Time Equations

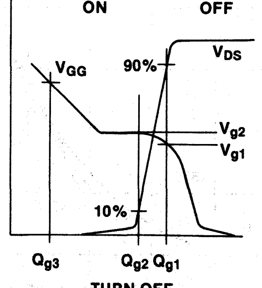
$$t_{d(on)} = \frac{Q_{g1}}{V_{g1}} R_{gen} \ln\left(\frac{V_{GG}}{V_{GG} - V_{g1}}\right)$$

$$t_{d(off)} = \frac{Q_{g3} - Q_{g2}}{V_{GG} - V_{g2}} R_{gen} \ln\left(\frac{V_{GG}}{V_{g2}}\right)$$

$$t_r = \frac{Q_{g2} - Q_{g1}}{V_{g2} - V_{g1}} R_{gen} \ln\left(\frac{V_{GG} - V_{g1}}{V_{GG} - V_{g2}}\right)$$

$$t_f = \frac{Q_{g2} - Q_{g1}}{V_{g2} - V_{g1}} R_{gen} \ln\left(\frac{V_{g2}}{V_{g1}}\right)$$





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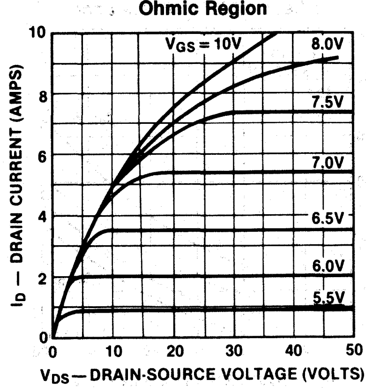
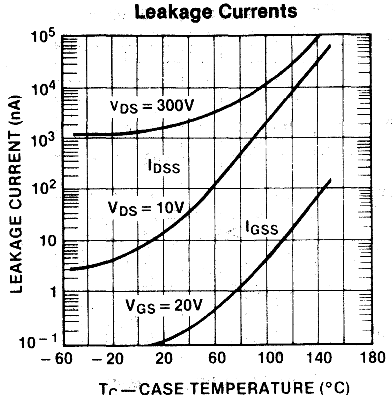
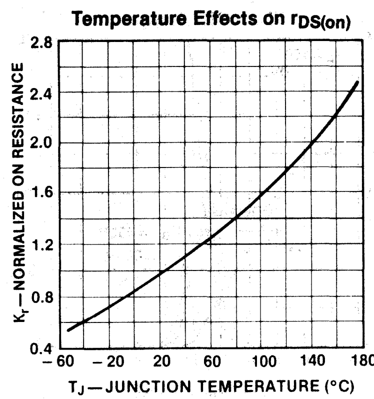
TYPICAL STATIC CHARACTERISTICS

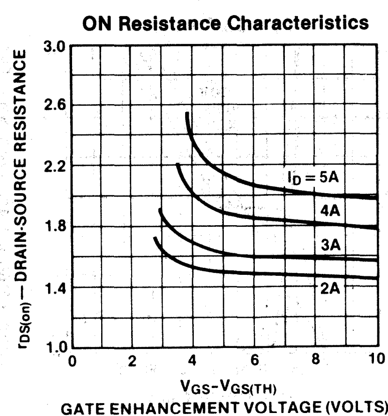
(Pulse width 80μs—300μs, Duty cycle 1%, T_C=25°C)

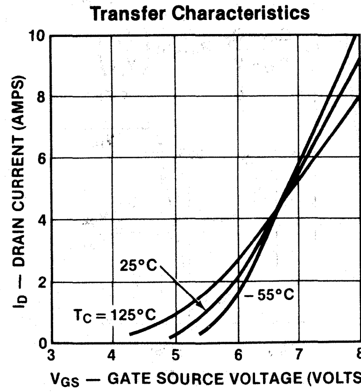
Part Numbers: VN4501A, VN4501D, VN4502A, VN4502D, VN5001A, VN5001D, VN5002A, VN5002D, IRF430, IRF431, IRF432, IRF433, IRF830, IRF831, IRF832, IRF833

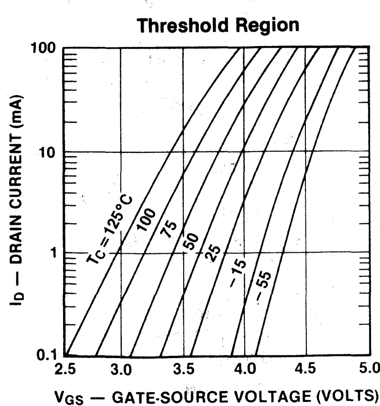












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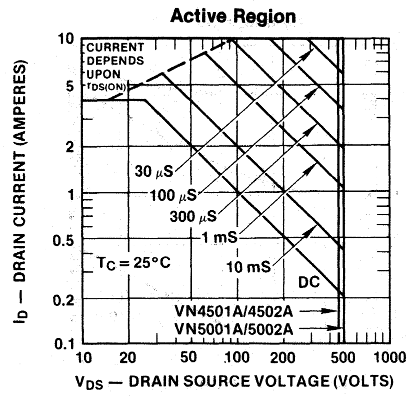
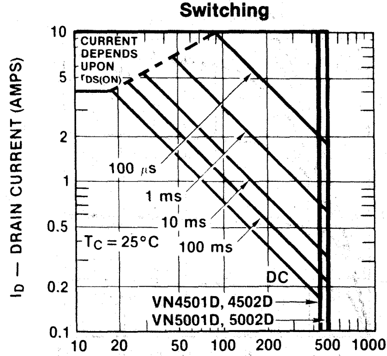
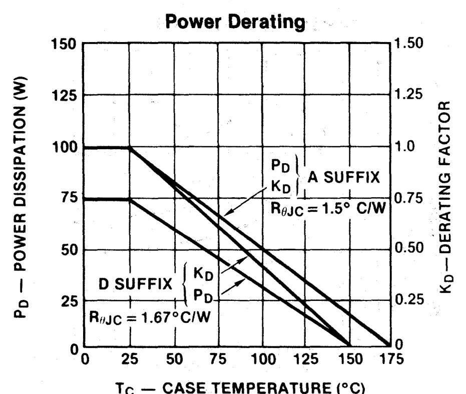
POWER RATINGS AND CHARACTERISTICS

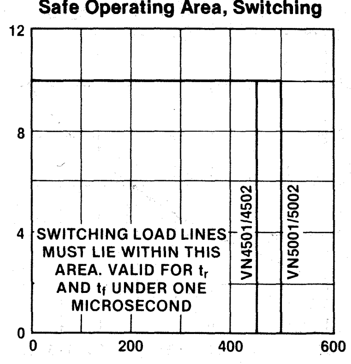
Part Numbers: VN4501A, VN4501D, VN4502A, VN4502D, VN5001A, VN5001D, VN5002A, VN5002D, IRF430, IRF431, IRF432, IRF433, IRF830, IRF831, IRF832, IRF833

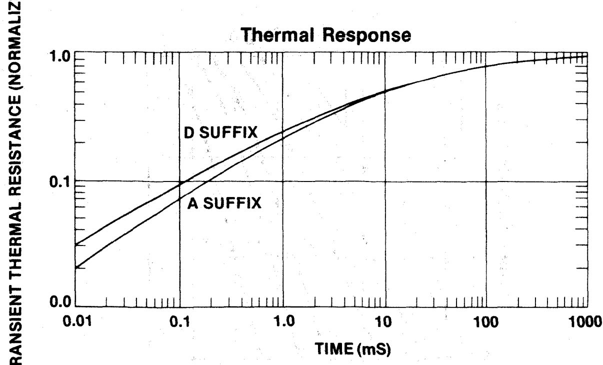
SAFE OPERATING AREA











The safe operating area data of "Power Derating" and "Safe Operating Area, Switching" indicates maximum operating current as a function of voltage and time at $T_C = 25°C$. At elevated temperatures, power must be derated using the derating factor, K_D from "Thermal Response". Current limitations imposed by $r_{DS(on)}$ are not shown except at 25°C. When operating in the ohmic region, the maximum current is found from:

$$I_D = \left(\frac{P_D}{K_r \, r_{DS(on)} \ @ \ 25°C} \right)^{1/2}$$

where P_D is the power dissipation at operating case temperature and $r_{DS(on)}$ is the on resistance for the part. K_r is the multiplying factor for on-resistance at the maximum rated junction temperature taken from "Transfer Characteristics".

Since on-resistance varies somewhat with current, some iteration of I_D and $r_{DS(on)}$ must be done using "Threshold Region" as a guide.

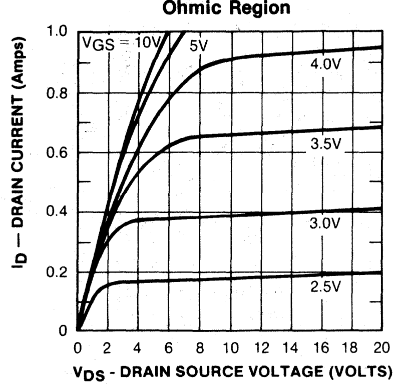
4

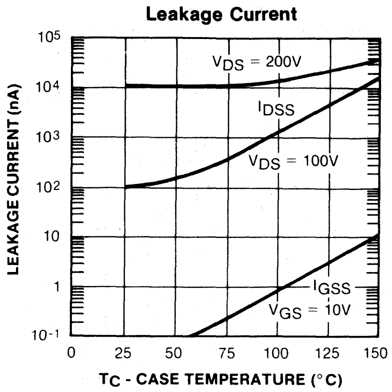
TYPICAL STATIC CHARACTERISTICS

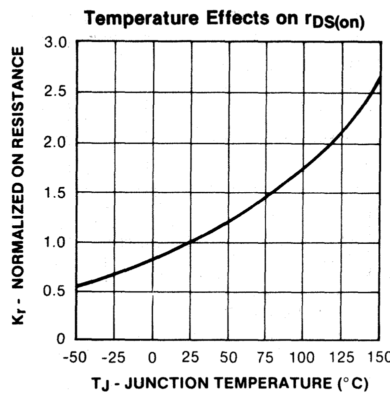
VNDB24

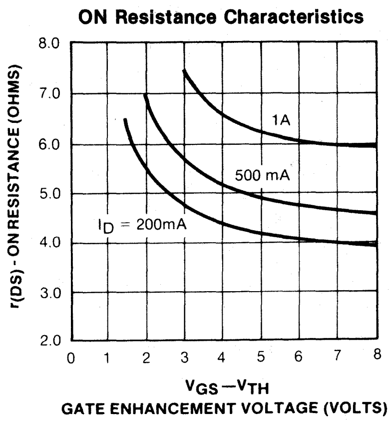
(Pulse width 80μs—300μs, Duty cycle 1%, T_C=25°C)

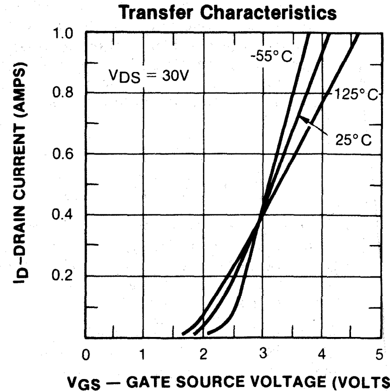
Part Numbers: VN2406L, VN1706L, VN1206L, VN2406M, VN1706M, VN1206M, VN2406B, VN1706B, VN1206B, VN2406D, VN1706D, VN1206D, VN2410L, VN1710L, VN1210L, VN2410M, VN1710M, VN1210M

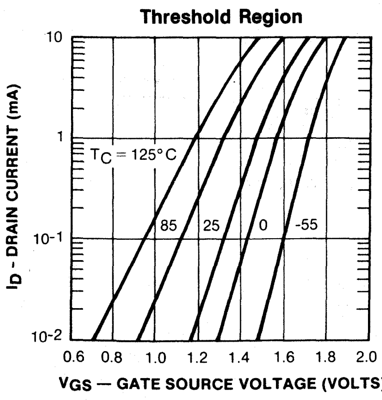












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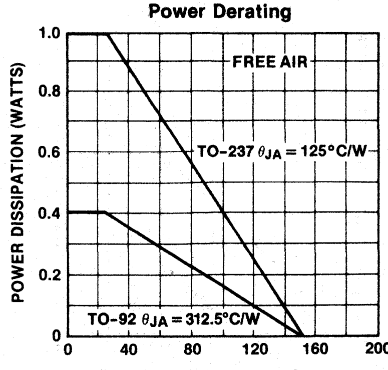
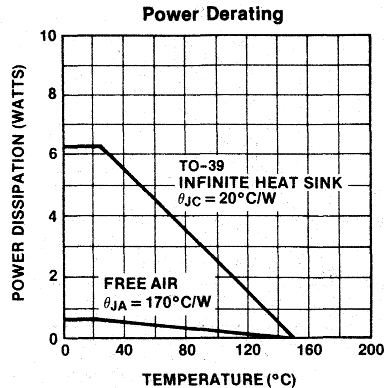
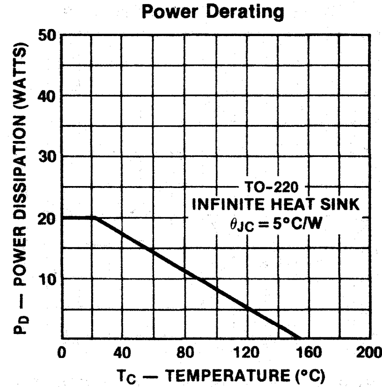
TYPICAL CHARACTERISTICS (Cont'd)

Part Numbers: VN2406L, VN1706L, VN1206L, VN2406M, VN1706M, VN1206M, VN2406B, VN1706B, VN1206B, VN2406D, VN1706D, VN1206D, VN2410L, VN1710L, VN1210L, VN2410M, VN1710M, VN1210M





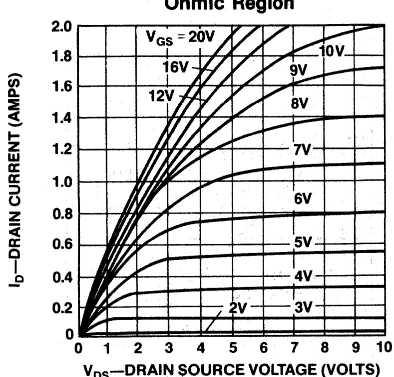


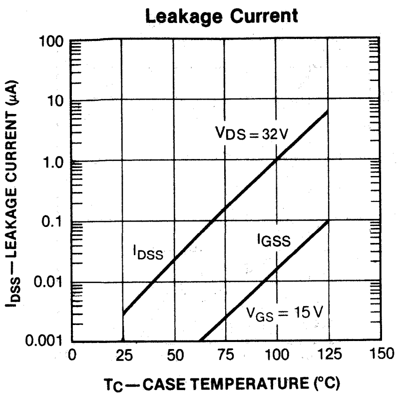
TYPICAL STATIC CHARACTERISTICS

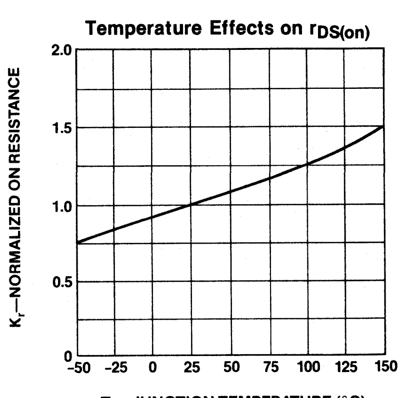
VNMA

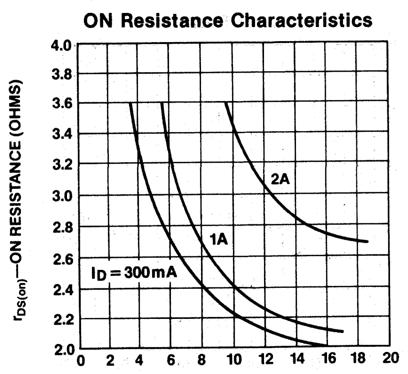
(Pulse width 80μs—300μs, Duty cycle 1%, T_C=25°C)

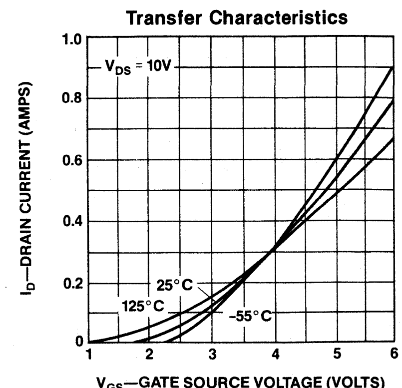
Part Numbers: VN99AA, VN99AB, VN90AA, VN90AB, VN89AD, VN89AF, VN88AD, VN88AF, VN80AF, VN0808M, VN67AA, VN67AD, VN67AB, VN67AF, VN66AD, VN66AF, VN0606M, VN46AD, VN46AF, VN40AD, VN40AF, VN35AA, VN35AB, 2N6656, 2N6657, 2N6658, 2N6659, 2N6660, 2N6661

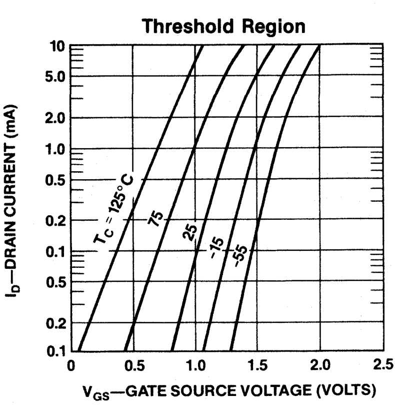












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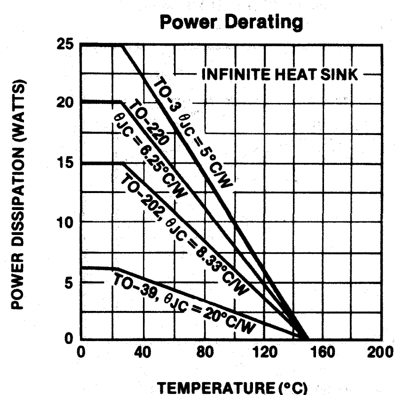
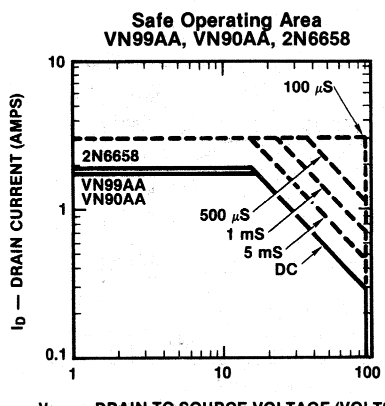
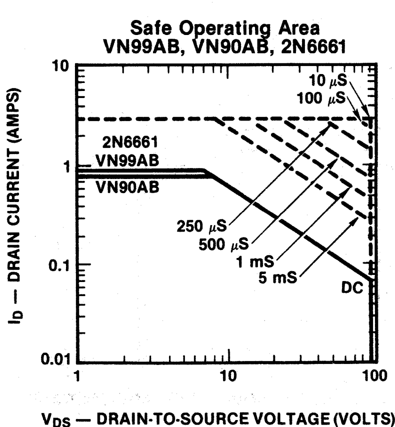
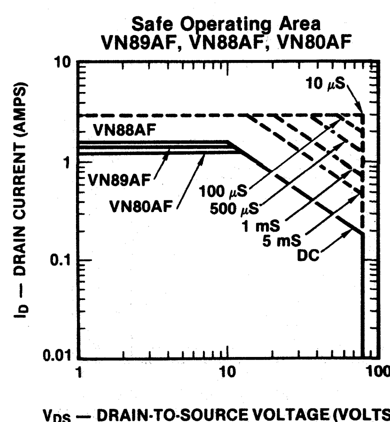
TYPICAL CHARACTERISTICS (Cont'd) VNMA

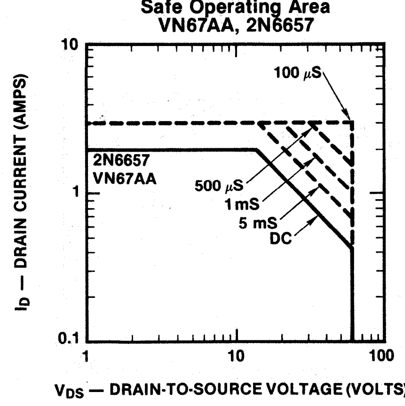
Part Numbers: VN99AA, VN99AB, VN90AA, VN90AB, VN89AD, VN89AF, VN88AD, VN88AF, VN80AF, VN0808M, VN67AA, VN67AD, VN67AB, VN67AF, VN66AD, VN66AF, VN0606M, VN46AD, VN46AF, VN40AD, VN40AF, VN35AA, VN35AB, 2N6656, 2N6657, 2N6658, 2N6659, 2N6660, 2N6661

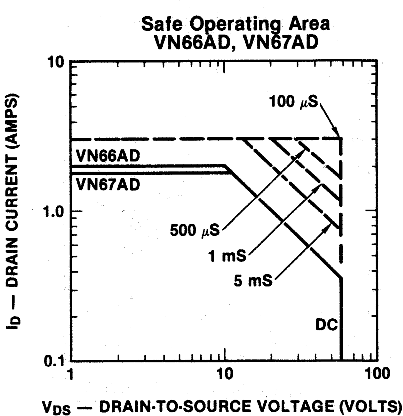






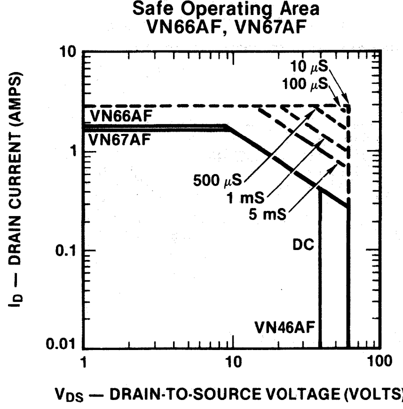


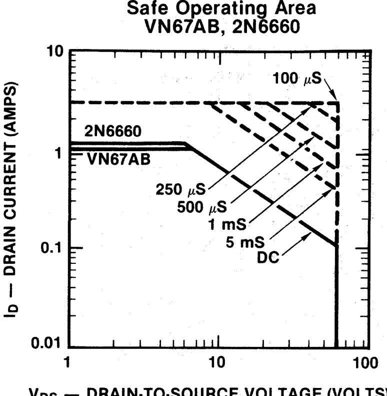


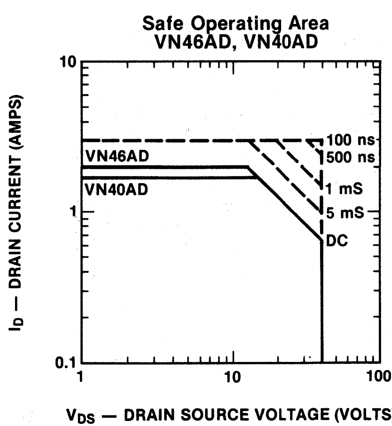


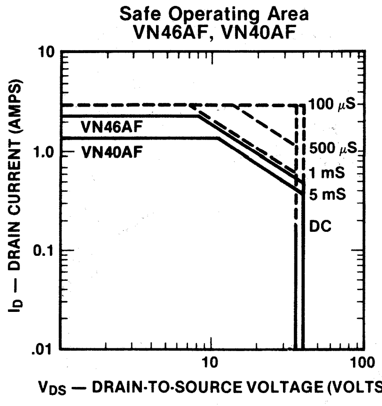
TYPICAL CHARACTERISTICS (Cont'd) VNMA

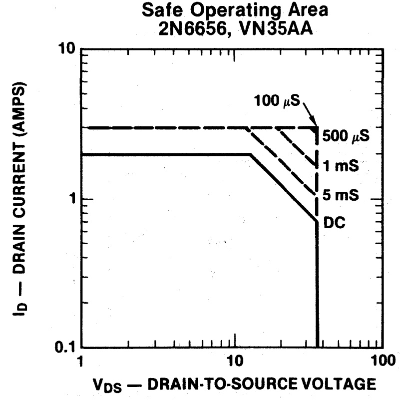
Part Numbers: VN99AA, VN99AB, VN90AA, VN90AB, VN89AD, VN89AF, VN88AD, VN88AF, VN80AF, VN0808M, VN67AA, VN67AD, VN67AB, VN67AF, VN66AD, VN66AF, VN0606M, VN46AD, VN46AF, VN40AD, VN40AF, VN35AA, VN35AB, 2N6656, 2N6657, 2N6658, 2N6659, 2N6660, 2N6661

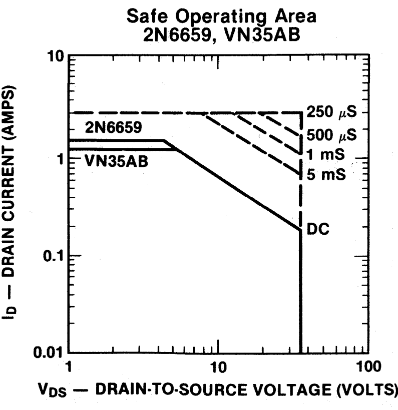








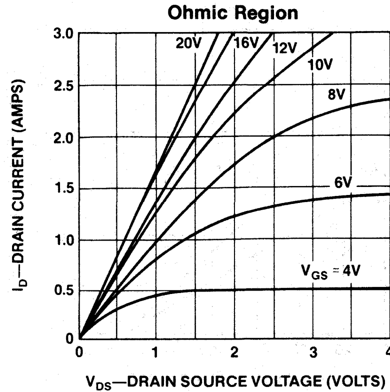


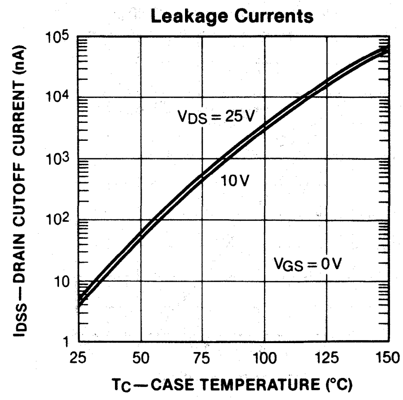


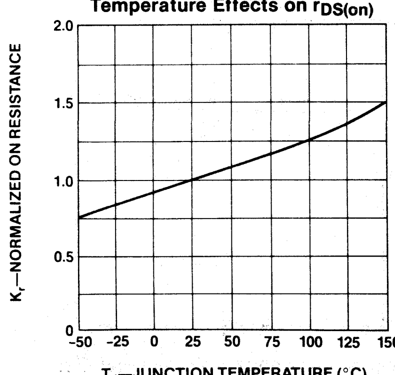
TYPICAL STATIC CHARACTERISTICS

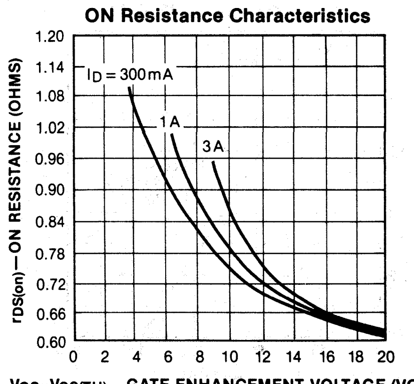
(Pulse width 80μs—300μs, Duty cycle 1%, $T_C = 25°C$)

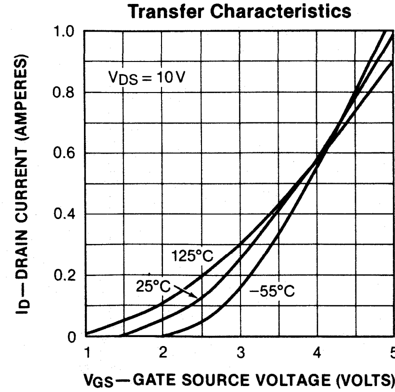
Part Numbers: VN0300D, VN0300M, VP1001P, VQ1001J,
Segments 1 and 3: VQ3001P, VQ3001J, VQ7254P, VQ7254J

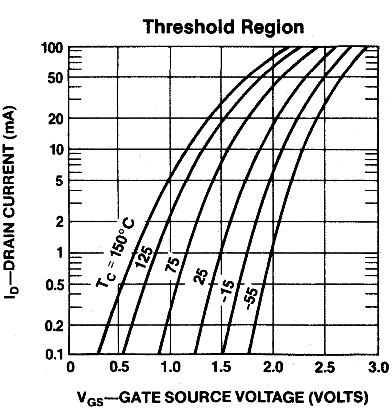












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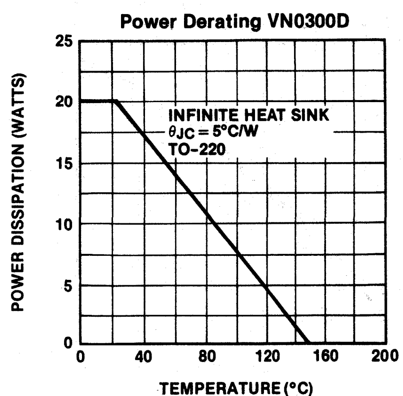
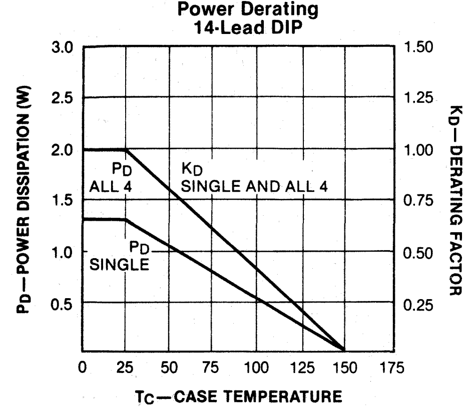
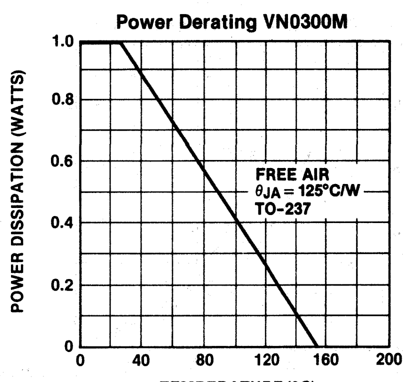
TYPICAL CHARACTERISTICS (Cont'd)

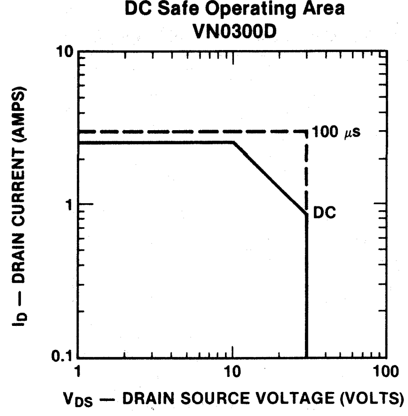
Part Numbers: VN0300D, VN0300M, VP1001P, VQ1001J,
Segments 1 and 3: VQ3001P, VQ3001J, VQ7254P, VQ7254J

SAFE OPERATING AREA





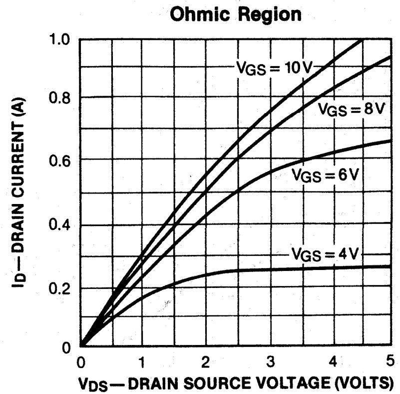


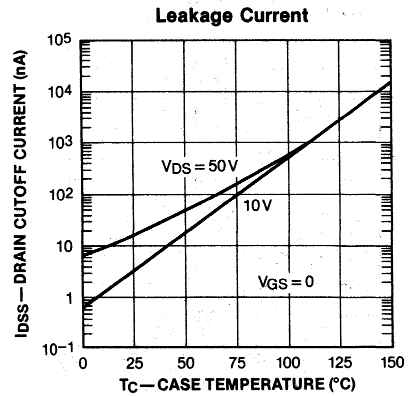


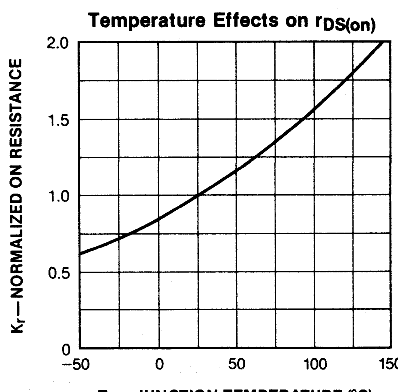
TYPICAL STATIC CHARACTERISTICS

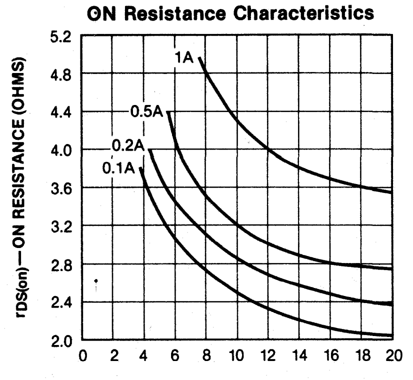
(Pulse width 80μs—300μs, Duty cycle 1%, $T_C = 25°C$)

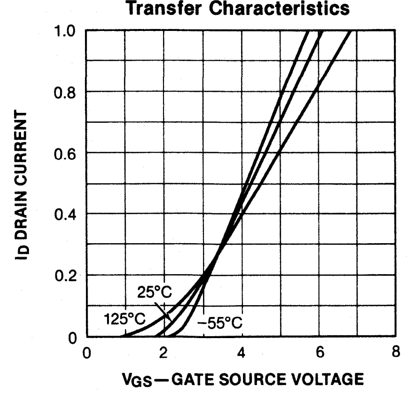
Part Numbers: VN10KM, VN10LM, VN10KE, VN10LE, VN0610L, VN2222L, VN2222LM, VN2222KM, VQ1000P, VQ1000J

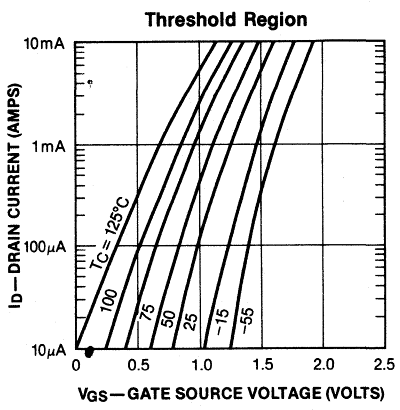












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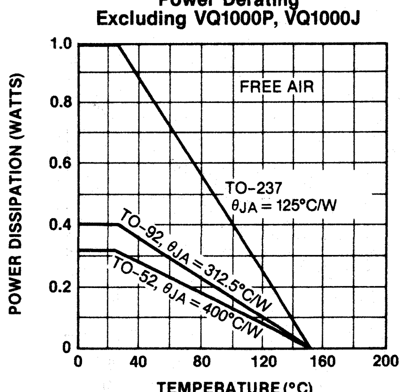
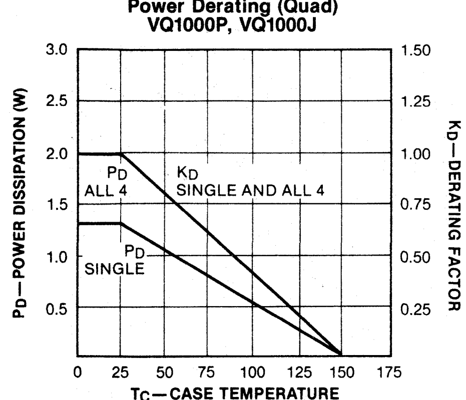
TYPICAL CHARACTERISTICS (Cont'd)

Part Numbers: VN10KM, VN10LM, VN10KE, VN10LE, VN0610L, VN2222L, VN2222LM, VN2222KM, VQ1000P, VQ1000J

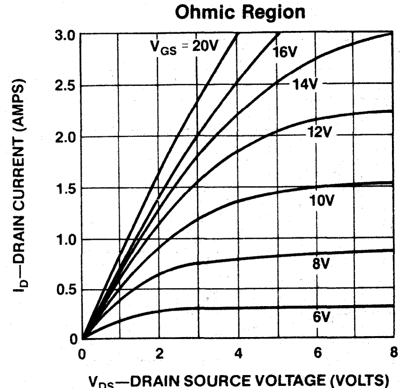


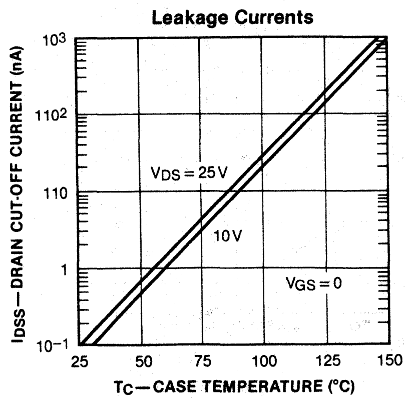


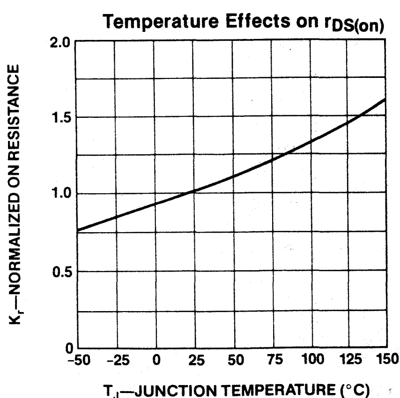
TYPICAL STATIC CHARACTERISTICS

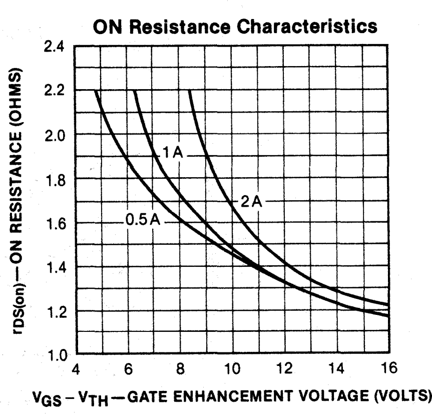
(Pulse width 80μs—300μs, Duty cycle 1%, T_C=25°C)

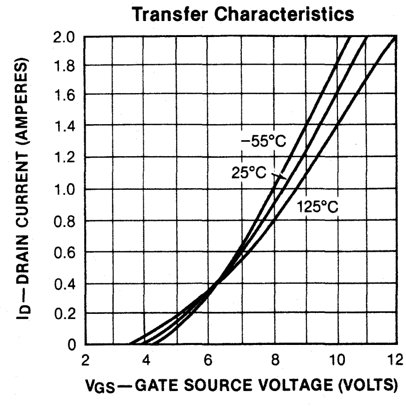
Part Numbers: VP0300M, VP0300L, VQ2001P, VQ2001J
Segments 2 and 4: VQ3001P, VQ3001J, VQ7254P, VQ7254J

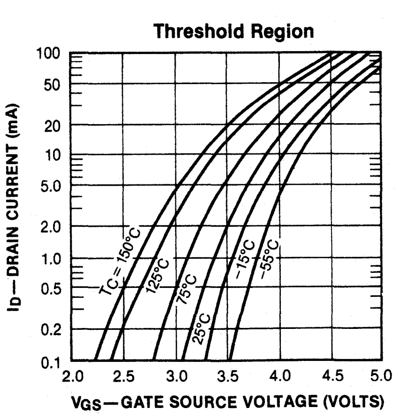












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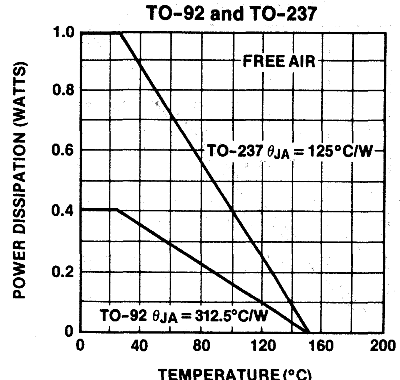
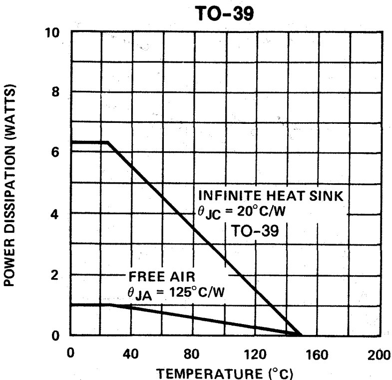
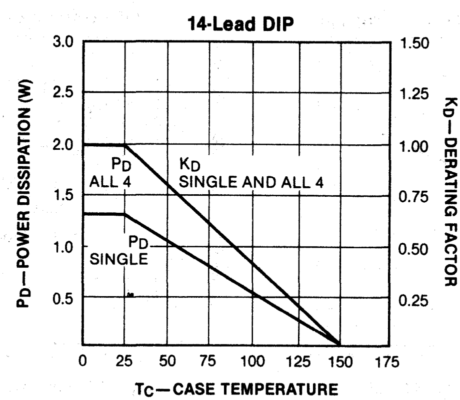
TYPICAL CHARACTERISTICS (Cont'd)

Part Numbers: VP0300M, VP0300L, VQ2001P, VQ2001J
Segments 2 and 4: VQ3001P, VQ3001J, VQ7254P, VQ7254J

POWER DERATING



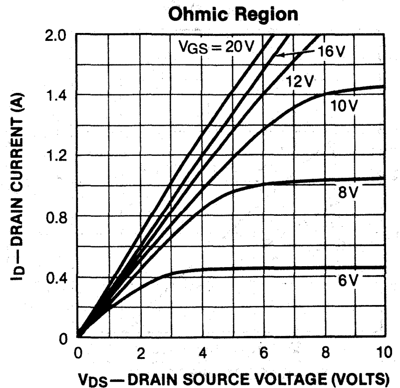


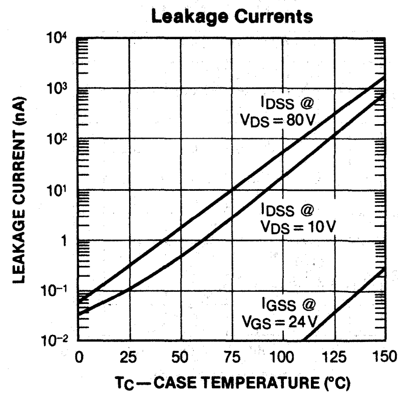


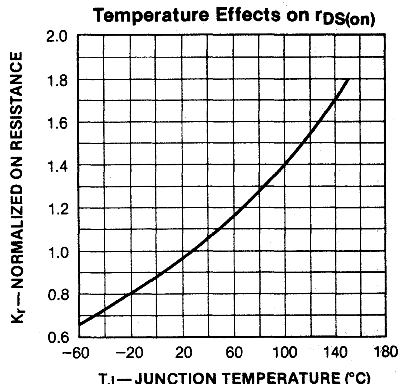
TYPICAL STATIC CHARACTERISTICS

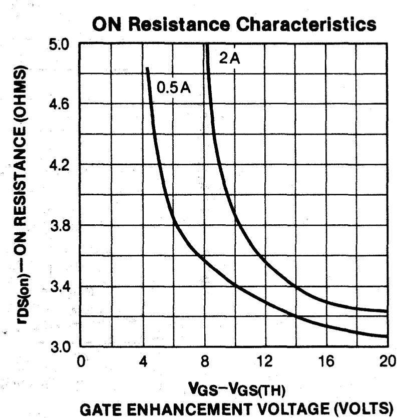
(Pulse width 80μs—300μs, Duty cycle 1%, T_C=25°C)

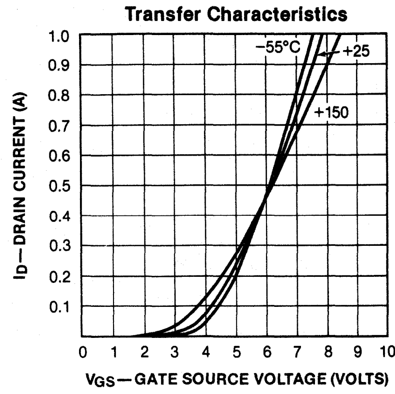
Part Numbers: VP1008L, VP0808L, VP1008M, VP0808M, VQ2006P, VQ2006J, VP1008B, VP0808B

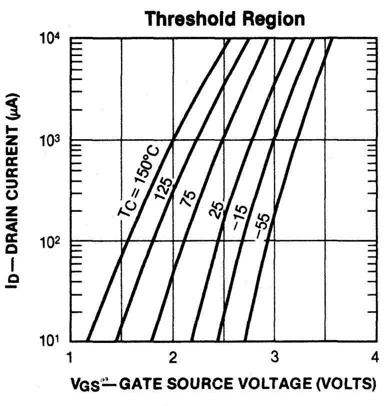












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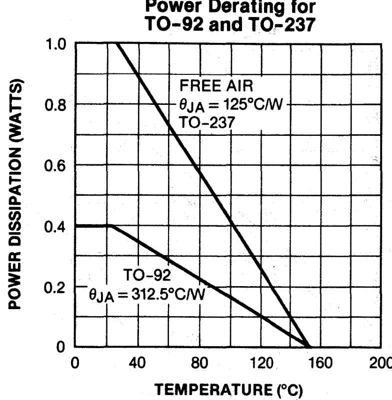
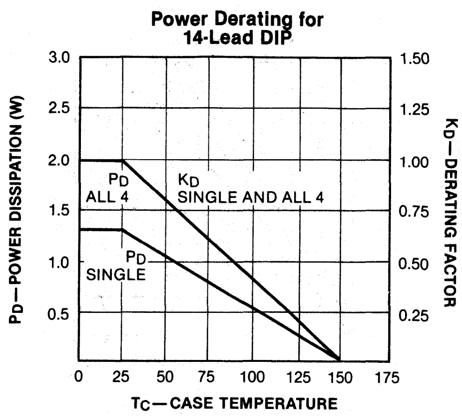
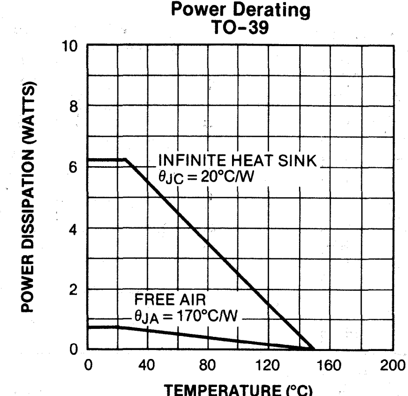
TYPICAL CHARACTERISTICS (Cont'd)

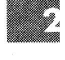
Part Numbers: VP1008L, VP0808L, VP1008M, VP0808M, VQ2006P, VQ2006J, VP1008B, VP0808B







MOSPOWER

Introduction

N-/P-Channel

Multi-Channel

Design Curves

RF 5
Application Notes

Other Siliconix Products

Worldwide Sales Offices 8

RF Power FETs Selector Guide

n-channel enhancement-mode RF Power FETs designed for. . .

HF/VHF/UHF Amplifiers Class A, B, C, D or E. High Dynamic Range Amp

BENEFITS

- Infinite VSWR
- No Thermal Runaway
- Broadband Capability
- Class A, B C, D, or E Operation
- Low Noise Figure
- High Dynamic Range
- Simple Bias Circuitry
- S-Parameter Design

ORDERING INFORMATION

DX XX XXX X

- X — Package Code
- XXX — Power Output (Watts)
- XX — Suggested Operating Voltage
- DX — Product Code

PACKAGE CODES

S = 380SOEF
T = 500JOF
U = 500SOEF
V = Push-Pull
W = C-220 Standard
Z = 280SOE

12.5 Volt DC — 300 MHz Series

Part Number	Test Frequency* (MHz)	Rated Power Out (Watts) @ 12.5 V_{DC}	Min. Gain (dB) 12.5 V, 175 MHz	Min. BV_{DSS}	θJc (°C/W)
DV1202S	175	2.0	10.0	45	17.6
DV1202W	175	2.0	10.0	45	14.1
DV1202Z	175	2.0	10.0	45	17.6
DV1205S	175	5.0	10.0	45	8.8
DV1205W	175	5.0	10.0	45	7.0
DV1205Z	175	5.0	10.0	45	8.8
DV1210S	175	10.0	10.0	45	4.4
DV1210W	175	10.0	10.0	45	3.5
DV1210Z	175	10.0	10.0	45	4.4
DV1220S	175	20.0	10.0	45	2.2
DV1220W	175	20.0	10.0	45	1.8
DV1230T	175	30.0	9.5	45	1.5
DV1230W	175	30.0	9.3	45	1.2
DV1240T	175	40.0	9.0	45	1.1
DV1240U	175	40.0	8.6	45	1.1
DV1240W	175	40.0	9.0	45	0.9
DV1260T	175	60.0	8.0	45	0.73

*All parts tested at 20:1 VSWR.
Note: See application notes AN80-4, AN80-6.

RF Power FETs Selector Guide (Cont'd)

28 Volt DC — 300 MHz Series

Part Number	Test Frequency* (MHz)	Rated Power Out (Watts) @ 28 V_{DC}	Min. Gain (dB) 28 V, 175 MHz	Min. BV_{DSS}	θJc (°C/W)
DV2805S	175	5	10	80	17.6
DV2805W	175	5	10	80	14.1
DV2805Z	175	5	10	80	17.6
DV2810S	175	10	10	80	8.8
DV2810W	175	10	10	80	7.0
DV2810Z	175	10	10	80	8.8
DV2820S	175	20	10	80	4.4
DV2820W	175	20	10	80	3.5
DV2820Z	175	20	10	80	4.4
DV2840S	175	40	10	80	2.2
DV2840W	175	40	10	80	1.8
DV2880T	175	80	10	80	1.1
DV2880U	175	80	10	80	1.1
DV2880W	175	80	10	80	0.9
DV28120T	175	120	10	80	0.73
DV28120U	175	120	9	80	0.73
VMP4	175	20	10	60	4.4

28 Volt Push-Pull — DC-300 MHz Series

Part Number	Test Frequency (MHz)	Test Voltage (V_{DS})	P_{in} (Max.) (Watts)	P_{out} @ 28 V (Watts)	G_{PS} (Min.) Power Gain (dB)	θJc Thermal Impedance (°C/W)
DV2880V	175	28	8	80	10	1.1
DV28120V	175	28	12	120	10	0.73

100 Volt DC — 300 MHz Series

Part Number	Test Frequency* (MHz)	Rated Power Out (Watts) @ 12.5 V_{DC}	Min. Gain (dB) 12.5 V, 175 MHz	Min. BV_{DSS}	θJc (°C/W)
DVD030S	175	25	13	220	4.40
DVD150T	175	120	10	220	0.73

*All parts tested at 20:1 VSWR.

Siliconix

175MHz
6-24V
2.0W
10db

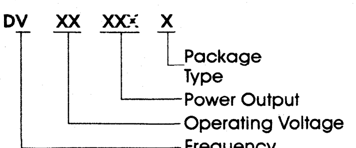
n-channel enhancement-mode RF Power FETs designed for...

HF/VHF/UHF Amplifiers Class A, B, or C
High Dynamic Range Amp

Benefits

Infinite VSWR
No Thermal Runaway
Broadband Capability
Class A, B, or C Operation
Low Noise Figure
High Dynamic Range
Simple Bias Circuitry
S-Parameter Design

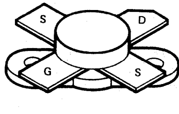
Other devices in series:
DV1205, DV1210, DV1220, DV1230, DV1240



Absolute Maximum Ratings (25°C)

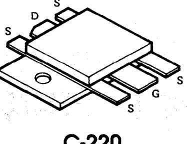
Gate-Source Voltage . . . . 30 V
Drain-Source Voltage . . . . 50 V
Drain-Gate Voltage . . . . 50 V
Drain Current (DC) . . . . 0.5 A
Total Device Dissipation . . . . 10 W
@ 25° Case
θjc . . . . 17.6°C/W
Storage Temperature . . . . −65°C to 150°C
Junction Temperature . . . . 200°C

Package Type S



.380 SOE FLANGE

Package Type W



C-220

See page 5-62 for Package Dimensions

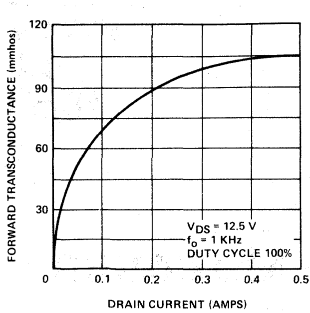
Electrical Characteristics (25°C)

Symbol	Characteristic	Min	Typ	Max	Unit	Test Conditions
P_{OUT}(1)	Power Output	2			W	V_{DS} = 12.5 V, I_{DQ} = 0.25 A P_{IN} = 0.20 W, f = 175 MHz
η(1)	Drain Efficiency		60		%	
g_m	Transconductance		100		mmho	V_{DS} = 12.5 V, I_D = 0.250 A
C_{oss}	Output Capacity		20		pF	V_{DS} = 12.5 V, V_{GS} = 0 V
C_{rss}	Reverse Transfer Capacity		2		pF	
C_{iss}	Input Capacity		14		pF	
NF(2)	Small Signal Noise Figure		7		dB	f = 175 MHz, V_{DS} = 12.5 V I_D = 0.25 A

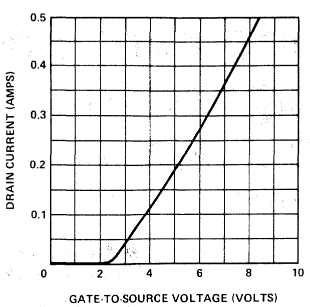
Notes: (1) All devices 100% power tested in Siliconix test fixture No. RF12175 [2]
(2) Noise figure measured with 2.5 watt power matched source and load

Typical Performance Curves (25°C)

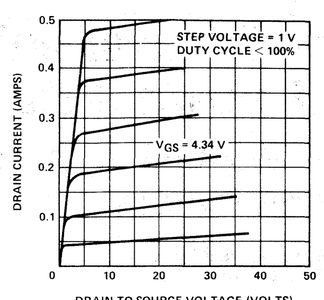
Transconductance vs Drain Current



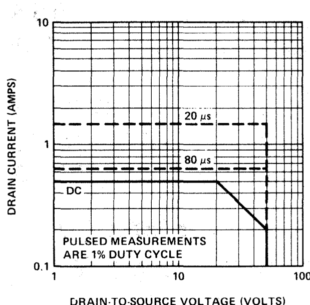
Drain Current vs Gate-to-Source Voltage



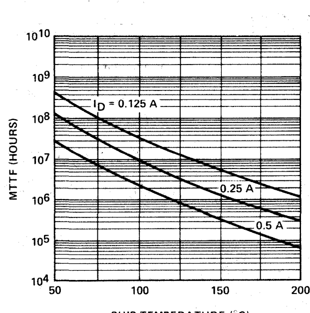
Output Characteristics vs Drain-to-Source Voltage



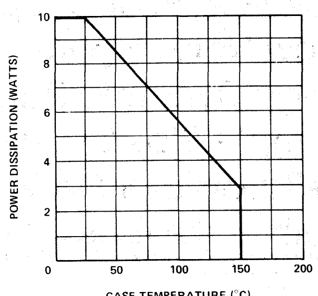
DC and Inductive Safe Operating Region $T_C = 25°C$



MTTF vs Chip Temperature

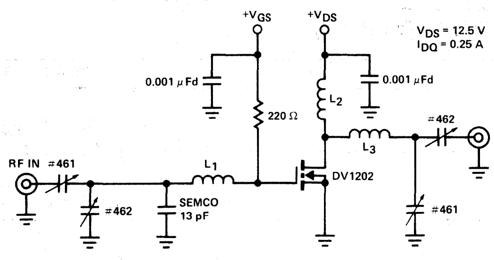


Power Dissipation vs Case Temperature



Test Fixture

DV1202S 175 MHz



Parts List

- L_1 4 turns #18 AWG on 1/8" diameter
- L_2 10 turns #22 AWG on 1/4" diameter
- L_3 4 turns #16 AWG on 1/4" diameter
- #461 3-30 pF
- #462 5-80 pF

All DV1202s are tested in this test fixture.

Small Signal 2-Port Parameters DV1202S

2-Port Y-Parameter Matrix in Millimhos

Freq (MHz)	Y_{11} (Real	Imag)	Y_{21} (Real	Imag)	Y_{12} (Real	Imag)	Y_{22} (Real	Imag)
10	−.058	.962	91.2	−3.76	−.002	−.108	1.59	1.54
20	.021	1.48	89.8	−4.31	.007	−.335	1.78	2.38
30	−.218	2.27	91.1	−6.85	.027	−.567	1.66	3.38
40	−.369	3.07	91.9	−8.32	.048	−.822	1.47	4.51
50	−.259	4.24	93.6	−10.7	.089	−1.01	1.74	5.98
60	−.200	5.30	92.9	−12.7	.119	−1.23	1.83	7.39
70	−.232	6.38	92.0	−17.0	.169	−1.47	1.82	8.78
80	.140	7.74	96.1	−17.8	.217	−1.64	2.29	10.6
90	.446	8.49	96.6	−19.1	.306	−1.97	2.34	11.8
100	.519	9.87	98.1	−23.7	.363	−2.19	3.09	13.1
120	1.34	12.1	105	−27	.460	−2.7	4.23	16.1
140	1.61	14.0	106	−33.9	.695	−3.49	4.8	18.5
160	2.37	16.1	111	−38.8	.949	−4.17	6.13	21.0
180	2.85	18.7	114	−47.9	1.25	−4.93	6.92	24.1
200	4.72	21.3	120	−58.5	1.47	−5.46	9.18	27.2
225	5.12	24.2	126	−70.1	1.83	−6.43	9.44	30.7
250	6.29	27.2	130	−84.7	2.36	−7.74	10.3	34.4
275	8.05	30.4	130	−101	3.03	−9.24	11.0	38.5
300	10.5	33.6	125	−118	3.64	−10.8	11.9	41.8
325	13.7	36.4	119	−128	4.46	−12.2	12.2	44.6
350	19.2	39.5	115	−148	4.98	−13.0	14.5	48.5
375	20.5	41.3	103	−152	6.43	−15.1	13.0	49.3
400	24.1	41.9	93.8	−159	7.68	−16.1	13.4	50.8
425	27.9	43.1	83.8	−162	8.49	−17.1	14.9	51.3
450	30.6	43.5	71.5	−167	9.22	−18.0	16.5	53.1
475	30.7	43.5	63.4	−162	11.0	−19.5	15.6	51.8
500	30.3	41.4	51.0	−156	12.1	−20.9	16.1	52.3

Conditions: 12.5 V @ 250 mA

Polar S-Parameters in 50.0 Ohm System

Freq (MHz)	S_{11} (Magn	Angl)	S_{21} (Magn	Angl)	S_{12} (Magn	Angl)	S_{22} (Magn	Angl)
10	1.00	−8	8.41	170	.01	81	.85	−12
20	.98	−16	8.04	163	.03	77	.83	−22
30	.98	−26	8.04	154	.05	71	.83	−34
40	.96	−36	7.85	146	.07	64	.83	−45
50	.92	−45	7.41	137	.08	58	.80	−57
60	.88	−53	6.84	129	.09	52	.78	−66
70	.84	−61	6.31	120	.10	47	.76	−75
80	.80	−69	5.89	114	.10	42	.74	−84
90	.76	−76	5.43	109	.11	39	.74	−92
100	.74	−83	5.01	103	.11	36	.70	−99
120	.69	−95	4.37	96	.11	30	.68	−111
140	.66	−105	3.76	88	.12	27	.67	−121
160	.65	−114	3.31	83	.12	25	.67	−129
180	.64	−122	2.92	76	.12	23	.67	−136
200	.63	−129	2.60	72	.11	23	.67	−141
225	.63	−136	2.37	66	.11	21	.68	−146
250	.63	−143	2.11	61	.11	21	.69	−151
275	.63	−149	1.86	56	.11	22	.70	−155
300	.63	−155	1.66	52	.11	24	.70	−158
325	.64	−159	1.48	49	.11	26	.71	−159
350	.65	−162	1.35	46	.10	29	.72	−161
375	.66	−165	1.23	43	.11	32	.72	−162
400	.67	−167	1.14	41	.11	36	.73	−162
425	.68	−169	1.05	40	.11	39	.73	−163
450	.68	−170	.99	38	.11	42	.73	−164
475	.69	−171	.93	37	.12	45	.73	−164
500	.68	−172	.88	36	.13	48	.73	−165

Conditions: 12.5 V @ 250 mA

Small Signal 2-Port Parameters DV1202W

2-Port Y-Parameter Matrix in Millimhos

Freq (MHz)	Y_{11} (Real	Imag)	Y_{21} (Real	Imag)	Y_{12} (Real	Imag)	Y_{22} (Real	Imag)
10	.241	.745	98.7	−2.88	.005	−.227	2.21	1.32
20	.063	1.70	96.1	−2.54	.015	−.343	2.21	2.56
30	−.132	2.30	97.1	−3.78	.038	−.576	1.94	3.63
40	−.370	3.11	97.2	−6.92	.058	−.837	1.73	4.94
50	−.149	4.32	98.9	−7.94	.080	−1.04	2.01	6.35
60	.012	5.23	99.3	−7.01	.131	−1.26	2.13	7.78
70	−.005	6.33	101	−10.1	.170	−1.53	2.21	9.17
80	.045	7.03	102	−11.2	.221	−1.84	2.64	10.4
90	.319	8.46	103	−11.1	.277	−2.01	2.95	11.8
100	.674	9.56	106	−11.4	.311	−2.24	3.47	13.5
120	1.01	11.3	107	−15.0	.461	−2.89	4.0	16.0
140	1.62	13.3	108	−18.5	.554	−3.38	4.65	18.4
160	1.93	15.5	113	−21.3	.657	−4.01	5.88	21.2
180	2.81	17.5	115	−24.6	.731	−4.66	6.49	23.6
200	2.66	18.8	113	−26.3	.964	−5.53	6.25	25.4
225	3.18	20.9	117	−29.8	1.22	−6.44	6.98	28.4
250	4.17	24.3	128	−34.4	1.27	−7.30	8.30	33.4
275	5.00	27.9	131	−42.9	1.49	−8.54	8.20	36.7
300	7.48	31.6	136	−49.5	1.48	−9.27	9.45	41.4
325	9.41	34.3	137	−56.8	1.58	−10.5	10.3	44.0
350	13.7	38.9	140	−69.4	1.31	−11.3	11.8	48.2
375	16.1	41.8	142	−71.3	1.82	−12.5	12.0	49.7
400	18.9	44.7	136	−78.3	1.90	−13.4	11.7	51.7
425	25.0	52.1	154	−98.8	2.26	−15.4	13.6	56.9
450	26.4	54.7	160	−112	2.46	−17.6	16.9	60.1
475	31.8	56.6	160	−130	2.78	−19.7	15.4	64.3
500	38.6	59.1	162	−164	1.71	−21.1	24.0	71.4

Conditions: 12.5 V @ 0.25 A

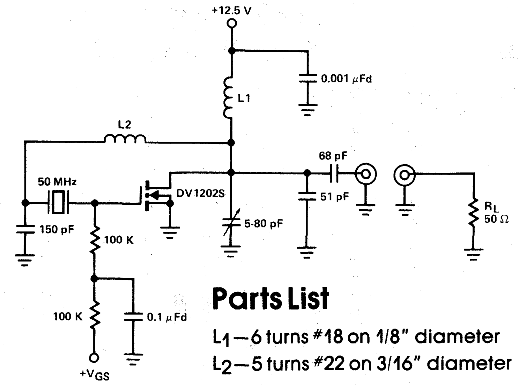
Polar S-Parameters in 50.0 Ohm System

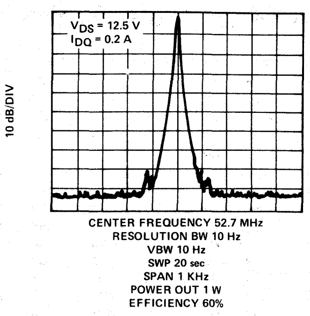
Freq (MHz)	S_{11} (Magn	Angl)	S_{21} (Magn	Angl)	S_{12} (Magn	Angl)	S_{22} (Magn	Angl)
10	.97	−10	8.71	170	.02	83	.80	−14
20	.98	−18	8.41	163	.03	77	.80	−24
30	.98	−27	8.41	155	.05	71	.82	−36
40	.96	−37	8.13	145	.07	63	.82	−49
50	.91	−47	7.59	137	.08	56	.79	−60
60	.88	−55	7.08	131	.09	51	.79	−70
70	.84	−64	6.61	123	.10	45	.77	−80
80	.81	−71	6.10	118	.11	41	.75	−89
90	.79	−78	5.62	113	.11	37	.74	−95
100	.76	−84	5.19	109	.11	33	.73	−102
120	.72	−95	4.42	101	.12	28	.72	−113
140	.69	−103	3.85	95	.12	24	.71	−120
160	.68	−111	3.39	90	.12	20	.70	−128
180	.66	−118	2.99	86	.12	17	.70	−133
200	.66	−123	2.69	82	.13	15	.71	−137
225	.66	−129	2.40	78	.13	13	.72	−142
250	.66	−135	2.14	74	.12	9	.73	−147
275	.66	−141	1.91	69	.12	7	.73	−150
300	.66	−145	1.70	66	.11	5	.74	−152
325	.66	−149	1.53	64	.11	5	.74	−154
350	.66	−153	1.38	61	.10	4	.74	−155
375	.68	−156	1.26	60	.10	5	.75	−156
400	.68	−158	1.16	57	.10	5	.75	−156
425	.71	−163	1.06	55	.09	6	.76	−159
450	.72	−165	.99	55	.09	8	.76	−162
475	.72	−168	.93	53	.09	10	.77	−163
500	.72	−170	.87	53	.08	13	.77	−166

Conditions: 12.5 V @ 0.25 A

Applications

DV1202S 50 MHz Crystal Oscillator

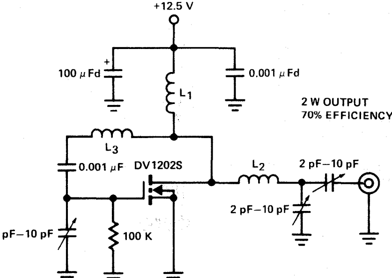




Parts List

L_1—6 turns #18 on 1/8" diameter
L_2—5 turns #22 on 3/16" diameter

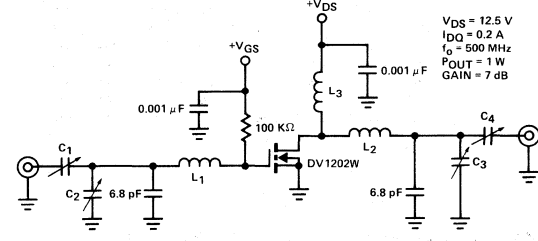
DV1202S 400 MHz Oscillator



Parts List

L_1—8 turns #22 closewound on 1/4" diameter
L_2—1/2 inch #16 wire
L_3—1 inch #16 wire

DV1202W 500 MHz Amplifier



Parts List

C_1, C_2, C_3, C_4, ARCO #400, 1→7 pF
L_1, L_2, 1/2" length #12 wire
L_3, 4 turns #22 enameled wire close wound on 1/4" diameter

CAUTION: Beryllium Oxide – The top cap of this device is alumina which is harmless. However the ceramic portion between the leads and the metal flange is Beryllium Oxide, the dust of which is toxic. Care must therefore be taken during handling and mounting the device to prevent any damage to this area.

Steps must be taken to ensure that all those who may handle, use, or dispose of this device are aware of its nature and of these necessary safety precautions. In particular the transistor should never be thrown out with general industrial or domestic waste.

Siliconix

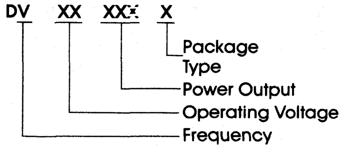
175 MHz
6-24 V
5 W
10 dB

n-channel enhancement-mode RF Power FETs designed for...

HF/VHF/UHF Amplifiers Class A, B, or C
High Dynamic Range Amp

Benefits

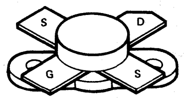
Infinite VSWR
No Thermal Runaway
Broadband Capability
Class A, B, or C Operation
Low Noise Figure
High Dynamic Range
Simple Bias Circuitry
S-Parameter Design
Other devices in series:
DV1202, DV1210, DV1220, DV1230, DV1240



Absolute Maximum Ratings (25°C)

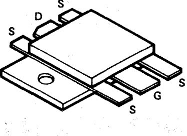
Gate-Source Voltage . . . . 30 V
Drain-Source Voltage . . . . 50 V
Drain-Gate Voltage . . . . 50 V
Drain Current (DC) . . . . 1 A
Total Device Dissipation . . . . 20 W
@ 25° Case
θjc . . . . 8.8°C/W
Storage Temperature . . . . −65°C to 150°C
Junction Temperature . . . . 200°C

Package Type S



.380 SOE FLANGE

Package Type W



C-220

See page 5-62 for Package Dimensions

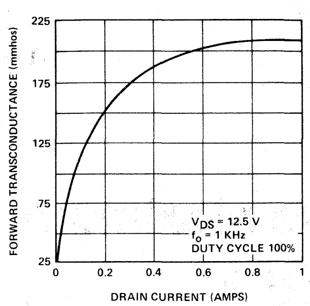
Electrical Characteristics (25°C)

Symbol	Characteristic	Min	Typ	Max	Unit	Test Conditions
P_{OUT}(1)	Power Output	5			W	V_{DS} = 12.5 V, I_{DQ} = 0.5 A, P_{IN} = 0.5 W, f = 175 MHz
η(1)	Drain Efficiency		60		%	
g_m	Transconductance		200		mmho	V_{DS} = 12.5 V, I_D = 0.5 A
C_{oss}	Output Capacity		38		pF	V_{DS} = 12.5 V, V_{GS} = 0 V
C_{rss}	Reverse Transfer Capacity		4		pF	V_{DS} = 12.5 V, V_{GS} = 0 V
C_{iss}	Input Capacity		26		pF	V_{DS} = 12.5 V, V_{GS} = 0 V
NF(2)	Small Signal Noise Figure		7		dB	f = 175 MHz, V_{DS} = 12.5 V, I_D = 0.5 A

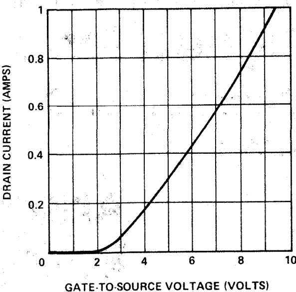
Notes: (1) All devices 100% power tested in Siliconix test fixture No. RF12175 [5]
(2) Noise figure measured with 5 watt power matched source and load

Typical Performance Curves (25°C)

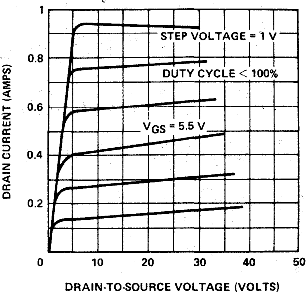
Transconductance vs Drain Current



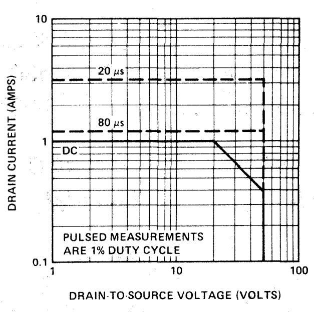
Drain Current vs Gate-to-Source Voltage



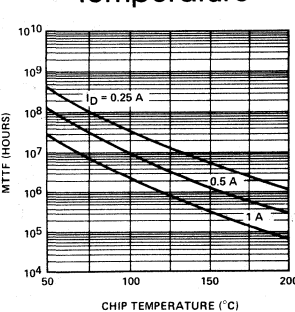
Output Characteristics vs Drain-to-Source Voltage



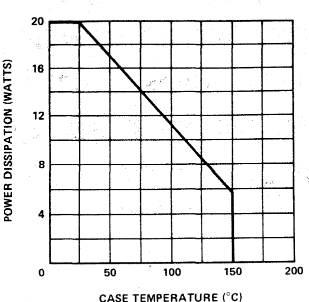
DC and Inductive Safe Operating Region $T_C = 25°C$



MTTF vs Chip Temperature

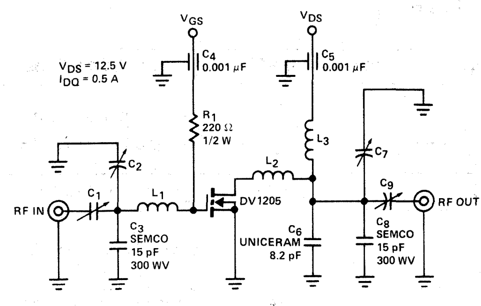


Power Dissipation vs Case Temperature



Test Fixture

DV1205 175 MHz



Parts List

C_1, C_7, 2.7 to 30 pF, ARCO #461 trimmer capacitors
C_2, C_9, 5 to 80 pF, ARCO #462 trimmer capacitors
L_1, 3 turns #18 AWG on 1/8" diameter, close wound
L_2, 2 turns #16 AWG on 1/8" diameter, close wound
L_3, 10 turns #22 AWG on 1/4" diameter, close wound

All DV1205s are tested in this test fixture.

Small Signal 2-Port Parameters DV1205S

2-Port Y-Parameter Matrix in Millimhos

Freq	Y_{11}		Y_{21}		Y_{12}		Y_{22}	
(MHz)	(Real	Imag)	(Real	Imag)	(Real	Imag)	(Real	Imag)
10	−.116	1.92	182	−7.52	−.004	−.216	3.18	3.08
20	.042	2.96	180	−8.62	.014	−.670	3.56	4.76
30	−.436	4.54	182	−13.7	.054	−1.13	3.32	6.76
40	−.738	6.14	184	−16.6	.096	−1.64	2.94	9.02
50	−.518	8.48	187	−21.4	.178	−2.02	3.48	12.0
60	−.400	10.6	186	−25.4	.238	−2.46	3.66	14.8
70	−.464	12.8	184	−34.0	.338	−2.94	3.64	17.6
80	.280	15.5	192	−35.6	.434	−3.28	4.58	21.2
90	.892	17.0	193	−38.2	.612	−3.94	4.68	23.6
100	1.04	19.7	196	−47.4	.726	−4.38	6.18	26.2
120	2.68	24.2	210	−54.0	.920	−5.40	8.46	32.2
140	3.22	28.0	212	−67.8	1.39	−6.98	9.60	37.0
160	4.74	32.2	222	−77.6	1.90	−8.34	12.3	42.0
180	5.70	37.4	228	−95.8	2.50	−9.86	13.8	48.2
200	9.44	42.6	240	−117	2.94	−10.9	18.4	54.4
225	10.2	48.4	252	−140	3.66	−12.9	18.9	61.4
250	12.6	54.4	260	−169	4.72	−15.5	20.6	68.8
275	16.1	60.8	260	−202	6.06	−18.5	22.0	77.0
300	21.0	67.2	250	−236	7.28	−21.6	23.8	83.6
325	27.4	72.8	238	−256	8.92	−24.4	24.4	89.2
350	38.4	79.0	230	−296	9.96	−26.0	29.0	97.0
375	41.0	82.6	206	−304	12.9	−30.2	26.0	98.6
400	48.2	83.8	188	−318	15.4	−32.2	26.8	102
425	55.8	86.2	168	−324	17.0	−34.2	29.8	103
450	61.2	87.0	143	−334	18.4	−36.0	33.0	106
475	61.4	87.0	127	−324	22.0	−39.0	31.2	104
500	60.6	82.8	102	−312	24.2	−41.8	32.2	105

Conditions: 12.5 V @ 500 mA

Polar S-Parameters in 50.0 Ohm System

Freq	S_{11}		S_{21}		S_{12}		S_{22}	
(MHz)	(Magn	Angl)	(Magn	Angl)	(Magn	Angl)	(Magn	Angl)
10	.98	−20	15.2	160	.02	71	.72	−29
20	.90	−43	13.3	145	.05	59	.70	−58
30	.86	−65	11.8	130	.07	47	.71	−83
40	.79	−84	10.1	117	.09	36	.72	−102
50	.74	−96	8.44	108	.09	29	.71	−115
60	.71	−106	7.11	100	.09	23	.70	−124
70	.68	−113	6.09	92	.10	20	.69	−131
80	.67	−120	5.32	87	.09	16	.70	−136
90	.66	−127	4.63	84	.09	14	.72	−141
100	.67	−131	4.11	79	.09	12	.71	−145
120	.68	−139	3.33	75	.08	9	.72	−151
140	.69	−146	2.73	69	.09	8	.74	−156
160	.71	−151	2.30	66	.08	8	.75	−159
180	.72	−154	1.97	61	.08	8	.76	−162
200	.73	−158	1.71	58	.07	9	.78	−164
225	.74	−161	1.53	54	.07	9	.79	−166
250	.75	−164	1.33	51	.07	11	.80	−168
275	.76	−167	1.15	47	.07	13	.81	−170
300	.77	−170	1.02	44	.07	16	.82	−171
325	.78	−171	.90	42	.07	19	.82	−171
350	.79	−173	.81	40	.06	23	.83	−172
375	.80	−174	.74	38	.07	26	.84	−172
400	.81	−175	.68	36	.07	31	.84	−173
425	.82	−176	.62	36	.06	34	.84	−173
450	.82	−176	.58	33	.06	37	.85	−173
475	.83	−177	.55	33	.07	41	.85	−173
500	.82	−177	.52	32	.08	44	.85	−174

Conditions: 12.5 V @ 500 mA

Small Signal 2-Port Parameters DV1205W

2-Port Y-Parameter Matrix in Millimhos

Freq	Y_{11}		Y_{21}		Y_{12}		Y_{22}	
(MHz)	(Real	Imag)	(Real	Imag)	(Real	Imag)	(Real	Imag)
10	.482	1.49	197	−5.77	.01	−.453	4.42	2.64
20	.126	3.4	192	−5.07	.03	−.685	4.42	5.12
30	−.263	4.6	194	−7.56	.08	1.15	3.87	7.27
40	−.739	6.22	194	−13.8	.115	−1.67	3.46	9.89
50	−.298	8.65	198	−15.9	.161	−2.09	4.02	12.7
60	−.023	10.5	199	−14	.263	−2.52	4.26	15.6
70	−.005	12.7	202	−20	.339	−3.06	4.42	18.3
80	.090	14.1	204	−22	.442	−3.68	5.28	20.8
90	.638	16.9	206	−22	.554	−4.03	5.91	23.7
100	1.35	19.1	212	−23	.622	−4.48	6.93	27.0
120	2.02	22.7	214	−30	.921	−5.79	8.01	31.9
140	3.24	26.7	216	−37	1.11	−6.75	9.29	36.9
160	3.86	30.9	226	−42.6	1.31	−8.02	11.8	42.3
180	5.62	35.0	230	−49.2	1.46	−9.32	13.0	47.3
200	5.31	37.6	226	−52.6	1.93	−11.1	12.5	50.8
225	6.35	41.8	234	−59.5	2.45	−12.9	14.0	56.9
250	8.34	48.6	255	−68.9	2.54	−14.6	16.6	66.7
275	10.0	55.7	262	−85.8	2.98	−17.1	16.4	73.3
300	15.0	63.2	273	−98.9	2.96	−18.5	18.9	82.8
325	18.8	68.6	274	−114	3.15	−21.1	20.7	88.1
350	27.3	77.9	280	−139	2.63	−22.5	23.5	96.4
375	32.2	83.7	284	−143	3.65	−24.9	24.1	99.4
400	37.8	89.5	272	−157	3.80	−26.8	23.5	103
425	50.0	104	309	−198	4.53	−30.8	27.1	114
450	52.9	109	320	−225	4.91	−35.2	33.7	120
475	63.6	113	320	−259	5.55	−39.4	30.8	129
500	77.1	118	324	−328	3.42	−42.2	48.0	143

Conditions: 12.5 V @ 0.50 A

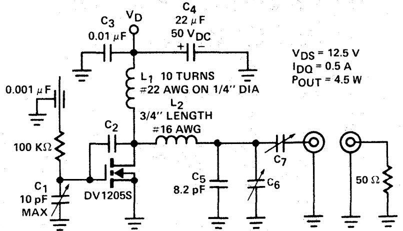
Polar S-Parameters in 50.0 Ohm System

Freq	S_{11}		S_{21}		S_{12}		S_{22}	
(MHz)	(Magn	Angl)	(Magn	Angl)	(Magn	Angl)	(Magn	Angl)
10	.92	−29	15	158	.03	71	.65	−40
20	.91	−47	13.5	145	.05	59	.67	−63
30	.86	−68	12.1	130	.07	46	.72	−87
40	.79	−86	10.1	116	.09	34	.73	−107
50	.74	−99	8.39	108	.09	27	.71	−119
60	.72	−108	7.16	102	.09	22	.73	−127
70	.70	−117	6.14	95	.09	17	.73	−134
80	.69	−124	5.31	92	.10	15	.74	−141
90	.70	−128	4.68	87	.09	11	.74	−143
100	.70	−132	4.15	85	.09	8.7	.75	−147
120	.70	−140	3.31	79	.09	6.2	.76	−152
140	.70	−144	2.78	75	.09	4.0	.76	−155
160	.72	−148	2.36	72	.08	2	.77	−158
180	.72	−152	2.03	69	.08	.4	.78	−160
200	.73	−154	1.79	66	.09	−.5	.79	−162
225	.75	−157	1.56	64	.08	−1.2	.80	−164
250	.76	−160	1.36	61	.08	−3.9	.82	−166
275	.77	−162	1.19	57	.07	−4.6	.82	−167
300	.78	−164	1.05	55	.07	−5.8	.83	−167
325	.78	−166	.93	54	.07	−4.9	.84	−168
350	.79	−168	.84	52	.06	−5.2	.84	−169
375	.81	−169	.75	51	.06	−3.7	.85	−169
400	.81	−170	.69	49	.06	−3.4	.85	−169
425	.83	−172	.62	48	.05	−1.1	.86	−170
450	.84	−173	.58	49	.05	1.8	.86	−172
475	.84	−175	.54	48	.05	4.5	.87	−172
500	.84	−176	.50	48	.05	8.5	.87	−174

Conditions: 12.5 V @ 0.5 A

Applications

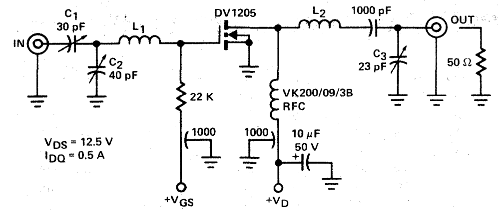
DV1205S 400 MHz Oscillator



Parts List

L_1, 10 turns #22 AWG on 1/4" diameter, close wound
L_2, 3/4" length of #16 AWG
C_6, 1.5 to 20 pF, ARCO #402 trimmer capacitor
C_7, 0.9 to 7 pF, ARCO #400 trimmer capacitor
C_2, Uniceram 47 pFd capacitor with ribbon leads.
Lead length ≈0.25" long and .05" wide.

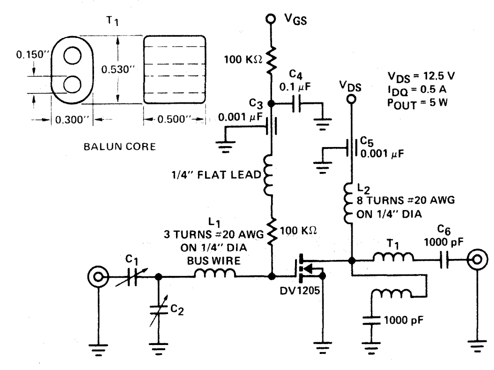
2 Meter Amplifier 5 W Output

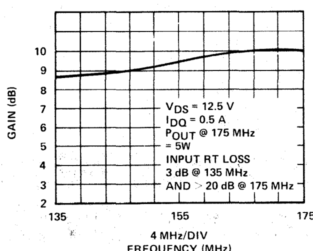


Parts List

L_1, 60 nHy 4T #22 AWG close wound 0.125" I.D.
L_2, 54 nHy 3 1/2T #22 AWG close wound 0.125" I.D.
C_1, C_2, C_3, ARCO #462 5-80 pF

DV1205S 135-175 MHz Amplifier





Parts List

C_1, C_2 ARCO #462, 2 to 80 pF, trimmer capacitors
L_1, 3 turns buss wire #20 AWG on 1/4" diameter
L_2, 8 turns #20 AWG on 1/4" diameter
T_1, 1 turn of 25 Ω coax on 2 balun cores.
Stackpole #57-0973 $\mu o = 35$.

CAUTION: Beryllium Oxide – The top cap of this device is alumina which is harmless. However the ceramic portion between the leads and the metal flange is Beryllium Oxide, the dust of which is toxic. Care must therefore be taken during handling and mounting the device to prevent any damage to this area.

Steps must be taken to ensure that all those who may handle, use, or dispose of this device are aware of its nature and of these necessary safety precautions. In particular the transistor should never be thrown out with general industrial or domestic waste.

DV1210S ▪ DV1210W ▪ DV1210Z

April 1982

N-Channel Enhancement-Mode RF Power FETs

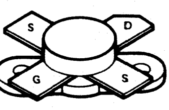
175 MHz **10 W**
10-20 V **10 dB**

Other Devices in Series:
DV1202, DV1205, DV1220, DV1230, DV1240, DV1260

FEATURES

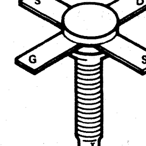
- Infinite VSWR
- No Thermal Runaway
- Broadband Capability
- Class A, B, C, D, E
- Low Noise Figure
- High Dynamic Range
- Simple Bias Circuitry

Package Type S



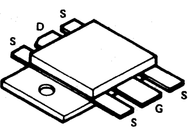
.380 SOE Flange

Package Type Z



.280 SOE Stud

Package Type W



C-220

See page 5-62 for Package Dimensions

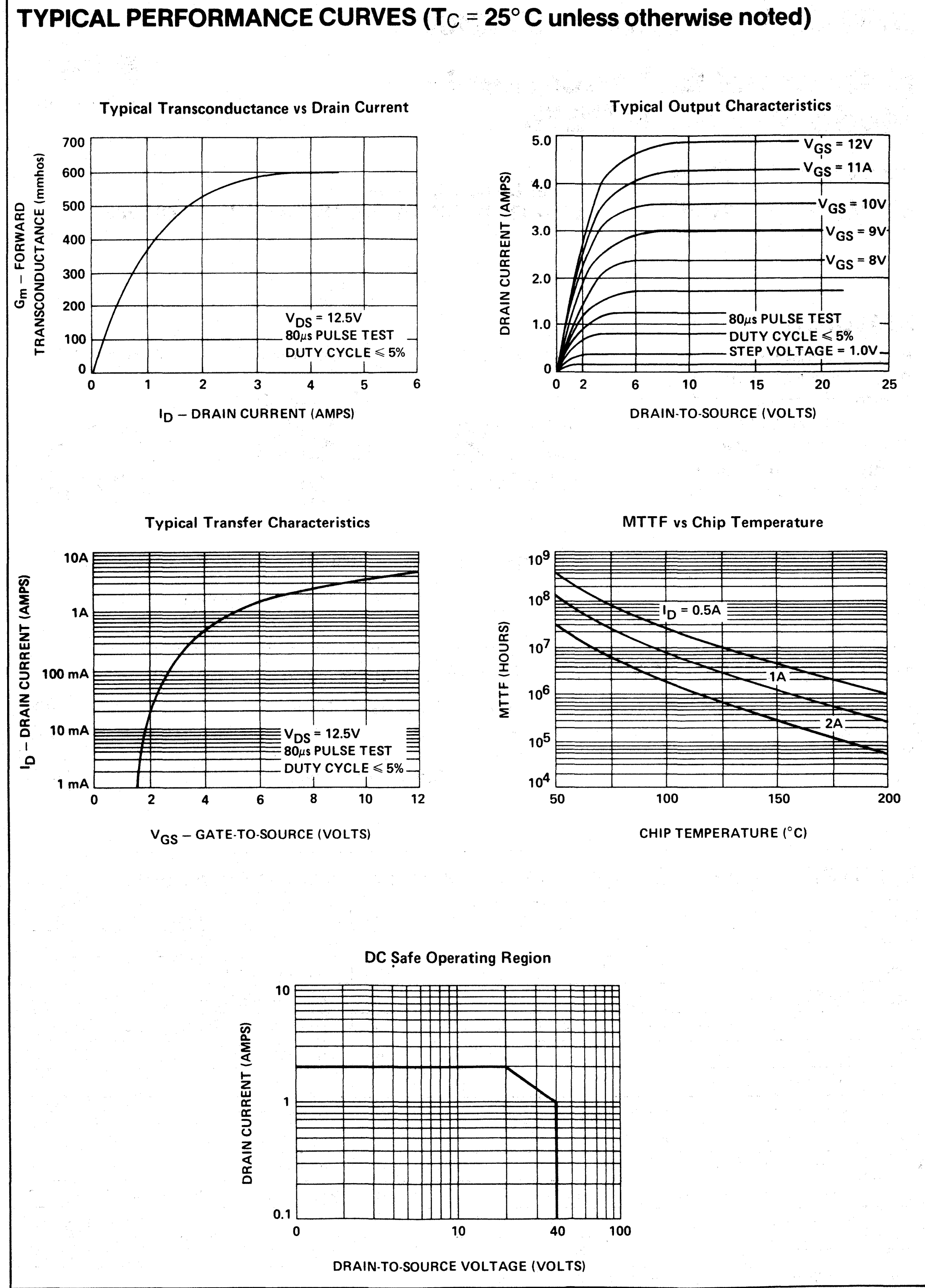
ABSOLUTE MAXIMUM RATINGS (T_C = 25° C unless otherwise noted)

Gate-Source Voltage.................... 30V
Drain-Source Voltage.................. 45V
Drain-Gate Voltage 45V
Drain Current (DC) 2A
Total Device Dissipation 40W
Thermal Resistance, Junction to Case ... 4.4°C/W
Junction Temperature .... 200°C
Storage Temperature .... –65°C to 150°C

ELECTRICAL CHARACTERISTICS (T_C = 25° C unless otherwise noted)

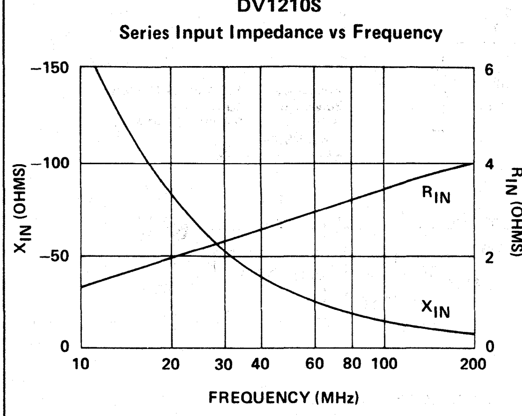
Symbol	Characteristics	Min	Typ	Max	Unit	Test Conditions
BV_{DSS}	Drain-Source Breakdown Voltage	45			V	V_{GS} = 0V, I_D = 5 mA
I_{DSS}	Drain-Source Leakage Current			0.5	mA	V_{GS} = 0V, V_{DS} = 15V
I_{GSS}	Gate-Source Leakage Current			100	nA	V_{GS} = 30V, V_{DS} = 0V
g_m	D.C. Forward Transconductance	0.2	0.4		Mho	V_{DS} = 10V, I_D = 1A, ΔV_{GS} = 1.0V
$I_{D(on)}$	On-State Drain Current		3.5		A	V_{DS} = 12V, V_{GS} = 10V
$V_{GS(th)}$	Gate Threshold Voltage	2		6	V	V_{GS} = V_{DS}, I_D = 100 mA
C_{iss}	Common-Source Input Capacitance			50	pF	V_{GS} = 0V, V_{DS} = 12.5V, f = 1.0 MHz
C_{oss}	Common-Source Output Capacitance			60	pF	V_{GS} = 0V, V_{DS} = 12.5V, f = 1.0 MHz
C_{rss}	Reverse Transfer Capacitance			10	pF	V_{GS} = 0V, V_{DS} = 12.5V, f = 1.0 MHz
G_{ps}	Common-Source Power Gain	10			dB	V_{DD} = 12.5V, Po = 10W, f = 175 MHz, I_{DQ} = 1.0 A
η	Drain Efficiency		65		%	V_{DD} = 12.5V, Po = 10W, f = 175 MHz, I_{DQ} = 1.0A
V_{SWR}	Load Mismatch Tolerance	30:1				V_{DD} = 12.5V, Po = 10W, f = 175 MHz, I_{DQ} = 1.0A

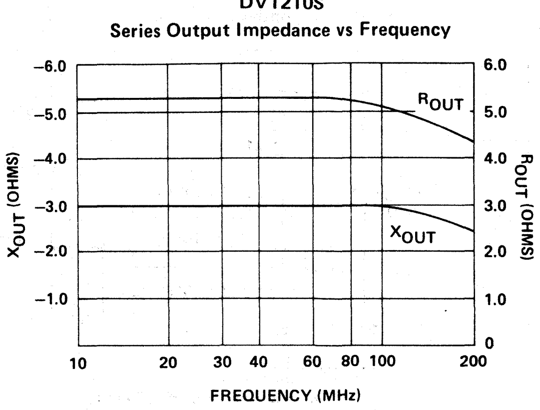
Note 1: Pulse Test—80μs to 300μs, 1% duty cycle



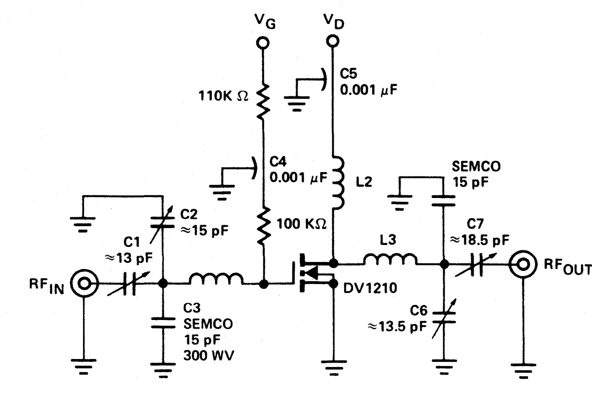
TYPICAL PERFORMANCE CURVES (TC = 25° C unless otherwise noted)
Typical Transconductance vs Drain Current
Gm – FORWARD TRANSCONDUCTANCE (mmhos)
VDS = 12.5V
80μs PULSE TEST
DUTY CYCLE ≤ 5%
ID – DRAIN CURRENT (AMPS)
Typical Output Characteristics
DRAIN CURRENT (AMPS)
VGS = 12V
VGS = 11A
VGS = 10V
VGS = 9V
VGS = 8V
80μs PULSE TEST
DUTY CYCLE ≤ 5%
STEP VOLTAGE = 1.0V
DRAIN-TO-SOURCE (VOLTS)
Typical Transfer Characteristics
ID – DRAIN CURRENT (AMPS)
VDS = 12.5V
80μs PULSE TEST
DUTY CYCLE ≤ 5%
VGS – GATE-TO-SOURCE (VOLTS)
MTTF vs Chip Temperature
MTTF (HOURS)
ID = 0.5A
1A
2A
CHIP TEMPERATURE (°C)
DC Safe Operating Region
DRAIN CURRENT (AMPS)
DRAIN-TO-SOURCE VOLTAGE (VOLTS)

TYPICAL PERFORMANCE CURVES-CONTINUED



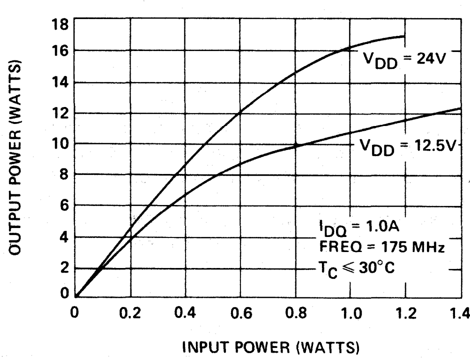


175 MHz TEST FIXTURE

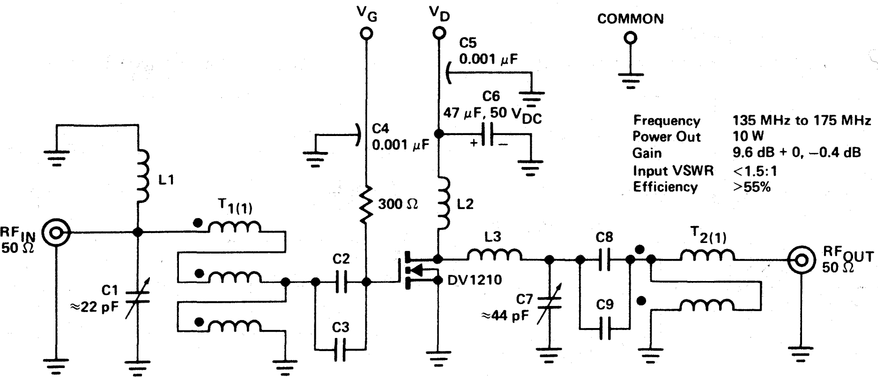


PARTS LIST

C1, C2, C5, C6, Arco #462, 5 to 80 pF
L1, 2 1/2" length of #AWG 12, 1/2 turn on 1/3" diameter
L2, 8 turns #AWG 22 on 1/4" diameter, close wound
L3, 1 5/8" length of #AWG 12, 1/2 turn on 1/3" diameter



APPLICATIONS



PARTS LIST

C1, Arco #462 trimmer capacitor, 5 to 80 pF
C7, Arco #463 trimmer capacitor, 9 to 180 pF
L1, 2 turns, #AWG 22 on 1/4" diameter close wound
L2, 7 turns, #AWG 22 on 1/4" diameter close wound
L3, 1/2" #AWG 18 buss, 1/2-turn on 1/4" diameter

C2, C3, C8, C9, 0.01 μF chip capacitors, Johanson P/N 201 L64 N 103 MA
T1, One turn #22 enamel wire trifilar twisted with 13 crests per inch on one Stackpole balun core #57-0973
T2, One turn 25Ω coax wound on two balun cores placed end on end. Stackpole balun cores #57-0973
(1) — Dot indicates winding starts

CAUTION: Beryllium Oxide — The top cap of this device is alumina which is harmless. However the ceramic portion between the leads and the metal flange is Beryllium Oxide, the dust of which is toxic. Care must therefore be taken during handling and mounting the device to prevent any damage to this area.

Steps must be taken to ensure that all those who may handle, use, or dispose of this device are aware of its nature and of these necessary safety precautions. In particular the transistor should never be thrown out with general industrial or domestic waste.

Siliconix

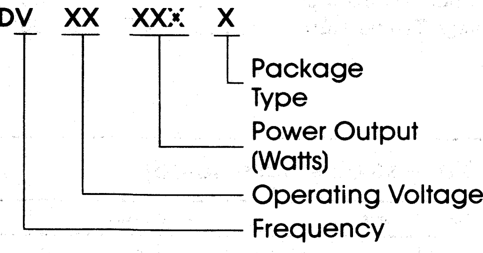
20W Broadband
12.5V
10dB Gain
175MHz

n-channel enhancement-mode RF Power FETs designed for...

HF/VHF/UHF Amplifiers
  Class A, B, or C
High Dynamic Range Amp

Benefits

No Thermal Runaway
Withstands Infinite VSWR
Class A, B, or C Operation
Low Noise Figure
High Dynamic Range
Simple Bias Circuitry

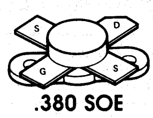


Absolute Maximum Ratings (25°C)

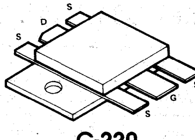
Gate-Source Voltage. . . . . 30 V
Drain-Source Voltage. . . . . 50 V
Drain-Gate Voltage. . . . . 50 V
Drain Current. . . . . 4 A
Total Device Dissipation. . . . . 80 W
  @ 25° Case
θjc for .380 SOE. . . . . 2.2°C/W
θjc for C-220. . . . . 1.76°C/W
Storage Temperature. . . . −65°C to 150°C
Junction Temperature. . . . . 200°C

DV1220S **DV1220W**

See page 5-62 for Package Dimensions



.380 SOE FLANGE



C-220

Electrical Characteristics (25°C)

Symbol	Characteristic	Min	Typ	Max	Unit	Test Conditions
P_{OUT}(1)	Power Output	18	20		W	V_{DD} = 12.5 V, I_{DQ} = 2 A, P_{IN} = 2 W Max, F = 175 MHz
η (1)	Drain Efficiency	55	60		%	
g_m	Transconductance		0.8		Mho	V_{DS} = 12.5 V, I_D = 2 A
C_{oss}	Output Capacity		98		pF	V_{DS} = 12.5 V, V_{GS} = 0 V
C_{rss}	Reverse Transfer Capacity		15			
C_{iss}	Input Capacity		82			
Z_S	Source Impedance		1.6+j6.5		Ω	V_{DS} = 12.5 V, P_{IN} = 2 W
Z_L	Load Impedance		2+j2			F = 175 MHz, P_{OUT} = 20 W

Note: (1) All devices 100% power tested in Siliconix test fixture No. RF12175 [20]

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DV1240T ■ DV1240U ■ DV1240W

N-Channel Enhancement - Mode RF Power FETs

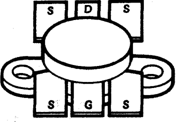
175 MHz
12.5V
40W

Other Devices in Series:
DV1202, DV1205, DV1210, DV1220, DV1230

FEATURES

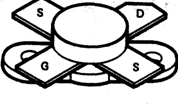
- Infinite VSWR
- No Thermal Runaway
- Broadband Capability
- Class A, B, C, D, E
- Low Noise Figure
- High Dynamic Range
- Simple Bias Circuitry

Package Type T



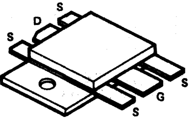
.500 JO Flange

Package Type U



.500 SOE Flange

Package Type W



C-220

See page 5-62 for Package Dimensions

ABSOLUTE MAXIMUM RATINGS (T_C = 25°C unless otherwise noted)

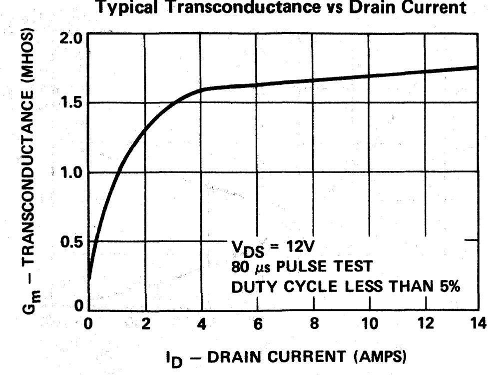
Gate-Source Voltage 30V
Drain-Source Voltage 45V
Drain-Gate Voltage 45V
Drain Current (DC) 8A
Total Device Dissipation 160W
Thermal Resistance, Junction to Case. . . 1.1°C/W
Junction Temperature .... 200°C
Storage Temperature .... –65°C to 150°C

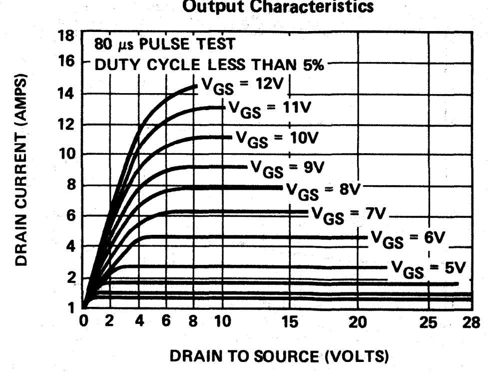
ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

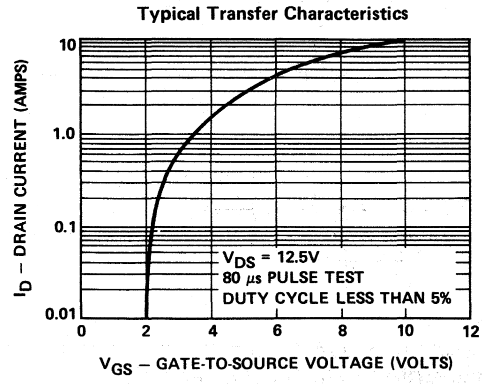
Symbol	Characteristics		Min	Typ	Max	Unit	Test Condition
BV_{DSS}	Drain-Source Breakdown Voltage		45			V	V_{GS} = 0V, I_D = 20 mA
I_{DSS}	Drain-Source Leakage Current				2.0	mA	V_{GS} = 0V, V_{DS} = 15V
I_{GSS}	Gate-Source Leakage Current				100	nA	V_{GS} = 30V, V_{DS} = 0V
g_m	D.C. Forward Transconductance[1]		1.1	1.6		Mho	V_{DS} = 10V, I_D = 4A, ΔV_{GS} = 1.0V
$I_{D(on)}$	On-State Drain Current[1]			12		A	V_{DS} = 12V, V_{GS} = 10V
$V_{GS(th)}$	Gate Threshold Voltage		2		6	V	V_{GS} = V_{DS}, I_D = 400 mA
C_{iss}	Common-Source Input Capacitance				190	pF	V_{GS} = 0V, V_{DS} = 12.5V, f = 1.0 MHz
C_{oss}	Common-Source Output Capacitance				225	pF	V_{GS} = 0V, V_{DS} = 12.5V, f = 1.0 MHz
C_{rss}	Reverse Transfer Capacitance				40	pF	V_{GS} = 0V, V_{DS} = 12.5V, f = 1.0 MHz
G_{ps}	Common-Source Power Gain	1240T,W	9.0			dB	V_{DD} = 12.5V, Po = 40W, f = 175 MHz, I_{DQ} = 4A
		1240U	8.6				
η	Drain Efficiency			65		%	V_{DD} = 12.5, Po = 40W, f = 175 MHz, I_{DQ} = 4A
V_{SWR}	Load Mismatch Tolerance		30:1				V_{DD} = 12.5, Po = 40W, f = 175 MHz, I_{DQ} = 4A

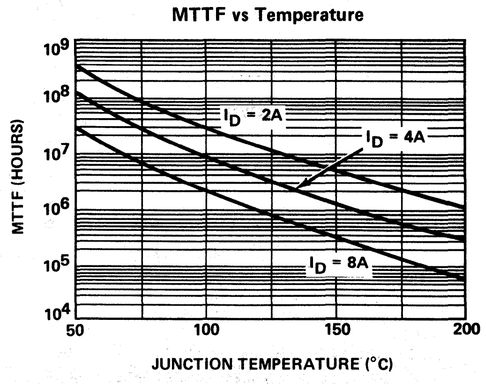
Note 1: Pulse Test—80μs to 300μs, 1% duty cycle

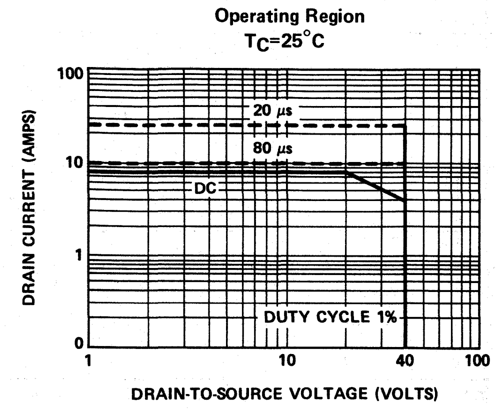
TYPICAL PERFORMANCE CURVES (25°C unless otherwise noted)

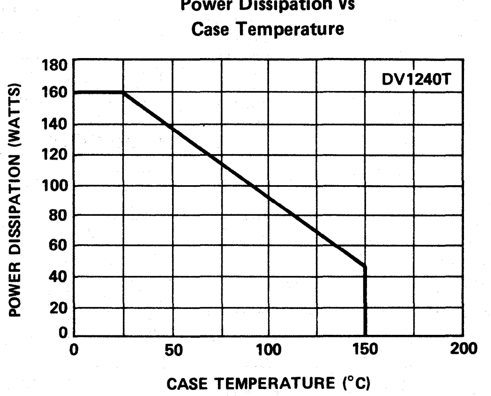




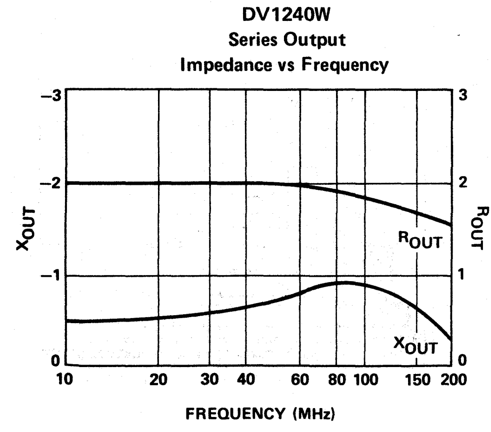


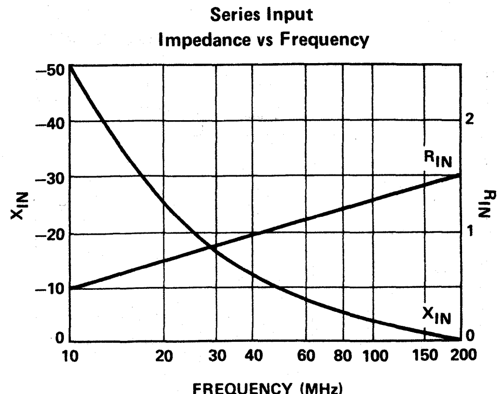




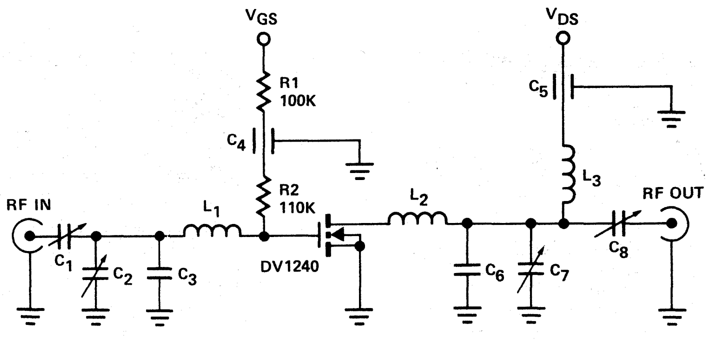


TYPICAL PERFORMANCE CURVES - CONTINUED





175 MHz TEST FIXTURE



NOTES:

C_1, C_8, ARCO #462 TRIMMER CAPACITORS, 5–80pF.

C_2, C_7, ARCO #422 TRIMMER CAPACITORS, 4–40pF.

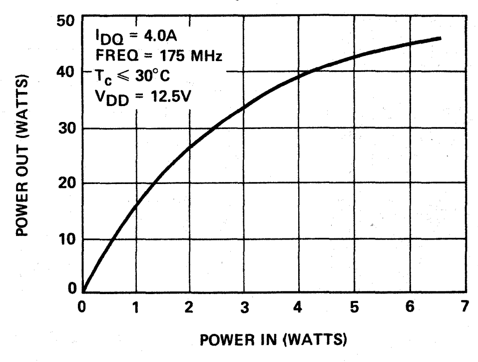
C_3, SEMCO 50pF, POWER CAPACITOR.

C_6, SEMCO 30pF, POWER CAPACITOR.

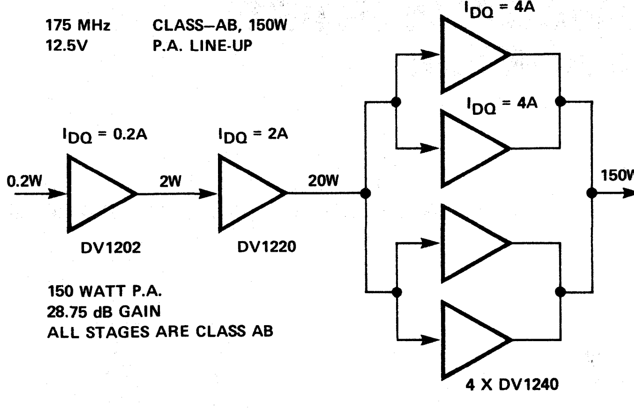
C_4, C_5, .001uF FEED–THRU CAPACITORS.

L_1, L_3, 1" LENGTH OF #12 AWG COPPER WIRE.

L_2, 8–TURNS OF #20 AWG ENAMELED WIRE ON 1/4" DIAMETER, CLOSE WOUND.



TYPICAL AMPLIFIER LINE-UP



CAUTION: Beryllium Oxide – The top cap of this device is alumina which is harmless. However, the ceramic portion between the leads and the metal flange is Beryllium Oxide, the dust of which is toxic. Care must therefore be taken during handling and mounting the device to prevent any damage to this area.

Steps must be taken to ensure that all those who may handle, use, or dispose of this device are aware of its nature and of these necessary safety precautions. In particular the transistor should never be thrown out with general industrial or domestic waste.

DV1260T

Siliconix

N-Channel MOSPOWER FETs Enhancement-Mode

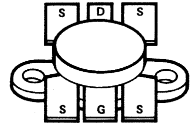
175 MHz
12.5 V
60 W

Other Devices in Series:
DV1202, DV1205, DV1210, DV1220, DV1230, DV1240

FEATURES

- Infinite VSWR
- No Thermal Runaway
- Broadband Capability
- Class A, B, C, D, E
- Low Noise Figure
- High Dynamic Range
- Simple Bias Circuitry

Package Type T



.500 JO Flange

See page 5-62 for Package Dimensions

ABSOLUTE MAXIMUM RATINGS (T_C = 25° C unless otherwise noted)

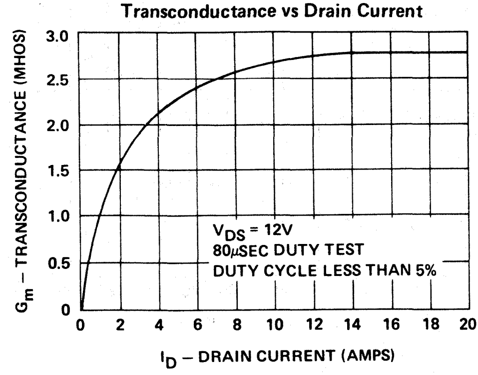
Gate-Source Voltage 30V
Drain-Source Voltage 45V
Drain-Gate Voltage 45V
Drain Current (DC) 12A
Total Device Dissipation 240W
Thermal Resistance, Junction to Case . . . . . . 0.73°C/W
Junction Temperature . . . . 200°C
Storage Temperature . . . . –65°C to 150°C

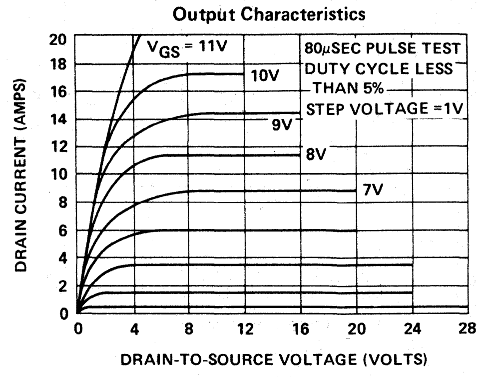
ELECTRICAL CHARACTERISTICS (T_C = 25° C unless otherwise noted)

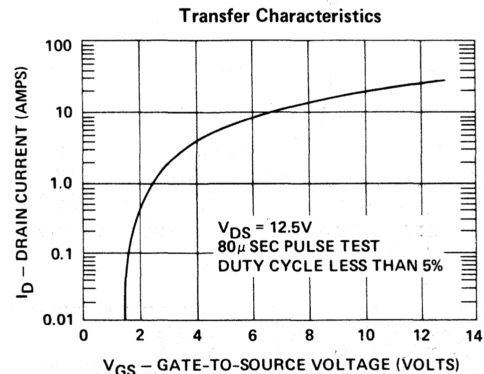
Symbol	Characteristics	Min	Typ	Max	Unit	Test Condition
BV_{DSS}	Drain-Source Breakdown Voltage	45			V	V_{GS} = 0V, I_D = 30 mA
I_{DSS}	Drain-Source Leakage Current			3.0	mA	V_{GS} = 0V, V_{DS} = 15V
I_{GSS}	Gate-Source Leakage Current			100	nA	V_{GS} = 30V, V_{DS} = 0V
g_m	D.C. Forward Transconductance[1]	1.5	2.4		Mho	V_{DS} = 10V, I_D = 6A, ΔV_{GS} = 1.0V
$I_{D(on)}$	On-State Drain Current[1]		20		A	V_{DS} = 12V, V_{GS} = 10V
$V_{GS(th)}$	Gate Threshold Voltage	2		6	V	V_{GS} = V_{DS}, I_D = 600 mA
C_{iss}	Common-Source Input Capacitance			285	pF	V_{GS} = 0V, V_{DS} = 12.5V, f = 1.0 MHz
C_{oss}	Common-Source Output Capacitance			340	pF	V_{GS} = 0V, V_{DS} = 12.5V, f = 1.0 MHz
C_{rss}	Reverse Transfer Capacitance			60	pF	V_{GS} = 0V, V_{DS} = 12.5V, f = 1.0 MHz
G_{ps}	Common-Source Power Gain	8.0			dB	V_{DD} = 12.5V, Po = 60W, f = 175 MHz, I_{DQ} = 6A
η	Drain Efficiency		60		%	V_{DD} = 12.5, Po = 60W, f = 175 MHz, I_{DQ} = 6A
V_{SWR}	Load Mismatch Tolerance	30:1				V_{DD} = 12.5, Po = 60W, f = 175 MHz, I_{DQ} = 6A

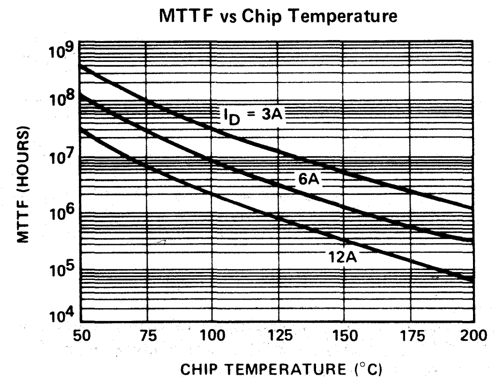
Note 1: Pulse Test—80μs to 300μs, 1% duty cycle

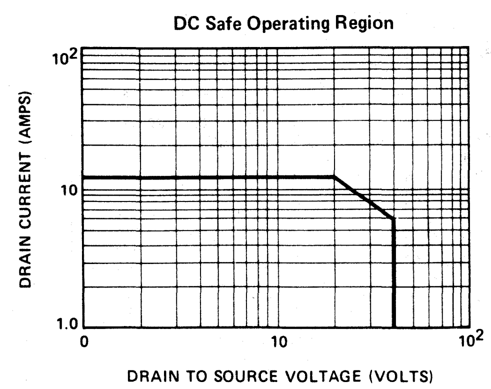
TYPICAL PERFORMANCE CURVES (T_C = 25°C unless otherwise noted)











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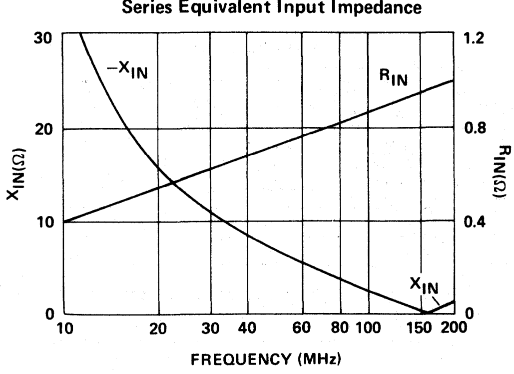
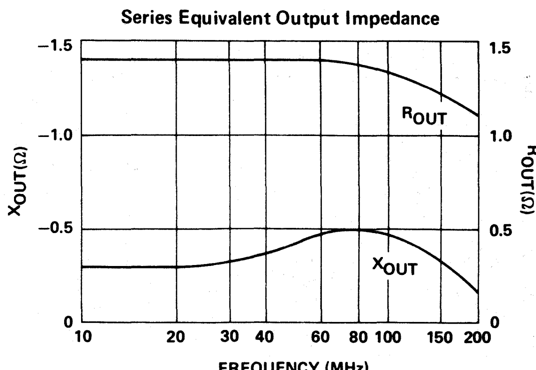
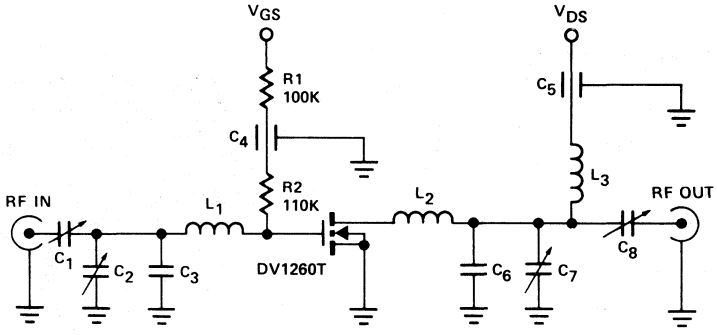
TYPICAL PERFORMANCE CURVES-CONTINUED



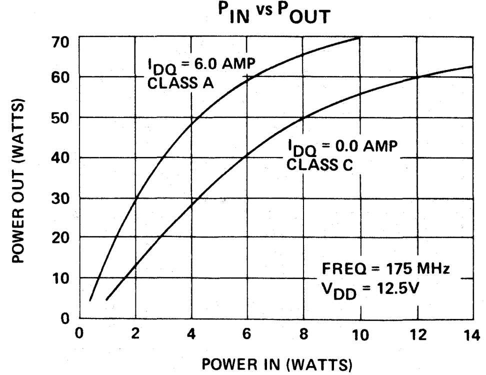


175 MHz TEST FIXTURE

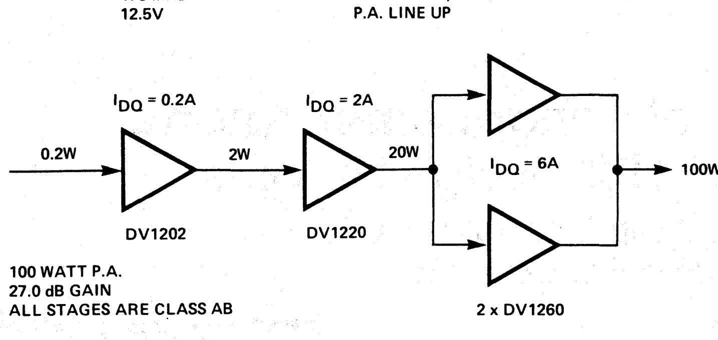


NOTES:

C_1, C_8, ARCO #462 TRIMMER CAPACITORS, 5–80pF.
C_2, C_7, ARCO #422 TRIMMER CAPACITORS, 4–40pF.
C_3, SEMCO 50pF, POWER CAPACITOR.
C_6, SEMCO 30pF, POWER CAPACITOR.
C_4, C_5, .001uF FEED-THRU CAPACITORS.
L_1, L_3, 1" LENGTH OF #12 AWG COPPER WIRE.
L_2, 8–TURNS OF #20 AWG ENAMELED WIRE ON 1/4" DIAMETER, CLOSE WOUND.



TYPICAL AMPLIFIER LINE-UP



CAUTION: Beryllium Oxide – The top cap of this device is alumina which is harmless. However, the ceramic portion between the leads and the metal flange is Beryllium Oxide, the dust of which is toxic. Care must therefore be taken during handling and mounting the device to prevent any damage to this area.

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DV2805S ■ DV2805W

Siliconix

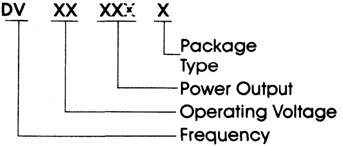
175 MHz
20-35 V
5 W
10 dB

n-channel enhancement-mode RF Power FETs designed for...

HF/VHF/UHF Amplifiers Class A, B, or C
High Dynamic Range Amp

Benefits

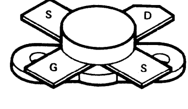
Infinite VSWR
No Thermal Runaway
Broadband Capability
Class A, B, or C Operation
Low Noise Figure
High Dynamic Range
Simple Bias Circuitry
S-Parameter Design
Other devices in series:
DV2810, DV2820, DV2840, DV2880, DV28120



Absolute Maximum Ratings (25°C)

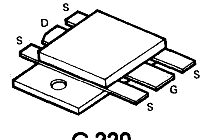
Gate-Source Voltage . . . . 40 V
Drain-Source Voltage . . . . 80 V
Drain-Gate Voltage . . . . 80 V
Drain Current (DC) . . . . 0.5 A
Total Device Dissipation @ 25° Case . . . . 10 W
θjc . . . . 17.6°C/W
Storage Temperature . . . . −65°C to 150°C
Junction Temperature . . . . 200°C

Package Type S



.380 SOE FLANGE

Package Type W



C-220

See page 5-62 for Package Dimensions

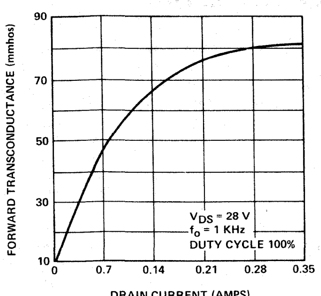
Electrical Characteristics (25°C)

Symbol	Characteristic	Min	Typ	Max	Unit	Test Conditions
P_{OUT}(1)	Power Output	5			W	V_{DS}=28 V, I_{DQ}=0.025 A, P_{IN}=0.5 W, f=175 MHz
η(1)	Drain Efficiency		60		%	
g_m	Transconductance		65		mmho	V_{DS}=0.28 V, I_D=0.125 A
C_{oss}	Output Capacity		11			
C_{rss}	Reverse Transfer Capacity		1.5		pF	V_{DS}=28 V, V_{GS}=0 V
C_{iss}	Input Capacity		12			
NF(2)	Small Signal Noise Figure		6.8		dB	f=175 MHz, V_{DS}=28 V, I_D=0.025 A

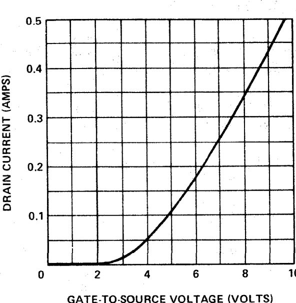
Notes: (1) All devices 100% power tested in Siliconix test fixture No. RF28175 [5]
(2) Noise figure measured with 5 watt power matched source and load

Typical Performance Curves (25°C)

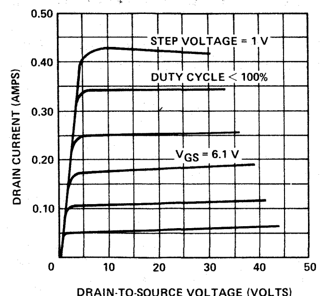
Transconductance vs Drain Current



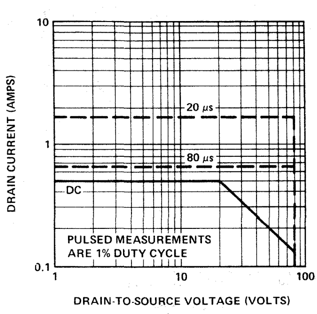
Drain Current vs Gate-to-Source Voltage



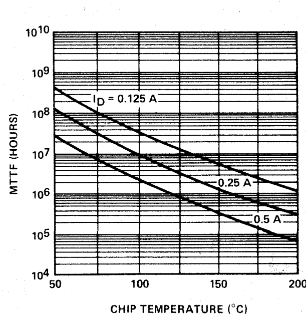
Output Characteristics vs Drain-to-Source Voltage



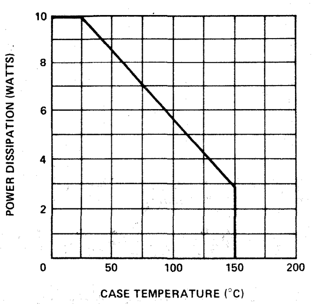
DC and Inductive Safe Operating Region T_C=25°C



MTTF vs Chip Temperature

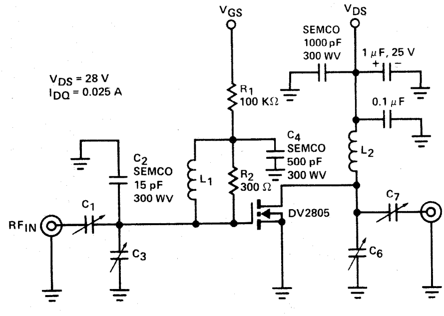


Power Dissipation vs Case Temperature



Test Fixture

DV2805 175 MHz



Parts List

C_3, 80 to 5 pF ARCO #462 trimmer capacitors
C_6, 30 to 2.7 pF ARCO #461 trimmer capacitors
L_1, 1 turn of #18 AWG on 1/4" diameter
L_2, 2 turns of #18 AWG on 1/4" diameter
C_1, 180 to 9 pF ARCO #463 trimmer capacitor

All DV2805s are tested in this test fixture.

Small Signal 2-Port Parameters DV2805S

2-Port Y-Parameter Matrix in Millimhos

Freq (MHz)	Y_{11} (Real	Imag)	Y_{21} (Real	Imag)	Y_{12} (Real	Imag)	Y_{22} (Real	Imag)
10	.095	.660	64.5	−1.84	.001	−.107	.421	.725
20	.067	1.23	65.0	−1.49	.015	−.220	.449	1.18
30	−.147	1.66	70.0	−4.38	.015	−.338	.162	1.50
40	−.129	2.79	65.5	−3.62	.037	−.431	.146	2.62
50	.062	3.65	66.0	−3.97	.064	−.555	.261	3.36
60	.167	4.27	68.0	−5.90	.087	−.705	.298	3.97
70	.049	4.94	67.0	−9.05	.111	−.865	.204	4.47
80	.286	5.90	69.0	−9.55	.141	−.985	.294	5.30
90	.555	6.75	72.5	−10.9	.189	−1.13	.530	6.05
100	.795	7.70	73.5	−13.4	.242	−1.28	.540	6.90
120	1.19	9.45	77.5	−15.7	.332	−1.62	.920	8.35
140	1.54	11.2	80.0	−20.5	.446	−1.98	1.13	9.85
160	2.15	13.2	85.5	−24.7	.575	−2.51	1.25	11.3
180	2.90	14.9	88.0	−31.5	.710	−3.01	1.18	12.8
200	3.35	16.6	89.5	−35.3	.910	−3.51	1.23	14.3
225	3.43	18.6	96.0	−44.0	1.25	−4.27	1.07	16.1
250	6.00	23.0	112	−63.0	1.42	−5.40	−3.64	20.0
275	7.00	26.6	117	−76.5	1.81	−6.85	−1.38	23.3
300	10.3	30.1	119	−98.5	1.87	−8.65	−3.08	27.0
325	16.6	33.1	114	−124	1.58	−9.50	−1.86	32.2
350	22.5	36.2	105	−145	1.37	−11.3	−3.03	36.2
375	27.7	37.3	93.5	−160	1.44	−12.9	−3.90	40.2
400	32.0	38.4	81.0	−170	1.38	−14.3	−3.09	42.8
425	41.3	33.5	49.7	−183	.067	−15.4	−1.99	47.9
450	43.0	31.9	33.0	−179	.122	−16.0	1.61	49.1
475	45.5	29.9	19.2	−182	−.297	−17.3	3.35	53.5
500	46.1	26.2	5.20	−172	.218	−16.9	6.10	52.0

Conditions: 28 V @ 125 mA

Polar S-Parameters in 50.0 Ohm System

Freq (MHz)	S_{11} (Magn	Angl)	S_{21} (Magn	Angl)	S_{12} (Magn	Angl)	S_{22} (Magn	Angl)
10	.99	−6	6.27	173	.01	86	.96	−6
20	.99	−11	6.30	170	.02	85	.96	−11
30	1.0	−16	6.88	164	.03	80	.97	−15
40	1.0	−24	6.32	158	.04	76	.97	−23
50	.98	−30	6.14	152	.05	72	.96	−29
60	.95	−37	6.12	146	.06	68	.94	−35
70	.94	−42	5.92	139	.08	64	.92	−40
80	.91	−49	5.78	134	.08	60	.90	−46
90	.88	−56	5.70	129	.09	57	.87	−52
100	.85	−62	5.47	123	.10	54	.86	−58
120	.81	−74	5.08	114	.11	47	.80	−69
140	.77	−85	4.66	105	.11	42	.76	−79
160	.72	−97	4.29	98	.12	37	.72	−89
180	.68	−106	3.92	90	.13	33	.69	−97
200	.67	−114	3.58	85	.13	31	.68	−104
225	.66	−123	3.35	77	.14	28	.66	−114
250	.59	−142	3.22	66	.14	20	.70	−122
275	.61	−149	2.70	62	.14	20	.64	−133
300	.59	−159	2.41	58	.14	20	.63	−139
325	.57	−165	2.16	54	.12	20	.62	−142
350	.58	−172	1.96	50	.12	21	.61	−145
375	.58	−176	1.79	47	.13	23	.62	−147
400	.59	−179	1.66	46	.13	26	.61	−149
425	.59	175	1.55	43	.13	28	.61	−149
450	.58	174	1.43	42	.13	32	.60	−151
475	.58	172	1.35	41	.13	34	.61	−154
500	.58	172	1.28	39	.13	38	.61	−153

Conditions: 28 V @ 125 mA

Small Signal 2-Port Parameters DV2805W

2-Port Y-Parameter Matrix in Millimhos

Freq (MHz)	Y_{11} (Real	Imag)	Y_{21} (Real	Imag)	Y_{12} (Real	Imag)	Y_{22} (Real	Imag)
10	.281	.543	65.1	−2.91	0	−.105	.599	.712
20	.154	.781	62.8	−3.75	0	−.208	.576	.924
30	.081	1.32	63.6	−3.68	0	−.306	.234	1.48
40	−.178	2.04	64.6	−4.82	.02	−.410	.141	2.20
50	−.151	2.78	65.0	−4.81	.034	−.521	.072	2.94
60	−.191	3.52	65.4	−6.58	.047	−.637	.021	3.50
70	−.139	4.35	63.7	−11.1	.070	−.774	.082	4.32
80	.137	5.03	65.2	−7.48	.105	−.928	.368	4.99
90	.319	5.76	65.9	−7.0	.152	−1.09	.440	5.73
100	.514	6.68	66.9	−6.62	.167	−1.14	.514	6.68
120	.946	8.15	69.2	−7.52	.269	−1.41	.996	8.35
140	1.11	9.70	69.3	−9.74	.332	−1.71	1.11	9.70
160	1.46	10.9	70.8	−9.70	.414	−2.09	1.55	11.2
180	1.53	12.5	71.4	−10.5	.589	−2.43	1.44	12.2
200	2.09	13.9	72.9	−11.7	.624	−2.73	1.97	13.7
225	2.82	15.9	76.0	−12.6	.751	−3.11	2.32	15.5
250	3.50	17.5	78.4	−14.4	.984	−3.79	2.24	17.0
275	3.89	20.0	81.6	−17.1	1.11	−4.40	2.41	19.5
300	5.53	22.7	84.8	−20.6	1.13	−4.76	2.96	21.7
325	6.66	24.7	86.8	−23.6	1.24	−5.46	3.68	23.7
350	8.24	27.5	89.5	−26.2	1.39	−6.19	3.63	25.2
375	10.4	30.5	92.4	−30.4	1.49	−6.54	4.56	27.6
400	11.6	32.6	92.6	−34.1	1.62	−7.13	4.61	29.1
425	13.6	34.9	90.4	−37.8	1.7	−7.76	5.13	29.9
450	16.1	37.0	92.0	−41.2	1.66	−7.86	6.56	31.8
475	17.8	38.7	90.2	−44.3	1.76	−8.38	6.78	32.9
500	21.0	40.8	91.6	−48.6	1.65	−8.48	8.46	35.0

Conditions: 28 V @ 125 mA

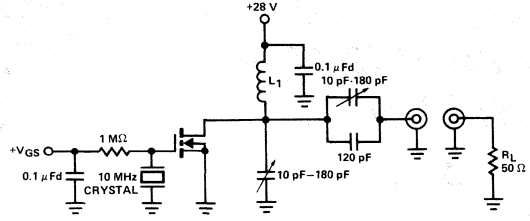
Polar S-Parameters in 50.0 Ohm System

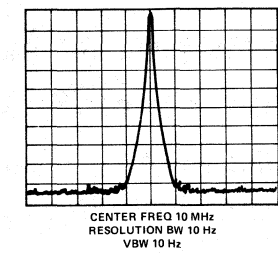
Freq (MHz)	S_{11} (Magn	Angl)	S_{21} (Magn	Angl)	S_{12} (Magn	Angl)	S_{22} (Magn	Angl)
10	.97	−5	6.22	173	.01	86	.94	−6
20	.98	−8	6.03	170	.02	85	.94	−9
30	1.00	−13	6.24	166	.03	82	.97	−14
40	1.00	−19	6.31	160	.04	77	.97	−20
50	.99	−25	6.24	155	.05	73	.97	−26
60	.98	−31	6.17	149	.06	69	.96	−31
70	.95	−37	5.82	140	.07	65	.93	−37
80	.93	−43	5.62	139	.08	62	.91	−43
90	.91	−49	5.43	135	.09	59	.90	−49
100	.89	−54	5.25	131	.09	55	.89	−54
120	.85	−64	4.84	123	.10	50	.85	−65
140	.82	−73	4.42	115	.11	44	.82	−73
160	.79	−81	4.03	110	.12	39	.79	−82
180	.79	−89	3.76	104	.13	36	.79	−88
200	.76	−95	3.43	100	.13	32	.76	−94
225	.74	−103	3.13	95	.13	28	.75	−101
250	.72	−111	2.85	90	.14	25	.75	−108
275	.71	−118	2.57	84	.14	20	.74	−115
300	.69	−124	2.32	80	.13	17	.73	−119
325	.68	−129	2.09	77	.13	15	.72	−124
350	.68	−135	1.91	74	.13	13	.72	−127
375	.68	−139	1.74	71	.12	12	.72	−130
400	.68	−142	1.62	68	.12	11	.72	−132
425	.68	−145	1.48	66	.12	11	.71	−133
450	.68	−147	1.38	65	.11	11	.71	−135
475	.68	−149	1.29	63	.11	11	.71	−136
500	.68	−151	1.20	62	.10	11	.71	−138
700	.65	−163	.77	53	.08	25	.70	−144

Conditions: 28 V @ 125 mA

Applications

DV2805 10 MHz Crystal Oscillator



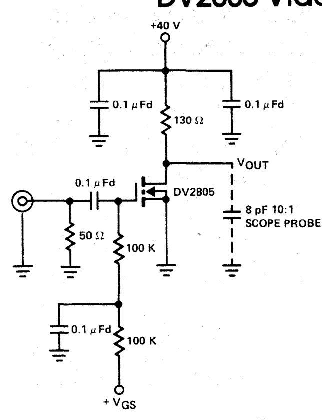


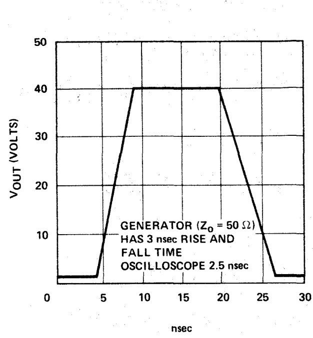
CENTER FREQ 10 MHz
RESOLUTION BW 10 Hz
VBW 10 Hz
SWP 20 sec
SPAN 1 KHz
POWER OUT 5 W
EFFICIENCY 65%

Parts List

L_1 ~ 18 turns #22 enameled wire on micrometals T-50-6 torroid core. ≈ 1.0 μH.

DV2805 Video CRT Driver





CAUTION: Beryllium Oxide – The top cap of this device is alumina which is harmless. However the ceramic portion between the leads and the metal flange is Beryllium Oxide, the dust of which is toxic. Care must therefore be taken during handling and mounting the device to prevent any damage to this area.

Steps must be taken to ensure that all those who may handle, use, or dispose of this device are aware of its nature and of these necessary safety precautions. In particular the transistor should never be thrown out with general industrial or domestic waste.

DV2810S ■ DV2810W

Siliconix

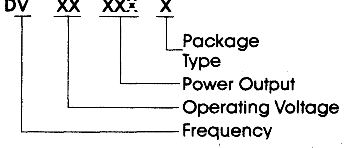
175 MHz
20-35 V
10 W
10 dB

n-channel enhancement-mode RF Power FETs designed for...

HF/VHF/UHF Amplifiers Class A, B, or C
High Dynamic Range Amp

Benefits

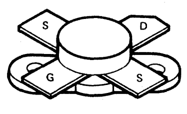
Infinite VSWR
No Thermal Runaway
Broadband Capability
Class A, B, or C Operation
Low Noise Figure
High Dynamic Range
Simple Bias Circuitry
S-Parameter Design
Other devices in series:
DV2805, DV2820, DV2840, DV2880, DV28120



Absolute Maximum Ratings (25°C)

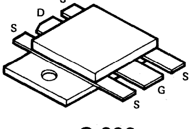
Gate-Source Voltage .... 40 V
Drain-Source Voltage .... 80 V
Drain-Gate Voltage .... 80 V
Drain Current (DC) .... 1 A
Total Device Dissipation .... 20 W
@ 25° Case
θjc .... 8.8°C/W
Storage Temperature .... −65°C to 150°C
Junction Temperature .... 200°C

Package Type S



.380 SOE FLANGE

Package Type W



C-220

See page 5-62 for Package Dimensions

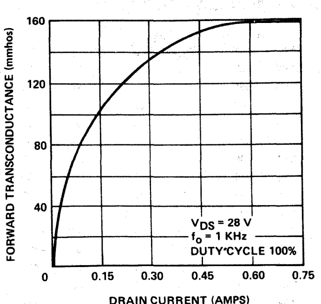
Electrical Characteristics (25°C)

Symbol	Characteristic	Min	Typ	Max	Unit	Test Conditions
P_{OUT}(1)	Power Output	10			W	V_{DS}=28 V, I_{DQ}=0.05 A P_{IN}=1 W, f=175 MHz
η(1)	Drain Efficiency		60		%	
g_m	Transconductance		130		mmho	V_{DS}=28 V, I_D=0.25 A
C_{oss}	Output Capacity		21		pF	V_{DS}=28 V, V_{GS}=0 V
C_{rss}	Reverse Transfer Capacity		3		pF	V_{DS}=28 V, V_{GS}=0 V
C_{iss}	Input Capacity		22		pF	V_{DS}=28 V, V_{GS}=0 V
NF(2)	Small Signal Noise Figure		6.8		dB	f=175 MHz, V_{DS}=28 V I_D=0.05 A

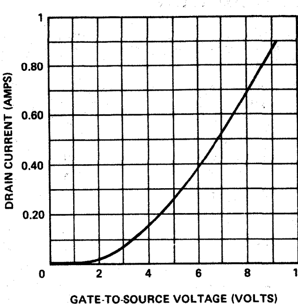
Notes: (1) All devices 100% power tested in Siliconix test fixture No. RF28175 [10]
(2) Noise figure measured with 10 watt power matched source and load

Typical Performance Curves (25°C)

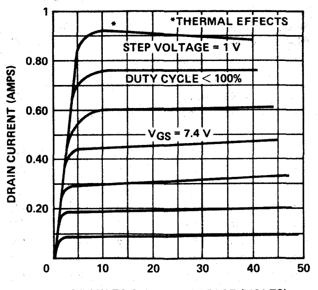
Transconductance vs Drain Current



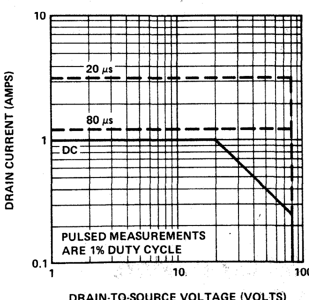
Drain Current vs Gate-to-Source Voltage



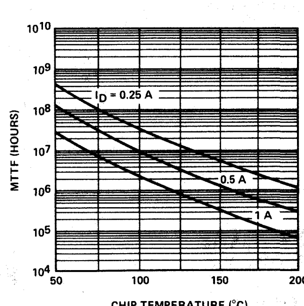
Output Characteristics vs Drain-to-Source Voltage



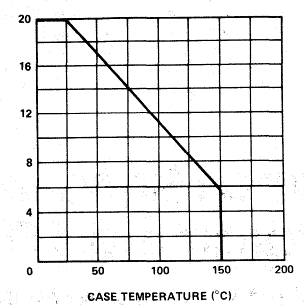
DC and Inductive Safe Operating Region TC=25°C



MTTF vs Chip Temperature

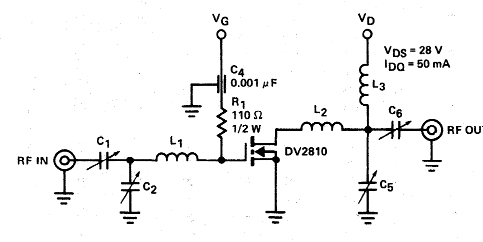


Power Dissipation vs Case Temperature



Test Fixture

DV2810 175 MHz



Parts List

C_1, C_2, C_3, C_4, 5 to 80 pF, ARCO #462 trimmer capacitors
L_1, 4 turns #18 AWG on 1/8" diameter, close wound
L_2, 4 turns #16 AWG on 1/8" diameter, close wound
L_3, 10 turns #20 AWG on 1/4" diameter, close wound

All DV2810s are tested in this test fixture.

Small Signal 2-Port Parameters DV2810S

2-Port Y-Parameter Matrix in Millimhos

Freq (MHz)	Y_{11} (Real	Imag)	Y_{21} (Real	Imag)	Y_{12} (Real	Imag)	Y_{22} (Real	Imag)
10	.189	1.32	129	−3.67	.002	−.214	.842	1.45
20	.134	2.46	130	−2.97	.030	−.440	.897	2.35
30	−.293	3.32	140	−8.76	.030	−.675	.323	2.99
40	−.257	5.58	131	−7.23	.073	−.862	.291	5.23
50	.123	7.29	132	−7.93	.128	−1.11	.521	6.72
60	.334	8.53	136	−11.8	.174	−1.41	.595	7.93
70	.098	9.88	134	−18.1	.221	−1.73	.408	8.94
80	.572	11.8	138	−19.1	.281	−1.97	.588	10.6
90	1.11	13.5	145	−21.7	.377	−2.26	1.06	12.1
100	1.59	15.4	147	−26.7	.483	−2.56	1.08	13.8
120	2.38	18.9	155	−31.3	.664	−3.24	1.84	16.7
140	3.08	22.3	160	−40.9	.891	−3.96	2.26	19.7
160	4.3	26.3	171	−49.3	1.15	−5.01	2.49	22.6
180	5.79	29.7	176	−63	1.42	−6.01	2.36	25.6
200	6.69	33.2	179	−70.6	1.82	−7.02	2.45	28.5
225	6.85	37.2	192	−88	2.50	−8.54	2.13	32.2
250	12.0	45.9	224	−126	2.84	−10.8	−.727	39.9
275	14.0	53.1	234	−153	3.62	−13.7	−2.75	46.5
300	20.6	60.1	237	−197	3.73	−17.3	−6.15	54.0
325	33.2	66.2	227	−248	3.15	−19	−3.71	64.4
350	45.0	72.3	209	−289	2.74	−22.5	−6.06	72.4
375	55.4	74.6	187	−319	2.88	−25.8	−7.8	80.3
400	64	76.8	162	−339	2.76	−28.5	−6.18	85.6
425	82.5	67	99.4	−365	.133	−30.8	−3.98	95.8
450	85.9	63.8	66	−358	.243	−32.0	3.21	98.1
475	91	59.7	38.4	−364	−.593	−34.5	6.7	107
500	92.1	52.3	10.4	−343	.436	−33.8	12.2	104

Conditions: 28 V @ 250 mA

Polar S-Parameters in 50.0 Ohm System

Freq (MHz)	S_{11} (Magn	Angl)	S_{21} (Magn	Angl)	S_{12} (Magn	Angl)	S_{22} (Magn	Angl)
10	.97	−15	12.02	167	.02	79	.91	−16
20	.97	−29	11.75	158	.04	73	.90	−29
30	.96	−43	12.45	147	.06	63	.90	−42
40	.93	−57	10.59	135	.07	53	.88	−56
50	.88	−70	9.44	126	.08	46	.84	−68
60	.83	−81	8.61	118	.09	40	.80	−79
70	.80	−90	7.76	110	.10	35	.76	−87
80	.77	−99	7.0	104	.10	30	.74	−95
90	.75	−107	6.38	99	.10	27	.72	−103
100	.73	−114	5.75	93	.10	24	.71	−109
120	.72	−125	4.79	86	.10	19	.69	−120
140	.71	−133	4.07	79	.10	16	.68	−128
160	.71	−142	3.47	74	.10	13	.68	−136
180	.70	−148	3.02	69	.10	12	.68	−141
200	.71	−152	2.66	65	.10	11	.69	−145
225	.72	−157	2.37	60	.10	11	.70	−151
250	.72	−165	2.07	55	.09	9	.72	−156
275	.73	−169	1.78	51	.09	9	.73	−160
300	.73	−174	1.57	49	.09	11	.73	−163
325	.73	−176	1.40	46	.08	13	.74	−164
350	.74	−179	1.26	44	.08	15	.74	−165
375	.75	179	1.14	42	.08	18	.75	−166
400	.76	178	1.05	41	.08	21	.75	−167
425	.76	175	.98	40	.08	25	.75	−167
450	.76	175	.91	39	.08	29	.75	−168
475	.76	174	.85	38	.08	31	.76	−169
500	.76	174	.81	37	.08	36	.76	−169

Conditions: 28 V @ 250 mA

Small Signal 2-Port Parameters DV2810W

2-Port Y-Parameter Matrix in Millimhos

Freq (MHz)	Y_{11} (Real	Imag)	Y_{21} (Real	Imag)	Y_{12} (Real	Imag)	Y_{22} (Real	Imag)
10	.562	1.09	130	−5.82	0	−.210	1.20	1.42
20	.308	1.56	126	−7.50	0	−.416	1.15	1.85
30	.162	2.64	127	−7.36	0	−.612	.468	2.96
40	−.356	4.08	129	−9.64	.04	−.820	.282	4.40
50	−.302	5.56	130	−9.62	.068	−1.04	.144	5.88
60	−.382	7.04	131	−13.2	.094	−1.27	.042	7.00
70	−.278	8.70	127	−22.2	.140	−1.55	.164	8.64
80	.274	10.1	130	−15.0	.210	−1.86	.736	9.98
90	.638	11.5	132	−14.0	.304	−2.18	.880	11.5
100	1.03	13.4	134	−13.2	.334	−2.28	1.03	13.4
120	1.89	16.3	138	−15.0	.538	−2.82	1.99	16.7
140	2.22	19.4	139	−19.5	.664	−3.42	2.22	19.4
160	2.92	21.8	142	−19.4	.828	−4.18	3.10	22.4
180	3.06	25.0	143	−21.0	1.18	−4.86	2.88	24.4
200	4.18	27.8	146	−23.4	1.25	−5.46	3.94	27.4
225	5.64	31.8	152	−25.2	1.50	−6.22	4.64	31.0
250	7.0	35.0	157	−28.8	1.97	−7.58	4.48	34.0
275	7.78	40.0	163	−34.2	2.22	−8.80	4.82	39.0
300	11.1	45.4	170	−41.2	2.26	−9.52	5.92	43.4
325	13.3	49.4	174	−47.2	2.48	−10.9	7.36	47.4
350	16.5	55.0	179	−52.4	2.78	−12.4	7.26	50.4
375	20.8	60.9	185	−60.8	2.97	−13.1	9.12	55.1
400	23.2	65.2	185	−68.2	3.24	−14.3	9.22	58.2
425	27.2	69.8	181	−75.6	3.40	−15.5	10.3	59.8
450	32.2	74.0	184	−82.4	3.32	−15.7	13.1	63.6
475	35.6	77.4	180	−88.6	3.52	−16.8	13.6	65.8
500	42.0	81.6	183	−97.2	3.30	−17.0	16.9	70.0

Conditions: 28 V @ 0.5 A

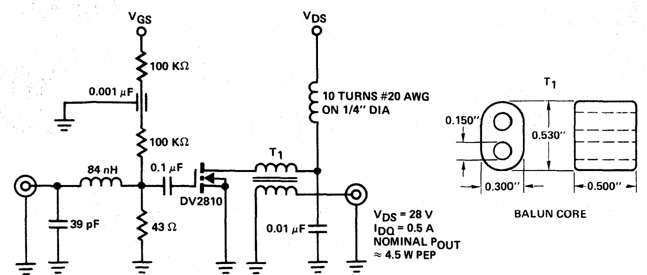
Polar S-Parameters in 50.0 Ohm System

Freq (MHz)	S_{11} (Magn	Angl)	S_{21} (Magn	Angl)	S_{12} (Magn	Angl)	S_{22} (Magn	Angl)
10	.93	−14	11.77	167	.02	80	.88	−16
20	.94	−23	11.26	161	.04	74	.87	−25
30	.92	−35	11.28	152	.05	65	.90	−37
40	.93	−49	10.98	140	.07	57	.89	−51
50	.89	−61	10.11	131	.08	49	.86	−63
60	.85	−72	9.29	122	.09	42	.82	−73
70	.79	−81	8.05	112	.10	37	.76	−82
80	.78	−91	7.19	109	.10	32	.76	−91
90	.76	−99	6.46	105	.11	29	.75	−99
100	.75	−104	5.93	100	.10	24	.75	−104
120	.74	−114	4.9	93	.10	20	.74	−115
140	.73	−122	4.14	86	.10	15	.73	−122
160	.72	−128	3.52	82	.10	11	.73	−129
180	.74	−134	3.11	77	.11	9	.74	−133
200	.74	−138	2.73	75	.10	7	.73	−137
225	.74	−143	2.37	71	.10	4	.75	−141
250	.75	−148	2.07	68	.10	3	.76	−145
275	.75	−151	1.80	64	.10	0	.77	−149
300	.76	−154	1.59	61	.09	−2	.78	−150
325	.76	−157	1.40	60	.09	−2	.78	−153
350	.77	−160	1.26	58	.09	−3	.79	−155
375	.78	−161	1.13	56	.08	−3	.80	−156
400	.79	−163	1.04	52	.08	−4	.80	−157
425	.79	−164	.95	52	.08	−3	.80	−157
450	.80	−165	.87	51	.07	−2	.80	−158
475	.80	−166	.81	50	.07	−2	.81	−159
500	.80	−167	.75	50	.06	−1	.81	−160

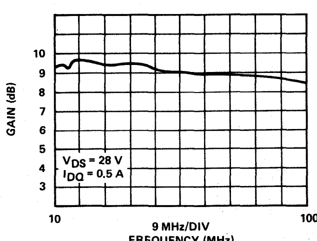
Conditions: 28 V @ 0.5 A

Applications

DV2810 28 V Wideband Amplifier



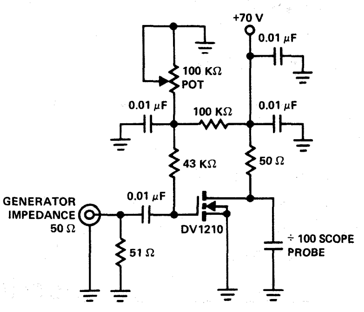
Gain vs Frequency (Nominal POUT=9.5)



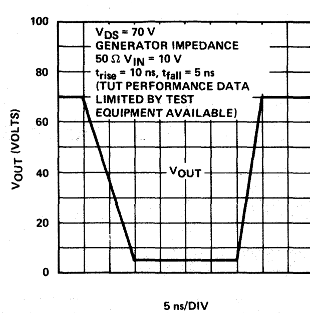
Parts List

T_1, 2 turns 50 Ω coax on 3-balun cores stackpole 57-0973, $\mu o = 35$

DV2810 70 V CRT Driver



tON and tOFF vs Voltage



CAUTION: Beryllium Oxide – The top cap of this device is alumina which is harmless. However the ceramic portion between the leads and the metal flange is Beryllium Oxide, the dust of which is toxic. Care must therefore be taken during handling and mounting the device to prevent any damage to this area.

Steps must be taken to ensure that all those who may handle, use, or dispose of this device are aware of its nature and of these necessary safety precautions. In particular the transistor should never be thrown out with general industrial or domestic waste.

DV2820S ■ DV2820W ■ DV2820Z

Siliconix

N-Channel Enhancement - Mode RF Power FETs

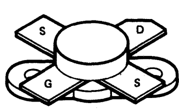
175MHz
20-35V
20W
10dB

Other Devices in Series:
DV2805, DV2810, DV2840, DV2880, DV28120

FEATURES

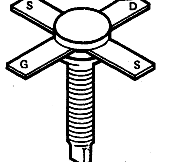
- Infinite VSWR
- No Thermal Runaway
- Broadband Capability
- Class A, B, C, D, E
- Low Noise Figure
- High Dynamic Range
- Simple Bias Circuitry
- S-Parameter Design

Package Type S



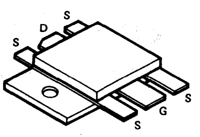
.380 SOE Flange

Package Type Z



.280 SOE Stud

Package Type W



C-220

See page 5-62 for Package Dimensions

ABSOLUTE MAXIMUM RATINGS (T_C = 25°C unless otherwise noted)

Gate-Source Voltage 40V
Drain-Source Voltage 80V
Drain-Gate Voltage 80V
Drain Current (DC) 2A

Total Device Dissipation 40W
Thermal Resistance, Junction to Case . . 4.4°C/W
Junction Temperature . . . . 200°C
Storage Temperature . . . . −65°C to 150°C

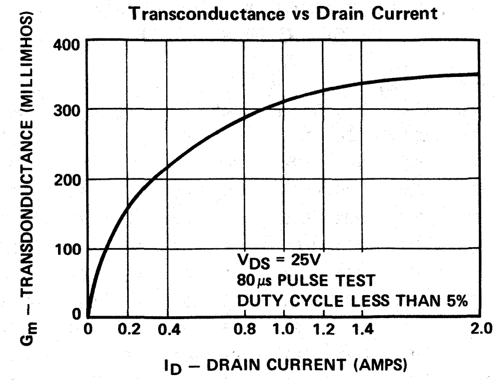
ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

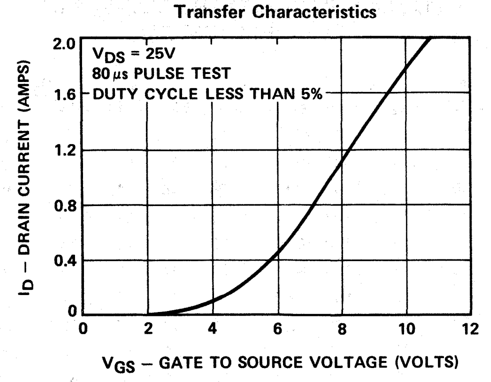
Symbol	Characteristics	Min	Typ	Max	Unit	Test Conditions
BV_{DSS}	Drain-Source Breakdown Voltage	80			V	V_{GS} = 0V, I_D = 5 mA
I_{DSS}	Drain-Source Leakage Current			1	mA	V_{GS} = 0V, V_{DS} = 30V
I_{GSS}	Gate-Source Leakage Current			100	nA	V_{GS} = 40V, V_{DS} = 0V
g_m	D.C. Forward Transconductance[1]	0.2	0.3		mho	V_{DS} = 10V, I_D = 1A, ΔV_{GS} = 1.0V
$I_{D(on)}$	On-State Drain Current[1]		1.8		A	V_{DS} = 30V, V_{GS} = 10V
$V_{GS(th)}$	Gate Threshold Voltage	2		6	V	V_{GS} = V_{DS}, I_D = 100 mA
C_{iss}	Common-Source Input Capacitance			50	pF	V_{GS} = 0V, V_{DS} = 30V, f = 1.0 MHz
C_{oss}	Common-Source Output Capacitance			40	pF	V_{GS} = 0V, V_{DS} = 30V, f = 1.0 MHz
C_{rss}	Reverse Transfer Capacitance			7.5	pF	V_{GS} = 0V, V_{DS} = 30V, f = 1.0 MHz
G_{ps}	Common-Source Power Gain	10			dB	V_{DD} = 28V, Po = 20W, f = 175 MHz, I_{DQ} = 0.1A
η	Drain Efficiency		65		%	V_{DD} = 28V, Po = 20W, f = 175 MHz, I_{DQ} = 0.1A
V_{SWR}	Load Mismatch Tolerance	30:1				V_{DD} = 28V, Po = 20W, f = 175 MHz, I_{DQ} = 0.1A
N.F.	Noise Figure		5.6		dB	V_{DS} = 28V, I_D = 0.1A, f = 175 MHz

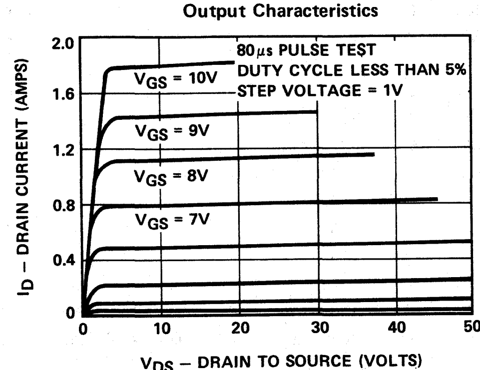
Note 1: Pulse Test—80μs to 300μs, 1% duty cycle

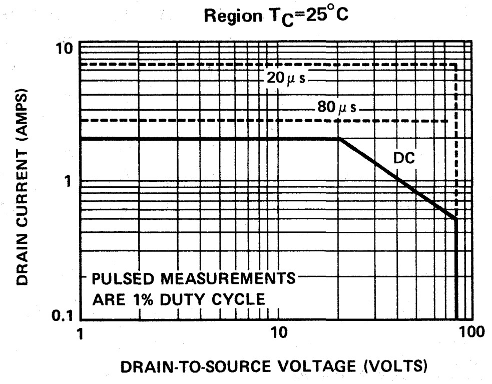
6VNR

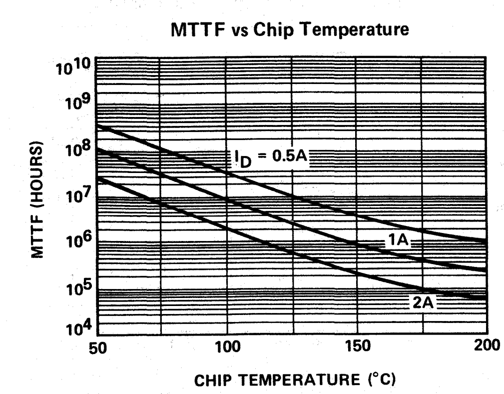
TYPICAL PERFORMANCE CURVES (25°C unless otherwise noted)

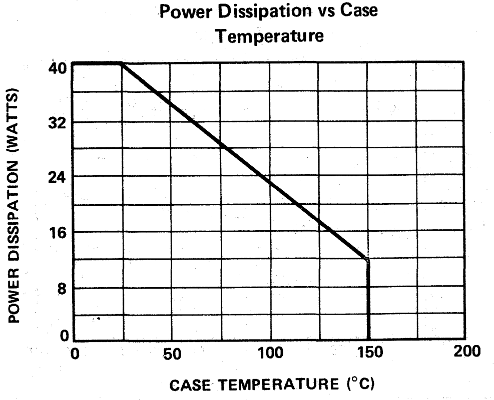












SMALL SIGNAL 2-PORT PARAMETERS

POLAR S-PARAMETERS DV2820S IN 50.0 OHM SYSTEM

Freq (MHz)	S_{11} (Magn	Angl)	S_{21} (Magn	Angl)	S_{12} (Magn	Angl)	S_{22} (Magn	Angl)
10	.93	−36	22.13	150	.03	63	.83	−35
20	.89	−67	18.84	134	.05	50	.78	−65
30	.84	−91	15.85	124	.06	41	.72	−85
40	.79	−107	12.59	113	.06	32	.69	−102
50	.76	−120	10.00	99	.07	19	.65	−114
60	.73	−129	8.41	91	.07	15	.62	−121
70	.72	−137	7.5	85	.07	12	.62	−128
80	.72	−142	6.31	80	.07	9	.62	−133
90	.72	−147	5.31	76	.06	8	.62	−139
100	.72	−151	5.01	73	.06	7	.62	−142
120	.73	−156	3.98	66	.06	6	.64	−148
140	.75	−162	3.35	61	.06	6	.66	−153
160	.76	−166	2.82	56	.06	7	.68	−157
180	.78	−169	2.37	53	.05	11	.71	−162
200	.79	−173	2.04	50	.05	14	.73	−165
225	.80	−175	1.78	45	.05	17	.78	−168
250	.81	180	1.51	40	.05	21	.78	−171
275	.82	175	1.29	37	.05	26	.79	−174
300	.82	173	1.12	35	.05	30	.80	−175
325	.83	171	.99	33	.05	36	.80	−176
350	.84	170	.87	31	.05	40	.81	−176
375	.84	169	.79	30	.06	45	.82	−177

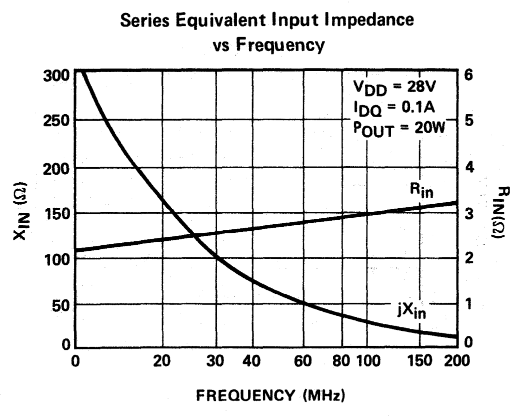
Conditions: 28V @ 450 mA

POLAR S-PARAMETERS DV2820W IN 50.0 OHM SYSTEM

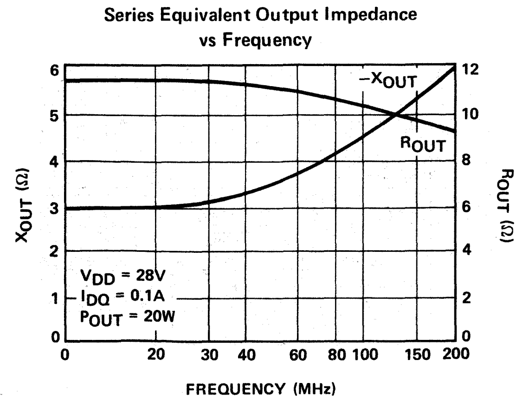
Freq (MHz)	S_{11} (Magn	Angl)	S_{21} (Magn	Angl)	S_{12} (Magn	Angl)	S_{22} (Magn	Angl)
10	.94	−34	20.89	155	.03	66	.84	−33
20	.92	−61	17.78	137	.05	51	.80	−58
30	.88	−85	14.96	122	.06	37	.76	−80
40	.83	−103	12.30	110	.07	27	.72	−95
50	.79	−115	10.00	102	.07	19	.69	−107
60	.77	−124	8.41	96	.07	15	.67	−116
70	.76	−131	7.24	89	.07	12	.66	−123
80	.76	−137	6.31	85	.07	7	.66	−127
90	.75	−141	5.62	81	.07	5	.66	−131
100	.75	−144	4.95	77	.07	3	.66	−135
120	.76	−151	3.98	72	.07	1	.68	−140
140	.78	−155	3.16	67	.06	−1	.70	−144
160	.79	−159	2.82	64	.06	−3	.71	−149
180	.79	−162	2.37	60	.06	−5	.73	−152
200	.80	−164	2.07	57	.06	−5	.75	−154
225	.81	−167	1.76	53	.06	−6	.77	−156
250	.82	−171	1.51	50	.05	−7	.78	−159
275	.83	−174	1.30	47	.05	−6	.79	−161
300	.84	−174	1.14	45	.05	−5	.82	−161
325	.84	−176	1.00	42	.05	−3	.82	−162
350	.85	−178	.88	41	.04	−1	.83	−163
375	.86	179	.79	40	.04	2	.84	−164
400	.88	175	.74	39	.04	5	.86	−165
425	.88	173	.66	39	.04	9	.86	−166
450	.88	172	.61	39	.04	14	.86	−168
475	.87	170	.57	38	.03	18	.86	−169
500	.87	168	.53	38	.03	24	.86	−172

Conditions: 28V @ 450 mA

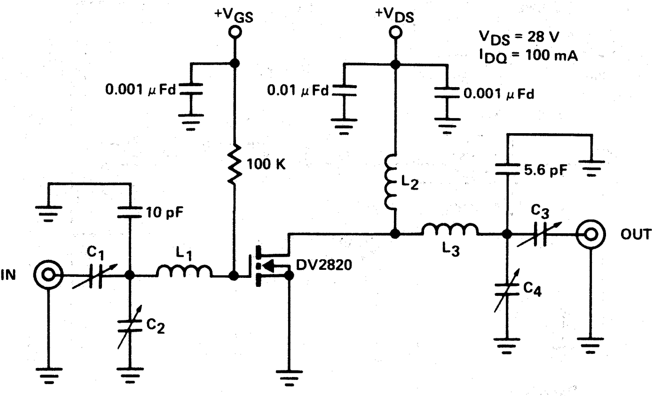
Series Equivalent Input Impedance vs Frequency



Series Equivalent Output Impedance vs Frequency



TEST FIXTURE

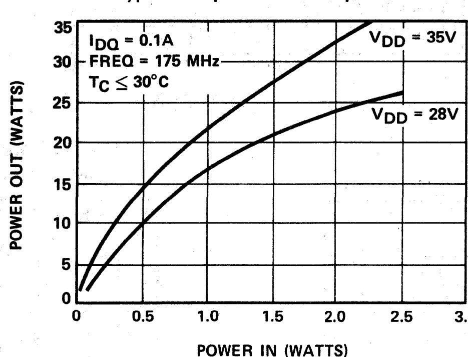


Parts List

C_1, C_3, 5–80 pFd
C_2, C_4, 3–30 pFd
L_1, L_3, 2 turns #20 enamel wire, close wound on 1/4" dia.
L_2, 7 turns #20 enamel wire, close wound on 1/4" dia.

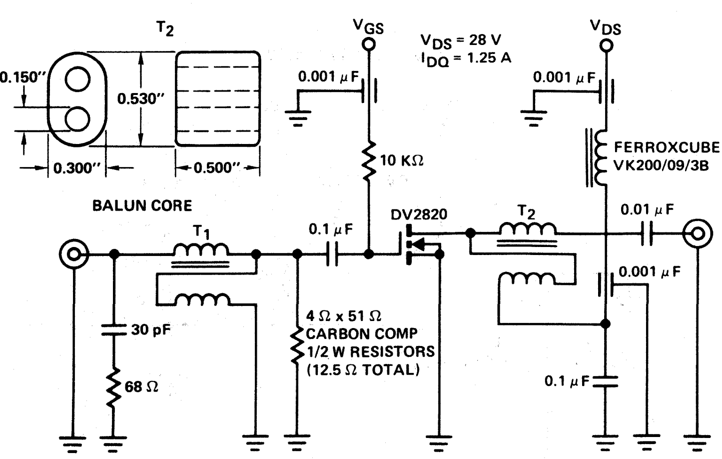
All DV2820s are tested in this test fixture.

Typical Output Power vs Input Power



APPLICATIONS

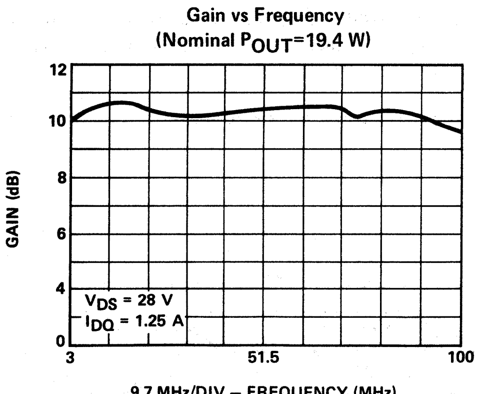
28V WIDEBAND AMPLIFIER



Parts List

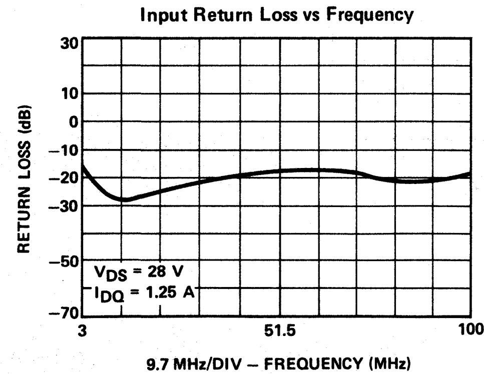
T_1, 20 turns 30 Ω, #30 bifilar on micrometals T-50-6 Toroid
T_2, 1 turn of 2-50 Ω coax cables in parallel through 2 balun cores stackpole #57-9130 μo = 125

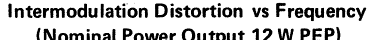
Gain vs Frequency
(Nominal P_{OUT}=19.4 W)

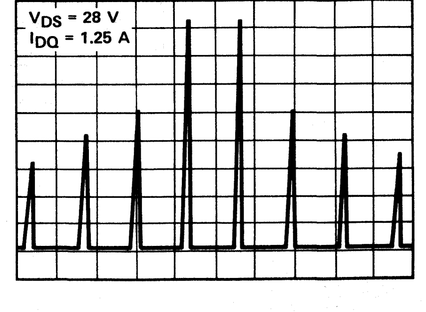


9.7 MHz/DIV – FREQUENCY (MHz)

Input Return Loss vs Frequency







TONE SPACING = 30 KHz

DV2840S ■ DV2840T ■ DV2840W

N-Channel Enhancement - Mode RF Power FETs

Siliconix

175 MHz
20-35 V
40 W
10 dB

Other Devices in Series:
DV2805, DV2810, DV2820, DV2880, DV28120

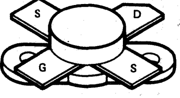
FEATURES

- Infinite VSWR
- No Thermal Runaway
- Broadband Capability
- Class A, B, C, D, E
- Low Noise Figure
- High Dynamic Range
- Simple Bias Circuitry
- S-Parameter Design

Package Type T

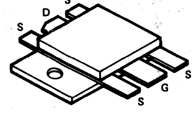
.500 SOE Flange

Package Type S



.380 SOE Flange

Package Type W



C-220

See page 5-62 for Package Dimensions

ABSOLUTE MAXIMUM RATINGS (T_C = 25° C unless otherwise noted)

Gate-Source Voltage	40V	Total Device Dissipation	80 W
Drain-Source Voltage	80V	Thermal Resistance, Junction to Case	2.2°C/W
Drain-Gate Voltage	80V	Junction Temperature	200°C
Drain Current (DC)	4 A	Storage Temperature	−65°C to 150°C

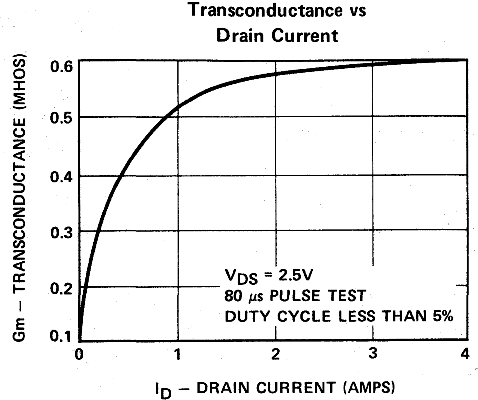
ELECTRICAL CHARACTERISTICS (T_C = 25° C unless otherwise noted)

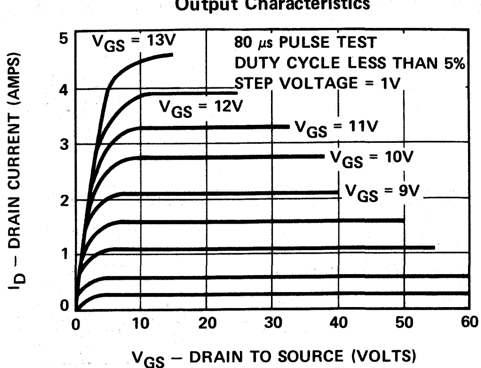
Symbol	Characteristics	Min	Typ	Max	Unit	Test Conditions
BV_{DSS}	Drain-Source Breakdown Voltage	80			V	V_{GS} = 0V, I_D = 10 mA
I_{DSS}	Drain-Source Leakage Current			2	mA	V_{GS} = 0V, V_{DS} = 30 V
I_{GSS}	Gate-Source Leakage Current			100	nA	V_{GS} = 40V, V_{DS} = 0V
g_m[1]	DC Forward Transconductance	0.4				V_{DS} = 10V, I_D = 2A, ΔV_{GS} = 1.0V
$I_{D(on)}$[1]	On-State Drain Current		3.0		A	V_{DS} = 30V, V_{GS} = 10V
$V_{GS(th)}$	Gate Threshold Voltage	2.0		6.0	V	V_{GS} = V_{DS}, I_D = 200 mA
C_{iss}	Common-Source Input Capacitance			100	pF	V_{GS} = 0V, V_{DS} = 30V, f = 1.0 MHz
C_{oss}	Common-Source Output Capacitance			80	pF	V_{GS} = 0V, V_{DS} = 30V, f = 1.0 MHz
C_{rss}	Reverse Transfer Capacitance			12	pF	V_{GS} = 0V, V_{DS} = 30V, f = 1.0 MHz
G_{ps}	Common-Source Power Gain	10			dB	V_{DD} = 28V, Po = 40W, f = 175 MHz, I_{DQ} = 0.2A
η	Drain Efficiency		65		%	V_{DD} = 28V, Po = 40W, f = 175 MHz, I_{DQ} = 0.2A
V_{SWR}	Load Mismatch Tolerance	30:1				V_{DD} = 28V, Po = 40W, f = 175 MHz, I_{DQ} = 0.2A

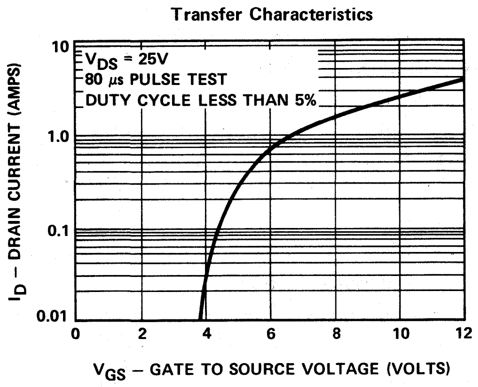
Note 1: Pulse Test—80μs to 300μs, 1% duty cycle

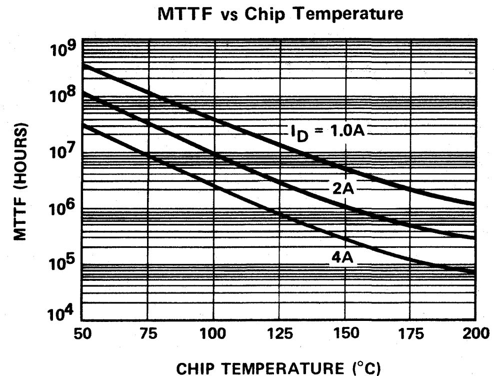
GEON

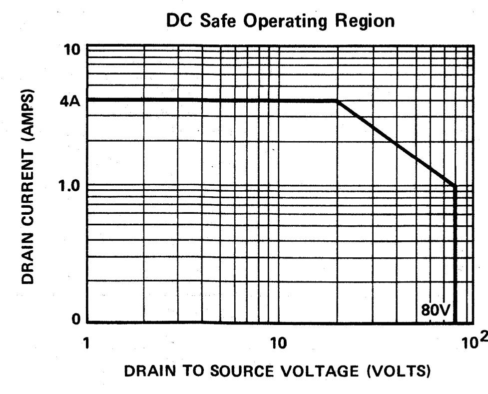
TYPICAL PERFORMANCE CURVES (25° C unless otherwise specified)



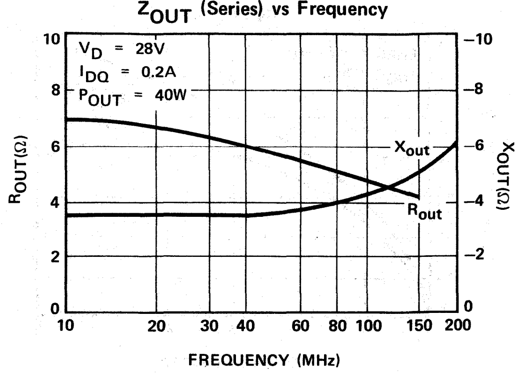


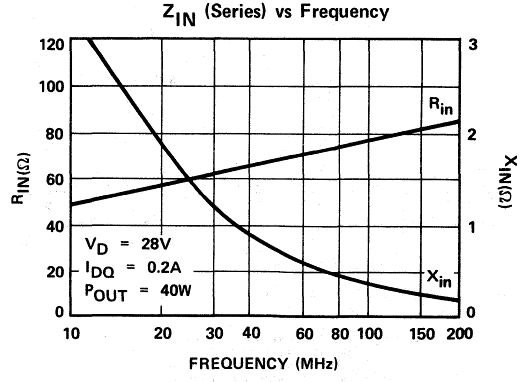






TYPICAL PERFORMANCE CURVES—CONTINUED (25° C unless otherwise specified)





SMALL SIGNAL 2-PORT PARAMETERS

2-PORT S-PARAMETERS DV2840S

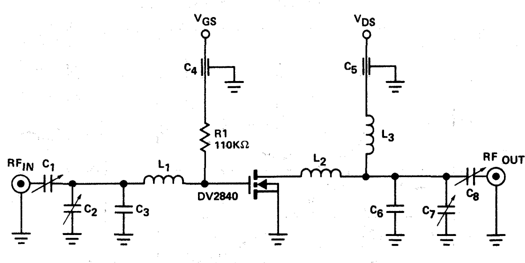
Freq	0 S_{11}	1	2 S_{21}	3	4 S_{12}	5	6 S_{22}	7
10	.78	−92°	28.71	124°	.04	37°	.65	−97°
20	.76	−127	17.44	108°	.05	19°	.66	−131
30	.78	−145	12.19	104	.05	13	.67	−146
40	.81	−151	9.07	91	.05	10	.73	−151
50	.78	−157	6.95	81	.05	10	.69	−155
60	.78	−160	5.71	75	.05	−1	.69	−157
70	.78	−164	4.96	71	.04	−2	.70	−160
80	.79	−165	4.11	67	.04	−4	.71	−161
90	.80	−167	3.39	65	.04	−3	.73	−163
100	.81	−169	3.16	63	.04	−3	.74	−164
120	.83	−170	2.45	57	.04	−3	.76	−166
140	.84	−173	2.01	54	.04	−2	.78	−168
160	.85	−174	1.67	50	.03	1	.80	−170
180	.87	−176	1.38	48	.03	6	.83	−172
200	.88	−177	1.17	46	.03	10	.84	−173
225	.89	−178	1.00	42	.03	14	.87	−175
250	.90	179	.84	38	.03	19	.87	−176
275	.88	180	.88	31	.03	20	.86	−176
300	.90	−177	.62	33	.03	28	.89	−178
325	.91	−176	.55	30	.03	33	.89	−178
350	.91	−175	.48	28	.03	37	.90	−178
375	.91	−175	.43	27	.03	42	.90	−179

2-PORT S-PARAMETERS DV2840W

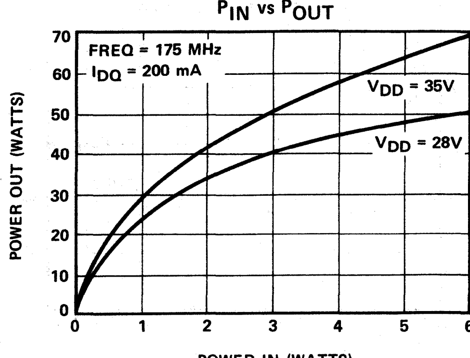
Freq	0 S_{11}	1	2 S_{21}	3	4 S_{12}	5	6 S_{22}	7
10	.82	−85°	28.32	129°	.04	40°	.68	−89
20	.78	−121	17.77	108	.05	21	.66	−123
30	.79	−139	12.40	95	.05	10	.68	−139
40	.79	−150	9.22	87	.05	4	.68	−146
50	.79	−153	7.10	82	.05	−1	.69	−150
60	.79	−157	5.75	78	.05	−3	.70	−154
70	.80	−160	4.81	73	.05	−4	.72	−157
80	.80	−162	4.13	70	.05	−8	.72	−157
90	.81	−164	3.62	67	.05	−9	.73	−159
100	.81	−165	3.14	64	.04	−10	.75	−160
120	.83	−167	2.47	60	.04	−11	.77	−167
140	.85	−169	1.91	56	.04	−12	.79	−163
160	.86	−171	1.67	54	.04	−13	.81	−166
180	.87	−172	1.39	51	.04	−14	.83	−167
200	.88	−173	1.19	49	.04	−13	.84	−168
225	.89	−174	1.00	46	.03	−13	.86	−168
250	.89	−176	.85	44	.03	−13	.87	−170
275	.90	−177	.73	42	.03	−11	.88	−171
300	.91	−177	.63	40	.03	−10	.90	−171
325	.91	−178	.55	37	.02	−8	.90	−171
350	.92	−179	.483	37	.02	−5	.90	−172
375	.92	179	.432	37	.02	−1	.91	−172
400	.93	177	.401	37	.02	3	.92	−173
425	.93	176	.358	38	.02	8	.92	−173
450	.93	176	.328	38	.02	13	.92	−174
475	.93	175	.307	38	.02	18	.93	−175
500	.93	174	.286	39	.02	25	.93	−176

TEST FIXTURE

175 MHz Schematic



NOTES: C_1, C_7, C_8, ARCO #422 TRIMMER CAPACITORS, 4–40 pF
C_2, ARCO #463 TRIMMER CAPACITOR, 9–180 pF
C_3, C_6, SEMCO 50 pF POWER CAPACITOR
C_4, C_5, 0.004 µF FEED-THRU CAPACITORS
L_1, 1 1/4" LENGTH OF #12 AWG COPPER WIRE
L_2, 1 1/2" LENGTH OF #12 AWG COPPER WIRE
L_3, 8-TURNS OF #22 AWG ENAMELED WIRE ON 1/4" DIAMETER, CLOSE WOUND



CAUTION: Beryllium Oxide — The top cap of this device is alumina which is harmless. However, the ceramic portion between the leads and the metal flange is Beryllium Oxide, the dust of which is toxic. Care must therefore be taken during handling and mounting the device to prevent any damage to this area.

Steps must be taken to ensure that all those who may handle, use, or dispose of this device are aware of its nature and of these necessary safety precautions. In particular the transistor should never be thrown out with general industrial or domestic waste.

DV2880T ■ DV2880U ■ DV2880W

Siliconix

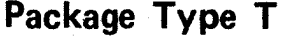
N-Channel Enhancement-Mode RF Power FETs

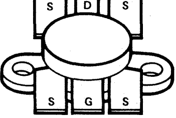
175 MHz
28-35 V
80 W
10 dB

Other Devices in Series:
DV2805, DV2810, DV2820, DV2840, DV28120

FEATURES

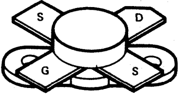
- Infinite VSWR
- No Thermal Runaway
- Broadband Capability
- Class A, B, C, D, E
- Low Noise Figure
- High Dynamic Range
- Simple Bias Circuitry
- S-Parameter Design


Package Type T



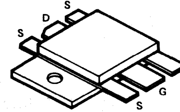
.500 J0 Flange

Package Type U



.500 SOE Flange

Package Type W



C-220

See page 5-62 for Package Dimensions

ABSOLUTE MAXIMUM RATINGS (T_C = 25° C unless otherwise noted)

Gate-Source Voltage 40V
Drain-Source Voltage 80V
Drain-Gate Voltage 80V
Drain Current (DC) . . . . 8 A

Total Device Dissipation . . . . 160 W
Thermal Resistance, Junction to Case . . 1.1°C/W
Junction Temperature . . . . 200°C
Storage Temperature . . . . –65°C to 150°C

ELECTRICAL CHARACTERISTICS (T_C = 25° C unless otherwise noted)

Symbol	Characteristics	Min	Typ	Max	Unit	Test Conditions
BV_{DSS}	Drain-Source Breakdown Voltage	80			V	V_{GS} = 0V, I_D = 20 mA
I_{DSS}	Drain-Source Leakage Current			4	mA	V_{GS} = 0V, V_{DS} = 30V
I_{GSS}	Gate-Source Leakage Current			100	nA	V_{GS} = 40V, V_{DS} = 0V
g_m[1]	D.C. Forward Transconductance	0.8	1.1		Mho	V_{DS} = 10V, I_D = 4A, ΔV_{GS} = 1.0V
$I_{D(on)}$[1]	On-State Drain Current		7		A	V_{DS} = 30V, V_{GS} = 10V
$V_{GS(th)}$	Gate Threshold Voltage	2		6	V	V_{GS} = V_{DS}, I_D = 400 mA
C_{iss}	Common-Source Input Capacitance			210	pF	V_{GS} = 0V, V_{DS} = 30V, f = 1.0 MHz
C_{oss}	Common-Source Output Capacitance			175	pF	V_{GS} = 0V, V_{DS} = 30V, f = 1.0 MHz
C_{rss}	Reverse Transfer Capacitance			25	pF	V_{GS} = 0V, V_{DS} = 30V, f = 1.0 MHz
G_{ps}	Common-Source Power Gain	10			dB	V_{DD} = 28V, Po = 80W, f = 175 MHz, I_{DQ} = 0.4A
η	Drain Efficiency		65		%	V_{DD} = 28V, Po = 80W, f = 175 MHz, I_{DQ} = 0.4A
V_{SWR}	Load Mismatch Tolerance	30:1				V_{DD} = 28V, Po = 80W, f = 175 MHz, I_{DQ} = 0.4A
N.F.	Noise Figure		4.0		dB	V_{DS} = 28V, I_D = 0.4A, f = 175 MHz

Note 1: Pulse Test—80 μs to 300 μs, 1% duty cycle

TYPICAL PERFORMANCE CURVES (25° C unless otherwise noted)

Transconductance vs Drain Current

Gm – TRANSCONDUCTANCE – MHOS

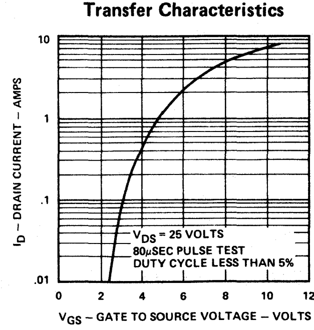
1.5
1.0
.5
1

V_{DS} = 25 VOLTS
80μSEC PULSE TEST
DUTY CYCLE LESS THAN 5%

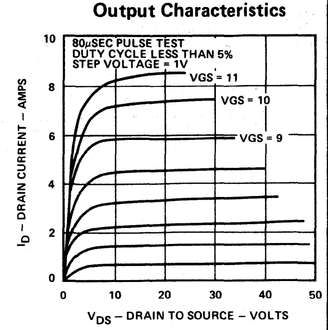
0 1 2 3 4 5 6 7 8

I_D – DRAIN CURRENT – AMPS

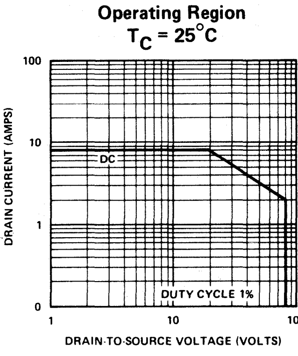
Transfer Characteristics



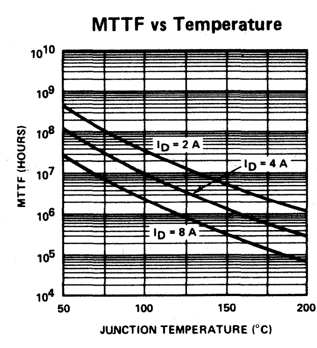
Output Characteristics



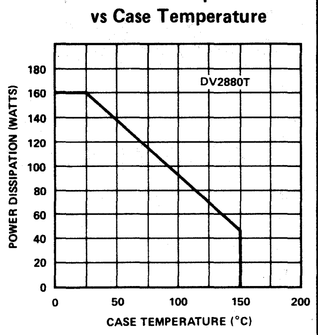
DC and Inductive Safe Operating Region T_C = 25°C



MTTF vs Temperature

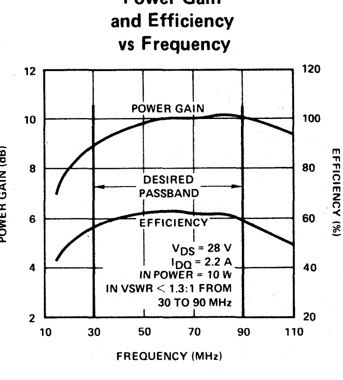


Power Dissipation vs Case Temperature

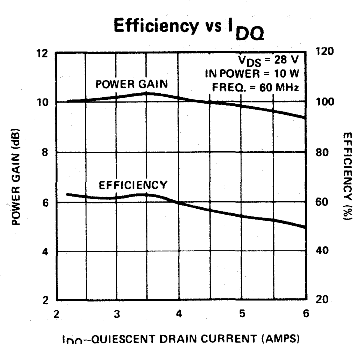


APPLICATIONS AND SYSTEMS DATA

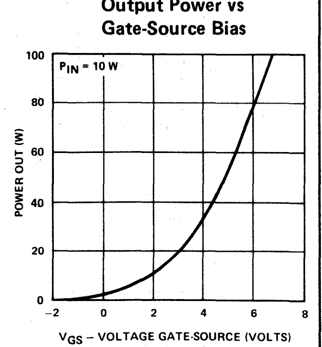
Power Gain and Efficiency vs Frequency



Efficiency vs I_{DQ}



Output Power vs Gate-Source Bias



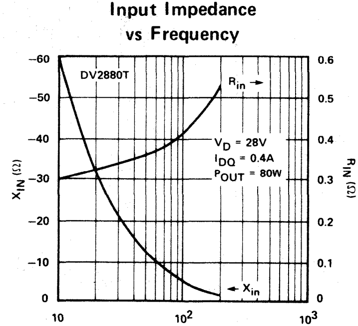
SMALL SIGNAL 2-PORT PARAMETERS

2-PORT Y-PARAMETER MATRIX IN MILLIMHOS

Freq	Y_{11}		Y_{21}		Y_{12}		Y_{22}	
(MHz)	(Real	Imag)	(Real	Imag)	(Real	Imag)	(Real	Imag)
10	0	10.5	886	−47.6	0	−1.03	4.42	8.34
20	0.897	21.3	881	−37.5	0	−2.05	5.31	15.9
50	6.52	58.3	902	−106	.5	−5.65	7.61	42.5
100	20.1	128	1060	−294	2.13	−11.9	11.0	89.3
150	57.0	207	1220	−565	6.63	−19.8	21.4	134
200	125	322	1450	−964	12.8	−33.4	23.1	191
250	241	340	1230	−1.61	32.5	−48.7	14.9	226
300	520	219	215.5	−2.4	33.6	−96.9	−76.3	371
350	565	124	−243.2	−2.02	43.5	−123	−66.1	417
400	574	4.06	−695.7	−1.72	37.1	−166	−59.3	551
450	509	−35.6	−812.7	−1.35	30.2	−198	−17.0	644
500	477	−11.6	−800.4	−1.27	43.7	−258	−13.8	749

Condition: 28 V, 1.6 A

Equivalent Large Signal Series Input Impedance vs Frequency

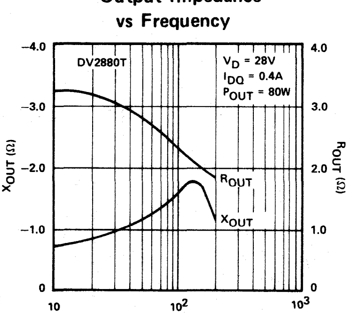


POLAR S-PARAMETERS IN 50.0 OHM SYSTEM

Freq	S_{11}		S_{21}		S_{12}		S_{22}	
(MHz)	(Magn	Angl)	(Magn	Angl)	(Magn	Angl)	(Magn	Angl)
10	.798	−134°	25.1	106°	.00	18.4°	.691	−141°
20	.819	−154°	13.1	91.8°	.03	6.42°	.819	−157°
50	.839	−168°	4.51	71.8°	.03	−6.34°	.766	−166°
100	.884	−173°	1.95	51.1°	.02	−13.2°	.835	−169°
150	.921	−175°	1.04	40.4°	.016	−6.22°	.888	−172°
200	.943	−177°	.629	34.2°	.013	−1.27°	.917	−174°
250	.953	−179°	.436	28.3°	.013	24.5°	.939	−175°
300	.959	178°	.309	26.4°	.013	40.4°	.950	−176°
350	.962	178°	.234	24.4°	.015	50.7°	.954	−176°
400	.966	177°	.187	24.3°	.017	58.8°	.957	−177°
450	.963	176°	.157	25.9°	.020	65.5°	.958	−178°
500	.966	176°	.138	27.2°	.029	69.0°	.962	−178°

Condition: 28 V, 1.6 A

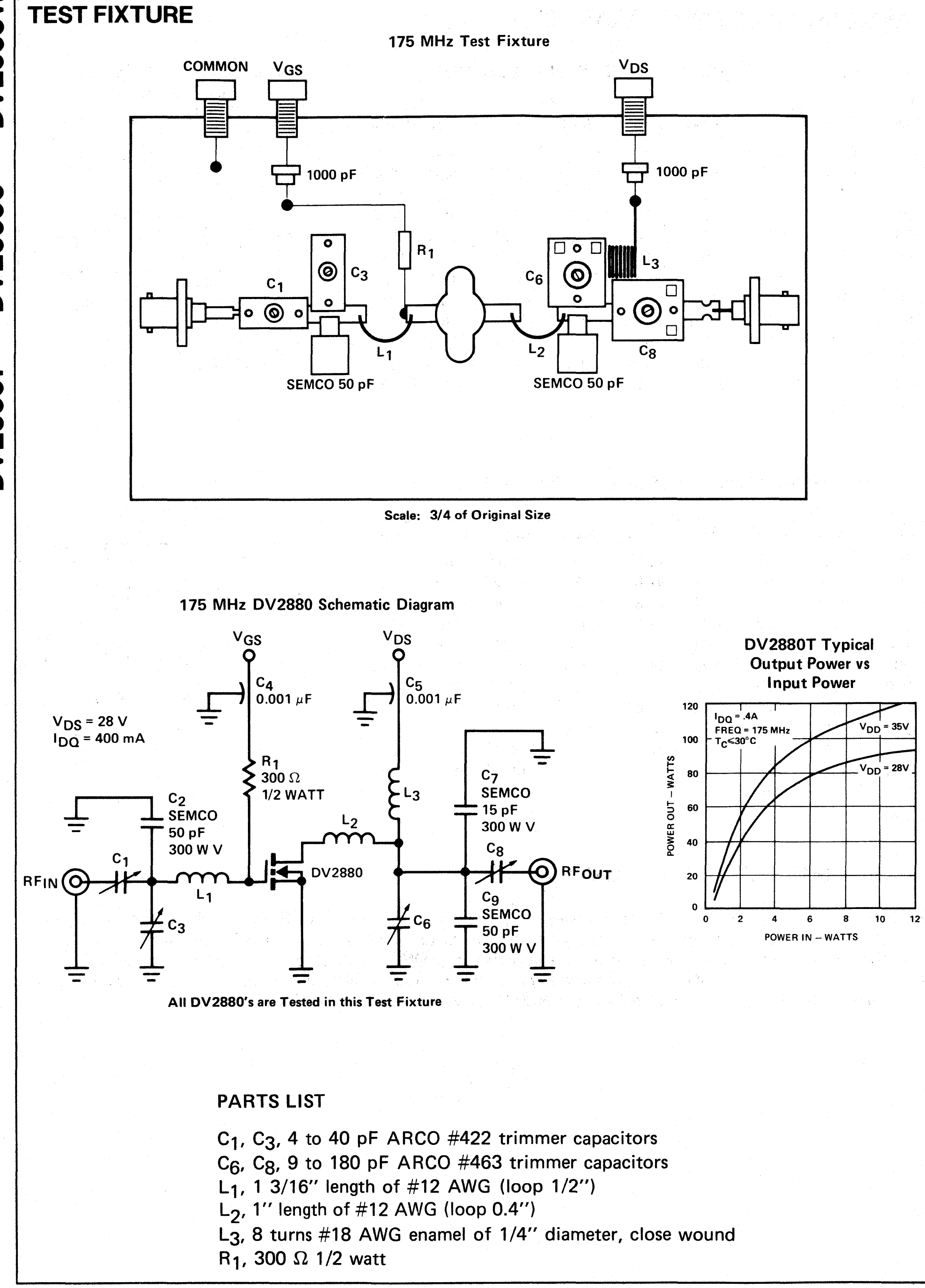
Equivalent Large Signal Series Output Impedance vs Frequency



BROADBAND AMPLIFIER ABSTRACT

Besides identifying five distinct advantages of power VMOS FETs which makes them the "designer's choice" for wideband amplifier design, Application Note AN80-4 derives useful equations that allow for the establishment of power gain and low input VSWR. Described is a 100 W power amplifier extending across the 30 MHz to 90 MHz band with an input VSWR less than 1.2:1, and a power gain of typically 10 dB. See Application Note AN80-6 for ALC, AGC applications.

TEST FIXTURE

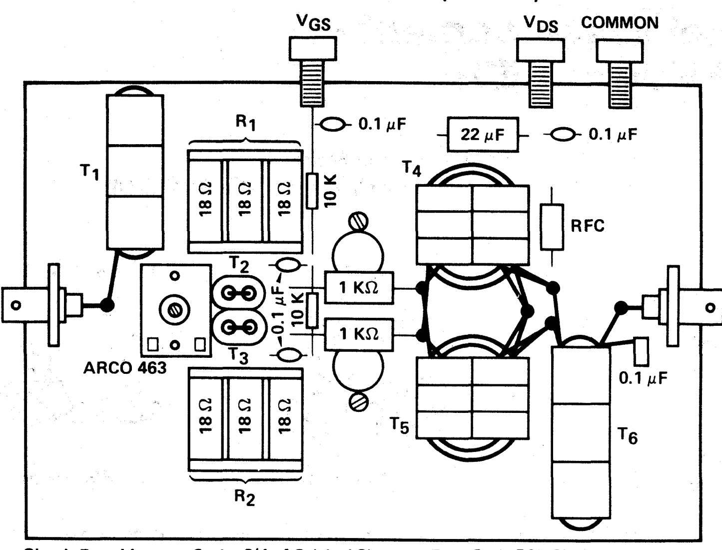


PARTS LIST

C_1, C_3, 4 to 40 pF ARCO #422 trimmer capacitors
C_6, C_8, 9 to 180 pF ARCO #463 trimmer capacitors
L_1, 1 3/16" length of #12 AWG (loop 1/2")
L_2, 1" length of #12 AWG (loop 0.4")
L_3, 8 turns #18 AWG enamel of 1/4" diameter, close wound
R_1, 300 Ω 1/2 watt

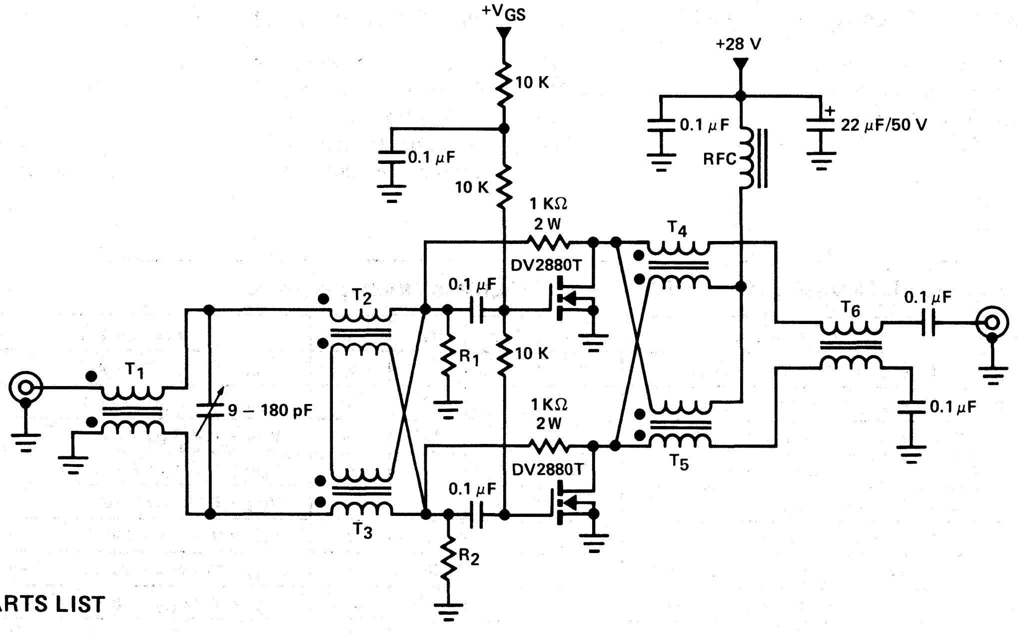
BROADBAND AMPLIFIER

30 to 80 MHz Broadband Component Layout



Circuit Board Layout, Scale: 3/4 of Original Size   Full–Scale PCB Shown on Last Page

100 Watt Broadband VMOS Power Amplifier



PARTS LIST

RFC ~ ferroxcube P/N VK200 09/3B

T_1, T_6 ~ two turns of RG-196A/U 50 Ω coax wound on three balun cores placed end on end. Cores are stackpole P/N 57-0973, μ_0 = 35

T_2, T_3 ~ two turns #22 twisted pair, four turns per inch, wound on two balun core. Core is stackpole P/N 57-0973. μ_0 = 35

T_4 = T_5 ~ three turns of 25 Ω coax wound on 6 torroid cores. Cores are configured similar to balun style core, three cores per side. Two 50 Ω coax RG-196A/U were paralleled to simulate 25 Ω coax. Cores are Indiana General P/N F627-8-Q2

R1, R2 ~ three 18 Ω 2 watt carbon composition resistors in parallel

DV28120T ■ DV28120U

N-Channel Enhancement - Mode RF Power FETs

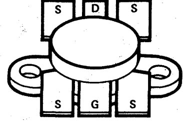
Siliconix

175 MHz
20-35 V
120 W
10 dB

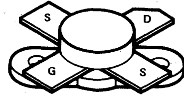
Other Devices in Series:
DV2805, DV2810, DV2820, DV2840, DV2880

FEATURES

- Infinite VSWR
- No Thermal Runaway
- Broadband Capability
- Class A, B, C, D, E
- Low Noise Figure
- High Dynamic Range
- Simple Bias Circuitry



.500 J0 Flange



.500 SOE Flange

See page 5-62 for Package Dimensions

ABSOLUTE MAXIMUM RATINGS (T_C = 25° C unless otherwise noted)

Gate-Source Voltage 40V
Drain-Source Voltage 80V
Drain-Gate Voltage 80V
Drain Current (DC) 12A

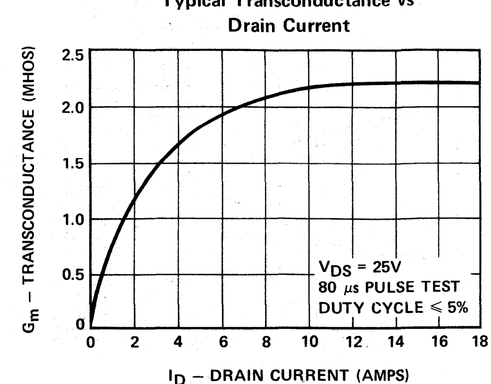
Total Device Dissipation 240W
Thermal Resistance,
Junction to Case . . . . 0.73°C/W
Junction Temperature . . . . 200°C
Storage Temperature . . . . . . –65°C to 150°C

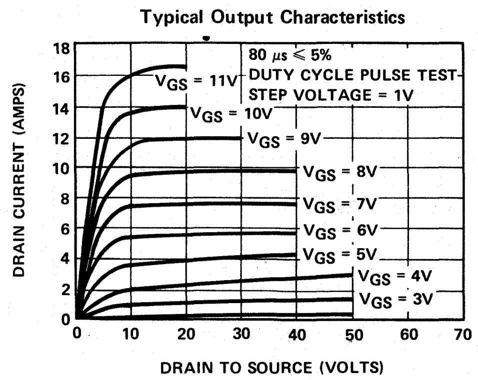
ELECTRICAL CHARACTERISTICS (T_C = 25° C unless otherwise noted)

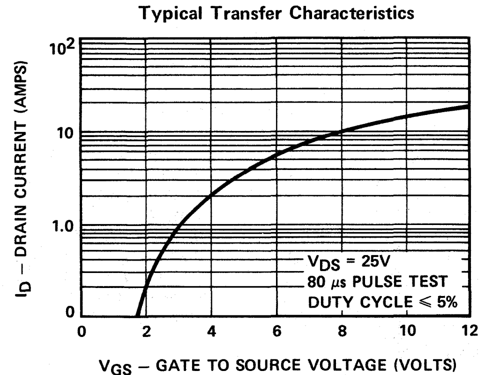
Symbol	Characteristics	Min	Typ	Max	Unit	Test Conditions
BV_{DSS}	Drain-Source Breakdown Voltage	80			V	V_{GS} = 0V, I_D = 30 mA
I_{DSS}	Drain-Source Leakage Current			6	mA	V_{GS} = 0V, V_{DS} = 30V
I_{GSS}	Gate-Source Leakage Current			100	nA	V_{GS} = 40V, V_{DS} = 0V
g_m	D.C. Forward Transconductance[1]	1.2	1.8		Mho	V_{DS} = 10V, I_D = 6A, ΔV_{GS} = 1.0V
$I_{D(on)}$	On-State Drain Current[1]		12		A	V_{DS} = 30V, V_{GS} = 10V
$V_{GS(th)}$	Gate Threshold Voltage	2		6	V	V_{GS} = V_{DS}, I_D = 600 mA
C_{iss}	Common-Source Input Capacitance			300	pF	V_{GS} = 0V, V_{DS} = 28V, f = 1.0 MHz
C_{oss}	Common-Source Output Capacitance			240	pF	V_{GS} = 0V, V_{DS} = 28V, f = 1.0 MHz
C_{rss}	Reverse Transfer Capacitance			35	pF	V_{GS} = 0V, V_{DS} = 28V, f = 1.0 MHz
G_{ps}	Common-Source Power Gain 28120T	10			dB	V_{DD} = 28V, Po = 120W, f = 175, MHz, I_{DQ} = 0.6A
	Common-Source Power Gain 28120U	9.0				
η	Drain Efficiency		65		%	V_{DD} = 28V, Po = 120W, f = 175 MHz, I_{DQ} = 0.6A
V_{SWR}	Load Mismatch Tolerance	30:1				V_{DD} = 28V, Po = 120W, f = 175 MHz, I_{DQ} = 0.6A

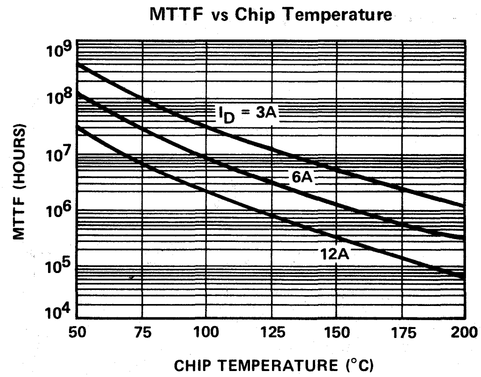
Note 1: Pulse Test—80μs to 300μs, 1% duty cycle

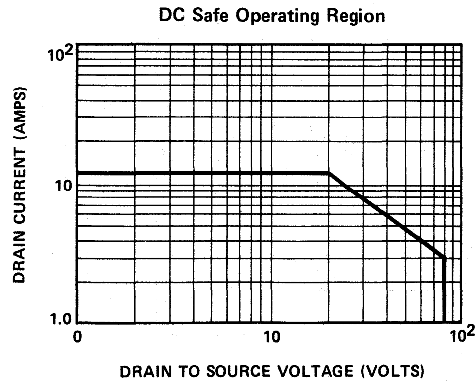
TYPICAL PERFORMANCE CURVES (25° C unless otherwise noted)



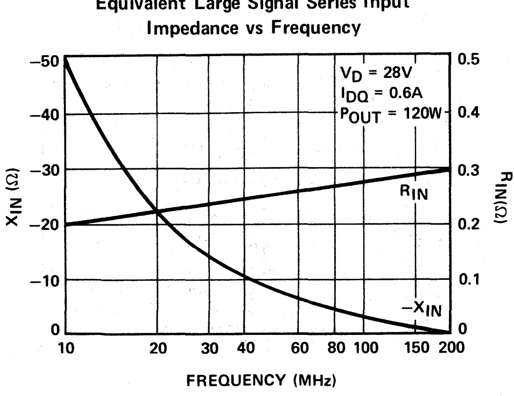


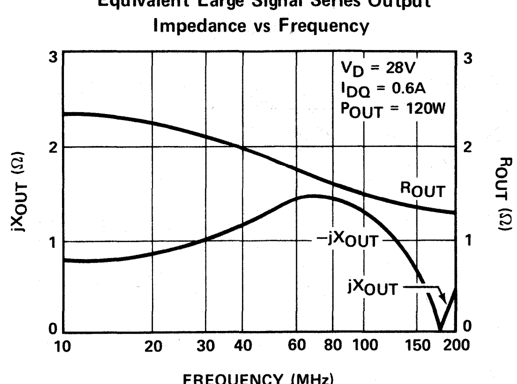




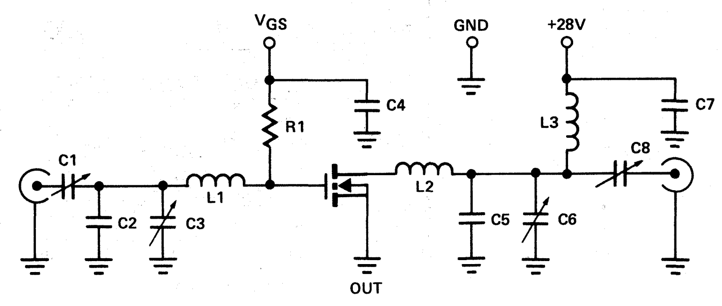


TYPICAL PERFORMANCE CURVES—CONTINUED (25° C unless otherwise noted)



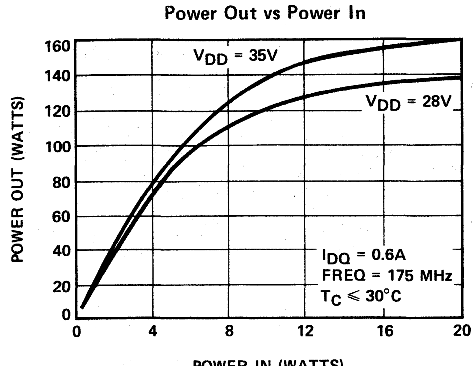


175 MHz RF TEST FIXTURE

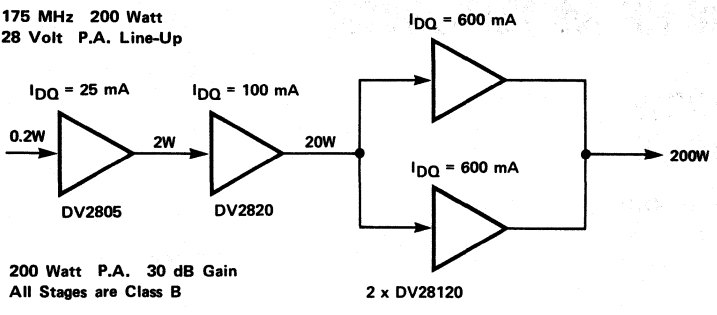


PARTS LIST

C1, C6	5–80 pF (ARCO 462)
C2, C5	50 pF SEMCO
C3	4–40 pF (ARCO 422)
C4, C7	0.01 μF
C8	9–180 pF (ARCO 463)
L1	7/8" #12 AWG 0.4" Loop
L2	7/8" #12 AWG 0.4" Loop
L3	8 Turns #16 AWG 1/4" I_D
R1	10K 1/4W



TYPICAL AMPLIFIER LINE-UP



CAUTION: **Beryllium Oxide** – The top cap of this device is alumina which is harmless. However, the ceramic portion between the leads and the metal flange is Beryllium Oxide, the dust of which is toxic. Care must therefore be taken during handling and mounting the device to prevent any damage to this area.

Steps must be taken to ensure that all those who may handle, use, or dispose of this device are aware of its nature and of these necessary safety precautions. In particular the transistor should never be thrown out with general industrial or domestic waste.

DV28120V

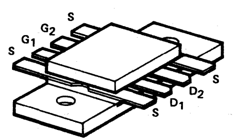
Siliconix

N-Channel Enhancement-Mode
Push-Pull RF MOSPOWER

175 MHz 120W
28-35V 10 dB

Other Devices in Series:
DV2880V

V Package



.400 Push-Pull Flange

See page 5-62 for Package Dimensions

FEATURES
- Infinite VSWR
- No Thermal Runaway
- Broadband Capability
- Class A, B, C
- Low Noise Figure
- High Dynamic Range
- Simple Bias Circuitry

ABSOLUTE MAXIMUM RATINGS (T_C=25°C unless otherwise noted)

Gate-Source Voltage 40V
Drain-Source Voltage 70V
Drain-Gate Voltage 70V
Drain Current (DC) 12A
Total Device Dissipation 240W
Thermal Resistance, Junction to Case . . 0.73°C/W
Junction Temperature . . . . .200°C
Storage Temperature . . . . –55°C to +150°C

ELECTRICAL CHARACTERISTICS (T_C=25°C unless other noted)

Symbol	Characteristics	Min	Typ	Max	Unit	Test Conditions
BV_{DSS}	Drain-Source Breakdown Voltage	70			V	V_{GS} = 0V, I_D = 30 mA
I_{DSS}	Drain-Source Leakage Current			6	mA	V_{GS} = 0V, V_{DS} = 30V
I_{GSS}	Gate-Source Leakage Current			100	nA	V_{GS} = 40V, V_{DS} = 0V
g_m	D.C. Forward Transconductance[1]	1.2	1.8		Mho	V_{DS} = 10V, I_D = 6A, ΔV_{GS} = 1.0V
$I_{D(on)}$	On-State Drain Current[1]		12		A	V_{DS} = 30V, V_{GS} = 10V
$V_{GS(th)}$	Gate Threshold Voltage	2		6	V	V_{GS} = V_{DS}, I_D = 600 mA
C_{iss}	Common-Source Input Capacitance[2]			300	pF	V_{GS} = 0V, V_{DS} = 28V, f = 1.0 MHz
C_{oss}	Common-Source Output Capacitance[2]			240	pF	V_{GS} = 0V, V_{DS} = 28V, f = 1.0 MHz
C_{rss}	Reverse Transfer Capacitance[2]			35	pF	V_{GS} = 0V, V_{DS} = 28V, f = 1.0 MHz
G_{ps}	Common-Source Power Gain	10			dB	V_{DD} = 28V, P_o = 120W f = 175 MHz, I_{DQ} = 0.6A
η	Drain Efficiency		65		%	V_{DD} = 28V, P_o = 120W f = 175 MHz, I_{DQ} = 0.6A
V_{SWR}	Load Mismatch Tolerance	30:1				V_{DD} = 28V, P_o = 120W f = 175 MHz, I_{DQ} = 0.6A

Note 1: Pulse Test—80μs to 300μs, 1% duty cycle
Note 2: All DC and Capacitance parameters measured with both sides in parallel.

TYPICAL PERFORMANCE CURVES (25°C unless otherwise noted)

FIGURE 1 Transconductance vs. Drain Current

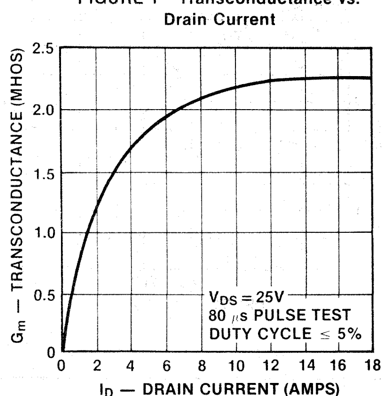


FIGURE 2 Transfer Characteristics

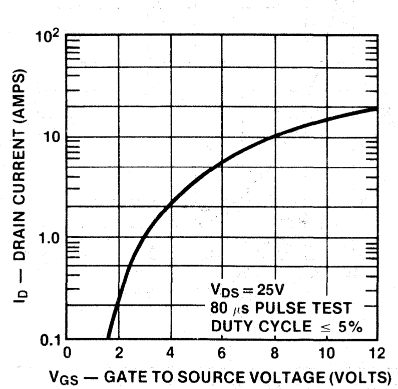


FIGURE 3 Output Characteristics

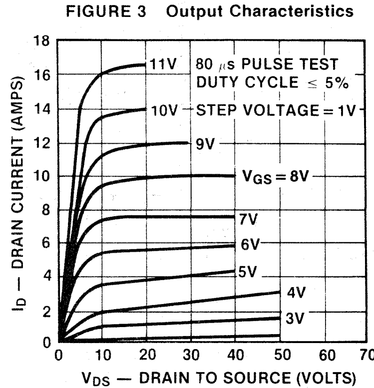


FIGURE 4 DC Safe Operating Region

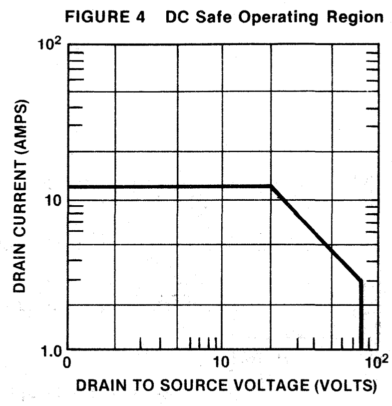
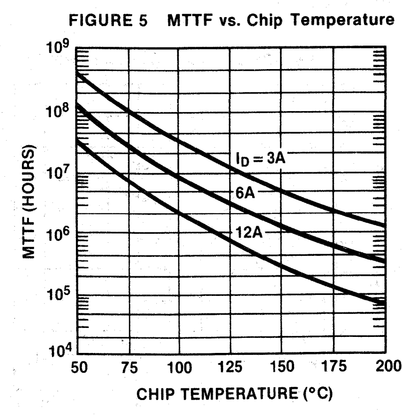


FIGURE 5 MTTF vs. Chip Temperature



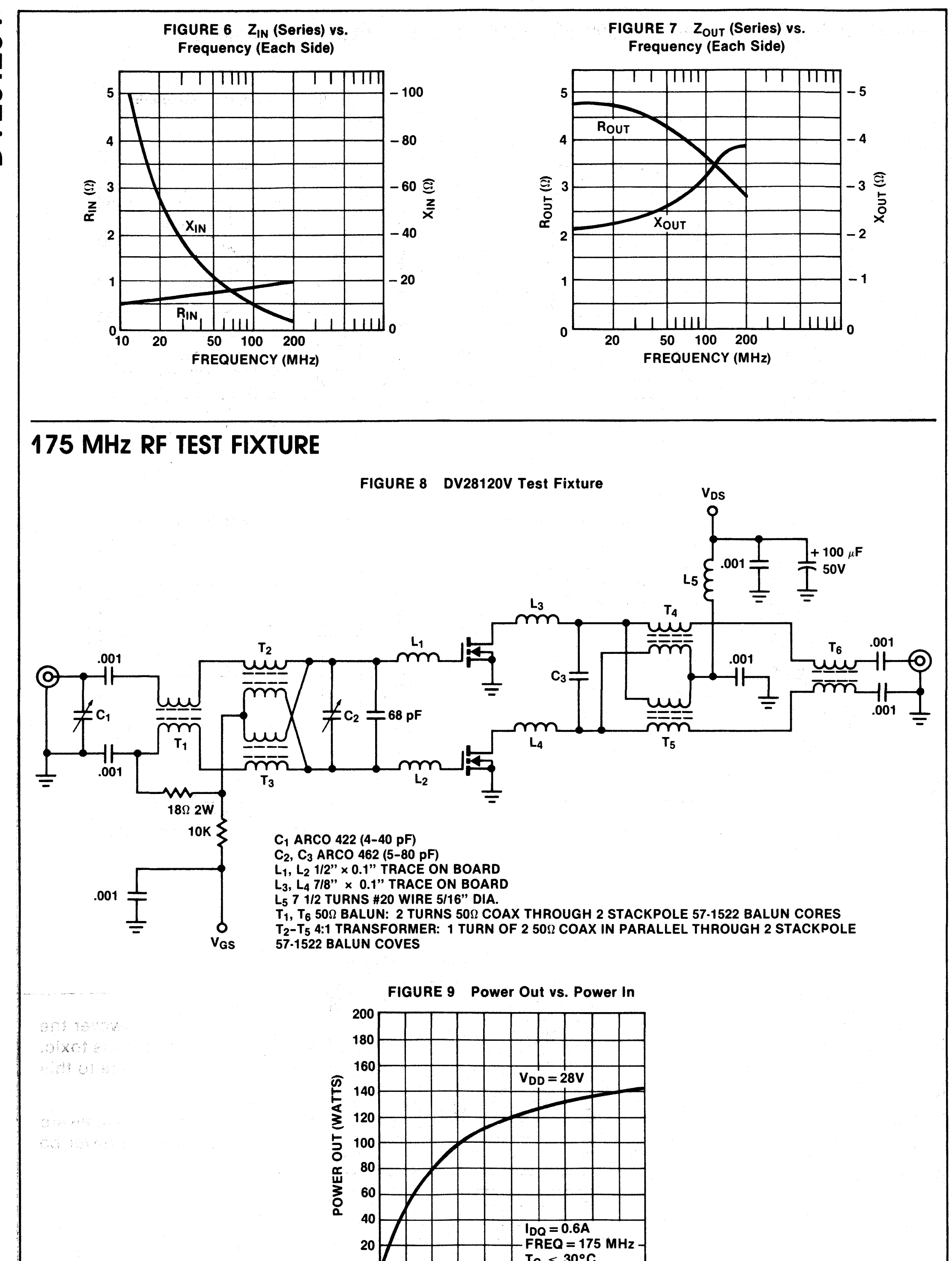


FIGURE 6 ZIN (Series) vs. Frequency (Each Side)
RIN (Ω)
XIN (Ω)
XIN
RIN
5
4
3
2
1
0
100
80
60
40
20
0
10 20 50 100 200
FREQUENCY (MHz)
FIGURE 7 ZOUT (Series) vs. Frequency (Each Side)
ROUT (Ω)
XOUT (Ω)
ROUT
XOUT
5
4
3
2
1
0
20 50 100 200
FREQUENCY (MHz)
175 MHz RF TEST FIXTURE
FIGURE 8 DV28120V Test Fixture
VDS
.001
+ 100 μF
50V
L5
L3
T4
L1
T2
.001
T6
.001
.001
C1
T1
C3
C2
68 pF
.001
.001
L4
T5
T3
L2
18Ω 2W
10K
.001
VGS
C1 ARCO 422 (4-40 pF)
C2, C3 ARCO 462 (5-80 pF)
L1, L2 1/2" × 0.1" TRACE ON BOARD
L3, L4 7/8" × 0.1" TRACE ON BOARD
L5 7 1/2 TURNS #20 WIRE 5/16" DIA.
T1, T6 50Ω BALUN: 2 TURNS 50Ω COAX THROUGH 2 STACKPOLE 57-1522 BALUN CORES
T2-T5 4:1 TRANSFORMER: 1 TURN OF 2 50Ω COAX IN PARALLEL THROUGH 2 STACKPOLE 57-1522 BALUN COVES
FIGURE 9 Power Out vs. Power In
POWER OUT (WATTS)
200
180
160
140
120
100
80
60
40
20
0
VDD = 28V
IDQ = 0.6A
FREQ = 175 MHz
TC ≤ 30°C
0 1 2 3 4 5 6 7 8 9 10
POWER IN (WATTS)

APPLICATIONS

FIGURE 10 Typical Amplifier Line Up

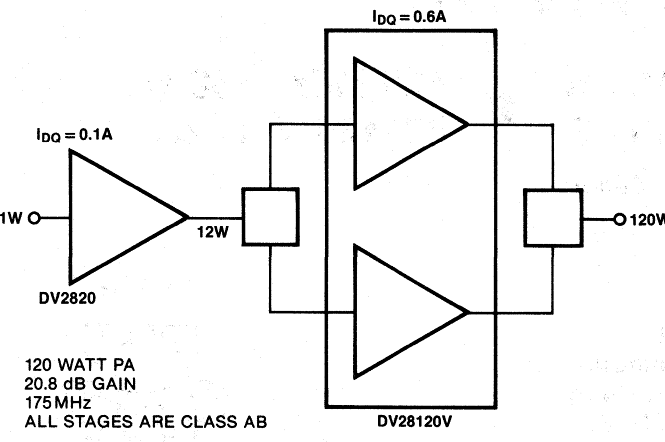
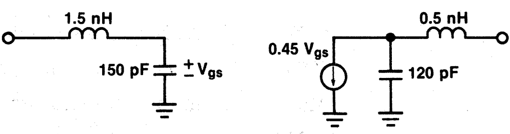


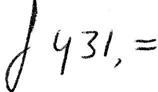
FIGURE 11 Simplified AC Equivalent Circuit Model, Each Half



CAUTION: Beryllium Oxide — the top cap of this device is alumina which is harmless. However the ceramic portion between the leads and the metal flange is Beryllium Oxide, the dust of which is toxic. Care must therefore be taken during handling and mounting the device to prevent any damage to this area.

Steps must be taken to ensure that all those who may handle, use, or dispose of this device are aware of its nature and of these necessary safety precautions. in particular the transistor should never be thrown out with general industrial or domestic waste.

DVD150T



Siliconix

100V RF Power FET

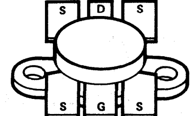
175 MHz 120 W ■ 100 MHz 150 W
80-120 V 10 dB ■ 80-120 V 17 dB

Other Devices in Series:
DVD030S

FEATURES

- Infinite VSWR
- No Thermal Runaway
- Broadband Capability
- Class A, B, C, D, E
- Low Noise Figure
- High Dynamic Range
- Simple Bias Circuitry
- Lower I^2R Losses

Package Type T



.500 JO Flange

See page 5-62 for Package Dimensions

ABSOLUTE MAXIMUM RATINGS (T_C=25°C unless otherwise noted)

Gate-Source Voltage 40V
Drain-Source Voltage 220V
Drain-Gate Voltage 220V
Drain Current (DC) 4.8A
Total Device Dissipation 240W
Thermal Resistance, Junction to Case ..0.73°C/W
Junction Temperature ....200°C
Storage Temperature ....−65°C to +150°C

ELECTRICAL CHARACTERISTICS (T_C=25°C unless other noted)

Symbol	Characteristics	Min	Typ	Max	Unit	Test Conditions
BV_{DSS}	Drain-Source Breakdown Voltage	220			V	V_{GS}=0V, I_D=30 mA
I_{DSS}	Drain-Source Leakage Current			6.0	mA	V_{GS}=0V, V_{DS}=100V
I_{GSS}	Gate-Source Leakage Current			100	nA	V_{GS}=40V, V_{DS}=0V
g_m[1]	D.C. Forward Transconductance	1.0			Mho	V_{DS}=50V, I_D=5A, ΔV_{GS}=1.0V
$I_{D(on)}$[1]	On-State Drain Current	1.5			A	V_{DS}=50V, V_{GS}=5V
$V_{GS(th)}$	Gate Threshold Voltage	2.0		6.0	V	V_{GS}=V_{DS}, I_D=1.0 Amp
C_{iss}	Common-Source Input Capacitance			400	pF	V_{GS}=0V, V_{DS}=30V, f=1.0 MHz
C_{oss}	Common-Source Output Capacitance			100	pF	V_{GS}=0V, V_{DS}=30V, f=1.0 MHz
C_{rss}	Reverse Transfer Capacitance			15	pF	V_{GS}=0V, V_{DS}=30V, f=1.0 MHz
G_{ps}	Common-Source Power Gain	10			dB	V_{DD}=100V, V_{GS}=0V, P_o=120W, f=175 MHz
			17			V_{DD}=100V, V_{GS}=0V, P_o=150W, f=100 MHz
η	Drain Efficiency		65		%	V_{DD}=100V, P_o=120W f=175 MHz, V_{GS}=0V
V_{SWR}	Load Mismatch Tolerance	30:1				V_{DD}=100V, P_o=120W f=175 MHz, $I_{D(max)}$=2.4A

Note 1: Pulse Test—80μs to 300μs, 1% duty cycle

TYPICAL PERFORMANCE CURVES

FIGURE 1 Transfer Characteristics

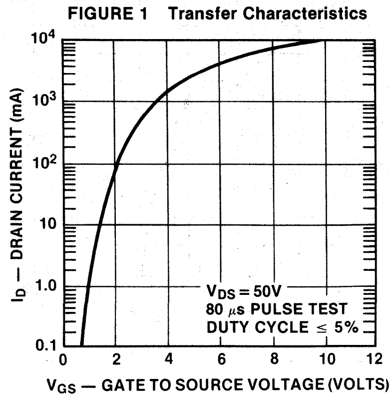


FIGURE 2 Output Characteristics

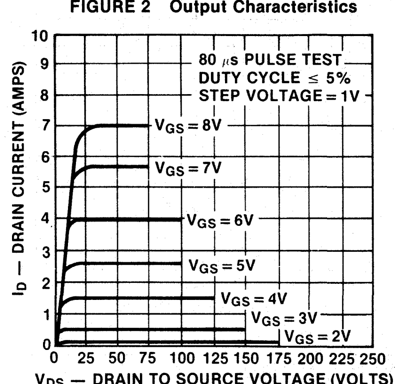


FIGURE 3 Transconductance vs. Drain Current

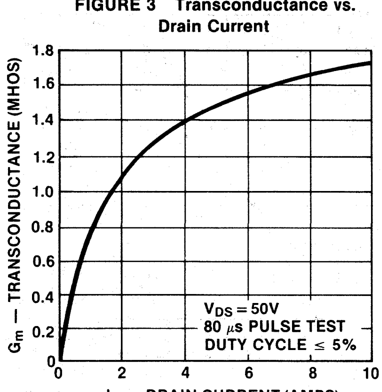


FIGURE 4 MTTF vs. Chip Temperature

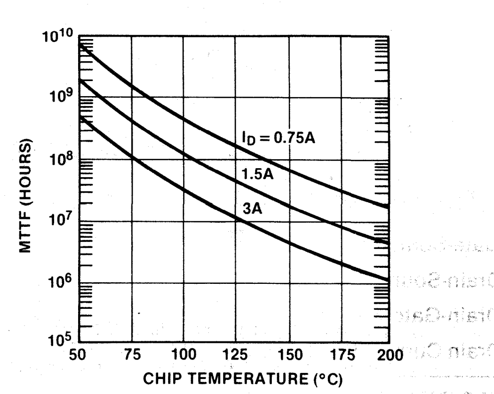
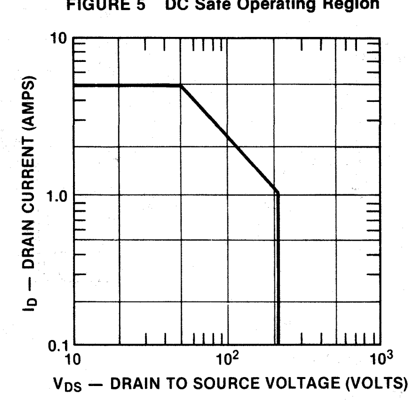


FIGURE 5 DC Safe Operating Region



5

FIGURE 6 Series Equivalent Input Impedance vs. Frequency

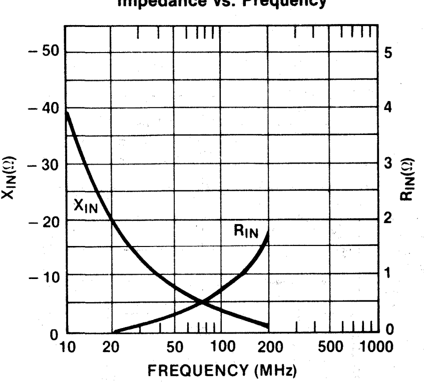
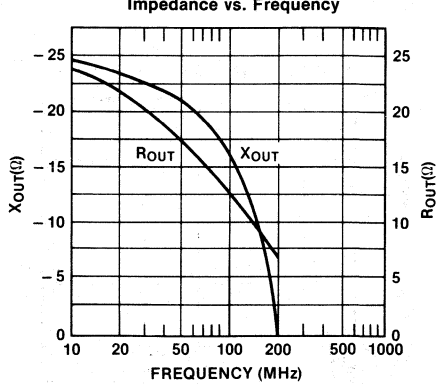
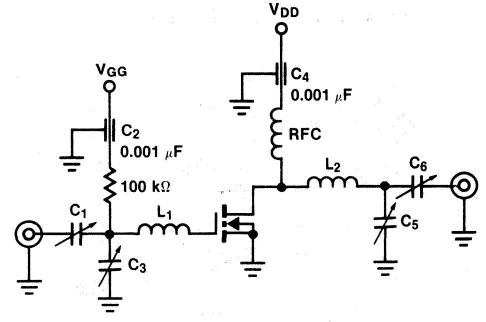


FIGURE 7 Series Equivalent Output Impedance vs. Frequency



RF TEST FIXTURES

FIGURE 8 175 MHz Test Fixture



PARTS LIST
C_1, C_3, C_5, C_6, ARCO #462, 5 TO 80 pF TRIMMER CAPACITORS
L_1, L_2, 1 1/2 TURNS #12 AWG AIR WOUND, 5/16" IN DIA.
RFC, 10-TURNS #20 AWG ENAMEL ON 1/4" DIA., CLOSE WOUND

FIGURE 9 Typical Power Out vs. Power In

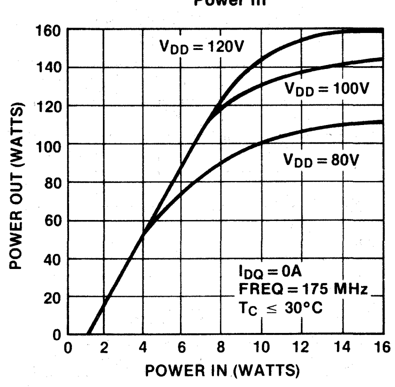
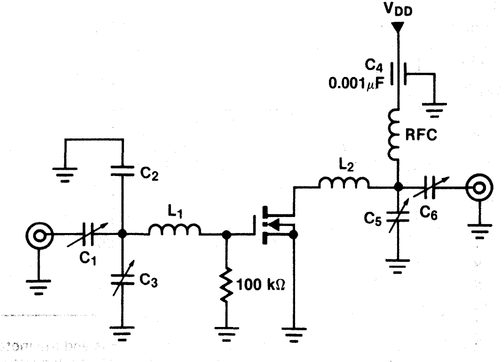
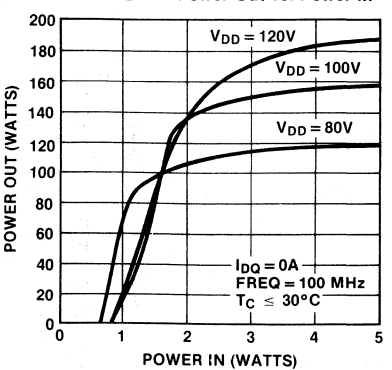


FIGURE 10 100 Volt VNR 100 MHz Test Fixture



C_1, C_5, C_6 ARCO #462 5 TO 80 pF TRIMMER CAPACITOR
C_2, 30 pF SEMCO POWER CAPACITOR
C_3, ARCO #422 4 TO 40 pF TRIMMER CAPACITOR
RFC, 13-TURNS #18 AWG CLOSE WOUND ON 0.3" DIA.
L_1, 3-TURNS #12 AWG ON 0.3" DIA.
L_2, 5-TURNS #12 AWG ON 0.3" DIA.

FIGURE 11 Power Out vs. Power In



APPLICATIONS

FIGURE 12 2-30 MHz Linear Amplifier

NOTES:
1. $V_{DD} = 100V$
2. $I_{DQ} = 0.25A$/TRANSISTOR

PARTS LIST

T_1 4:1 TRANSFORMER
4 TURNS OF TWO 50Ω COAX IN PARALLEL THROUGH SIX INDIANA GENERAL FERRITE CORES PN F627-8-Q1

T_2 12.5Ω BALUN
2 TURNS OF FOUR 50Ω COAX IN PARALLEL THROUGH SIX INDIANA GENERAL FERRITE CORES PN F627-8-Q1

T_3 4:1 TRANSFORMER
4 TURNS OF TWO 50Ω COAX IN PARALLEL THROUGH SIX INDIANA GENERAL FERRITE CORES PN F627-8-Q1

T_4 50Ω BALUN
6 TURNS OF 50Ω COAX THROUGH SIX INDIANA GENERAL FERRITE CORES PN F627-8-Q1

FIGURE 13 Gain and Input VSWR vs. Frequency

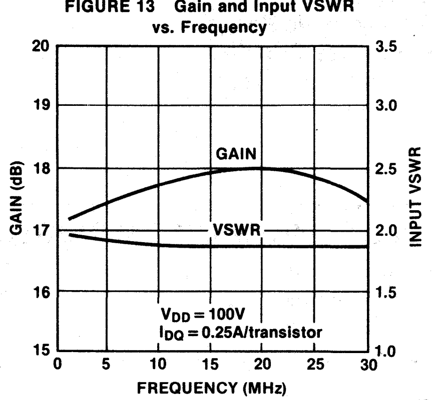


FIGURE 14 Intermodulation Ratio vs. Output Power (30 MHz)

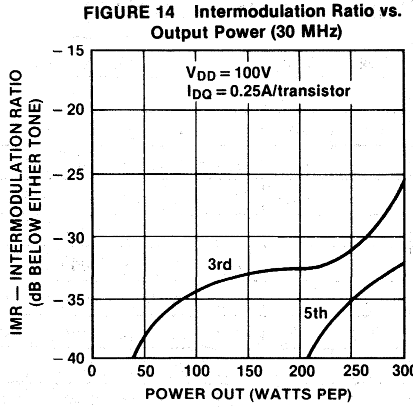
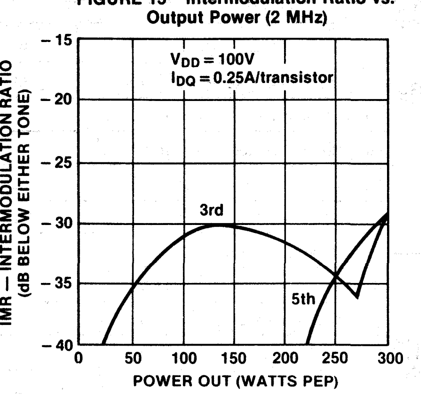


FIGURE 15 Intermodulation Ratio vs. Output Power (2 MHz)



CAUTION: Beryllium Oxide — The top cap of this device is alumina which is harmless. However, the ceramic portion between the leads and the metal flange is Beryllium Oxide, the dust of which is toxic. Care must therefore be taken during handling and mounting the device to prevent any damage to this area.

Steps must be taken to ensure that all those who may handle, use, or dispose of this device are aware of its nature and of these necessary safety precautions. In particular the transistor should never be thrown out with general industrial or domestic waste.

VMP4

Siliconix

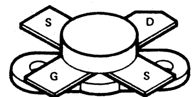
N-Channel Enhancement-Mode RF Power FETs

175 MHz
20-35 V
20 W
10 dB

FEATURES

- Infinite VSWR
- No Thermal Runaway
- Broadband Capability
- Class A, B, C, D, E
- Low Noise Figure
- High Dynamic Range
- Simple Bias Circuitry
- S-Parameter Design

Package Type S



.380 SOE Flange

See page 5-62 for Package Dimensions

ABSOLUTE MAXIMUM RATINGS (T_C = 25° C unless otherwise noted)

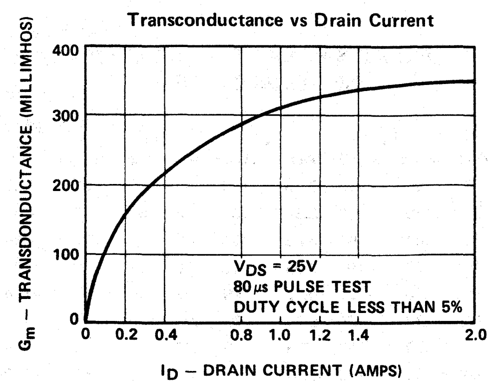
Gate-Source Voltage 40V
Drain-Source Voltage 60V
Drain-Gate Voltage 60V
Drain Current (DC) 2A
Total Device Dissipation 40W
Thermal Resistance, Junction to Case . . 4.4°C/W
Junction Temperature . . . . 200°C
Storage Temperature . . . . −65°C to 150°C

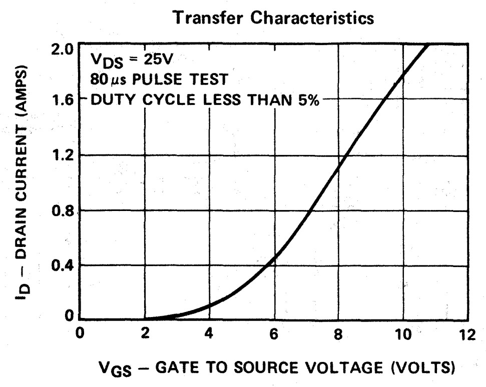
ELECTRICAL CHARACTERISTICS (T_C = 25° C unless otherwise noted)

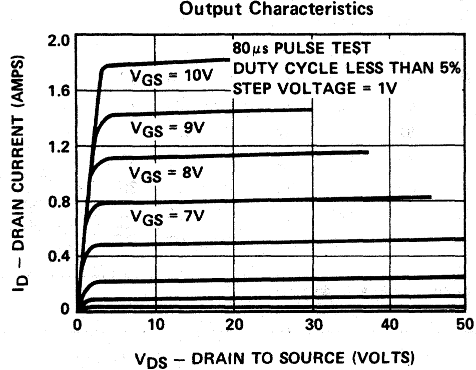
Symbol	Characteristics	Min	Typ	Max	Unit	Test Conditions
BV_{DSS}	Drain-Source Breakdown Voltage	60			V	V_{GS} = 0V, I_D = 1.0 mA
I_{DSS}	Drain-Source Leakage Current			100	μA	V_{GS} = 0V, V_{DS} = 25V
I_{GSS}	Gate-Source Leakage Current			100	nA	V_{GS} = 40V, V_{DS} = 0V
g_m[1]	D.C. Forward Transconductance	0.2	0.3		mho	V_{DS} = 10V, I_D = 1A, ΔV_{GS} = 1.0V
$I_{D(on)}$[1]	On-State Drain Current	1.2	1.8		A	V_{DS} = 30V, V_{GS} = 10V
$V_{GS(th)}$	Gate Threshold Voltage	2		6	V	V_{GS} = V_{DS}, I_D = 100 mA
C_{iss}	Common-Source Input Capacitance		35	50	pF	V_{GS} = 0V, V_{DS} = 30V, f = 1.0 MHz
C_{oss}	Common-Source Output Capacitance		30	40	pF	V_{GS} = 0V, V_{DS} = 30V, f = 1.0 MHz
C_{rss}	Reverse Transfer Capacitance		5.0	7.5	pF	V_{GS} = 0V, V_{DS} = 30V, f = 1.0 MHz
G_{ps}	Common-Source Power Gain	10			dB	V_{DD} = 28V, Po = 20W, f = 175 MHz, I_{DQ} = 0.1A
η	Drain Efficiency		65		%	V_{DD} = 28V, Po = 20W, f = 175 MHz, I_{DQ} = 0.1A
V_{SWR}	Load Mismatch Tolerance	30:1				V_{DD} = 28V, Po = 20W, f = 175 MHz, I_{DQ} = 0.1A
N.F.	Noise Figure		5.6		dB	V_{DS} = 28V, I_D = 0.1A, f = 175 MHz

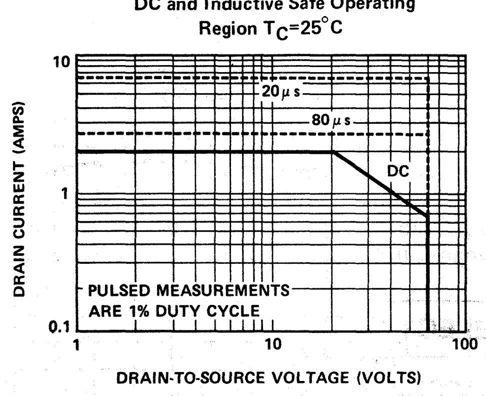
Note 1: Pulse Test — 80μs to 300μs, 1% duty cycle

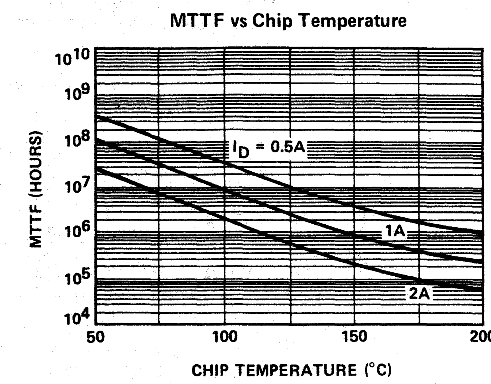
TYPICAL PERFORMANCE CURVES (25° C unless otherwise noted)

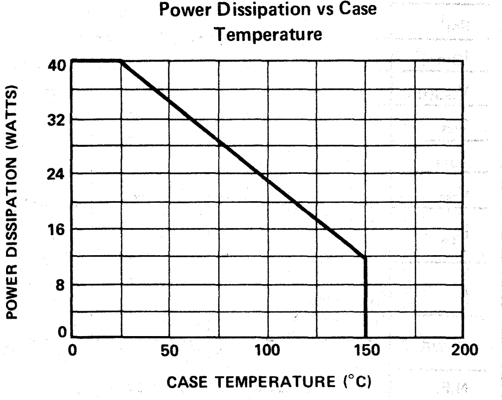






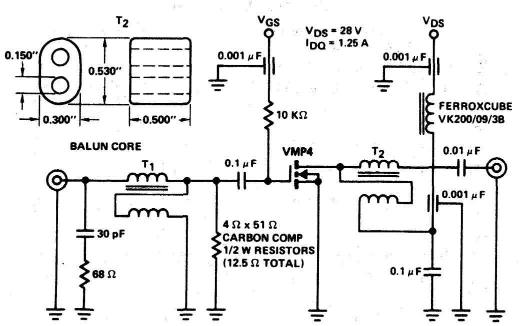






APPLICATIONS

28V WIDEBAND AMPLIFIER

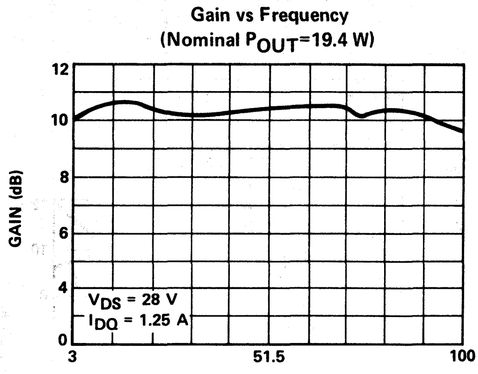


Parts List

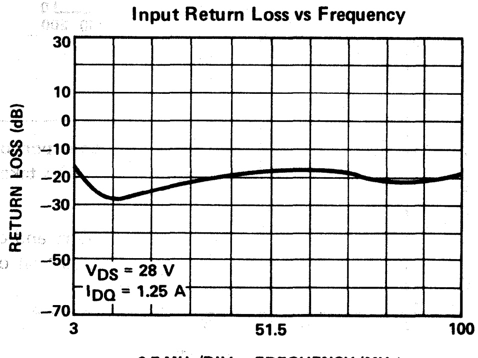
T_1, 20 turns 30 Ω, #30 bifilar on micrometals T-50-6 Toroid

T_2, 1 turn of 2-50 Ω coax cables in parallel through 2 balun cores stackpole #57-9130 μo = 125

Gain vs Frequency (Nominal P_{OUT}=19.4 W)



Input Return Loss vs Frequency



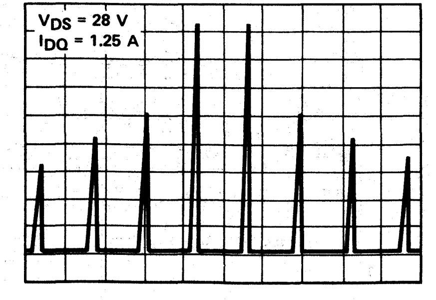
SMALL SIGNAL 2-PORT PARAMETERS

POLAR S-PARAMETERS VMP4 IN 50.0 OHM SYSTEM

Freq	S_{11}		S_{21}		S_{12}		S_{22}	
(MHz)	(Magn	Angl)	(Magn	Angl)	(Magn	Angl)	(Magn	Angl)
10	.93	−36	22.13	150	.03	63	.83	−35
20	.89	−67	18.84	134	.05	50	.78	−65
30	.84	−91	15.85	124	.06	41	.72	−85
40	.79	−107	12.59	113	.06	32	.69	−102
50	.76	−120	10.00	99	.07	19	.65	−114
60	.73	−129	8.41	91	.07	15	.62	−121
70	.72	−137	7.5	85	.07	12	.62	−128
80	.72	−142	6.31	80	.07	9	.62	−133
90	.72	−147	5.31	76	.06	8	.62	−139
100	.72	−151	5.01	73	.06	7	.62	−142
120	.73	−156	3.98	66	.06	6	.64	−148
140	.75	−162	3.35	61	.06	6	.66	−153
160	.76	−166	2.82	56	.06	7	.68	−157
180	.78	−169	2.37	53	.05	11	.71	−162
200	.79	−173	2.04	50	.05	14	.73	−165
225	.80	−175	1.78	45	.05	17	.78	−168
250	.81	180	1.51	40	.05	21	.78	−171
275	.82	175	1.29	37	.05	26	.79	−174
300	.82	173	1.12	35	.05	30	.80	−175
325	.83	171	.99	33	.05	36	.80	−176
350	.84	170	.87	31	.05	40	.81	−176
375	.84	169	.79	30	.06	45	.82	−177

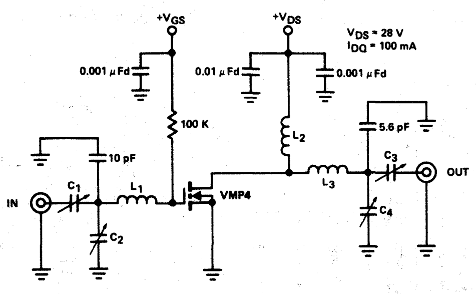
Conditions: 28V @ 450 mA

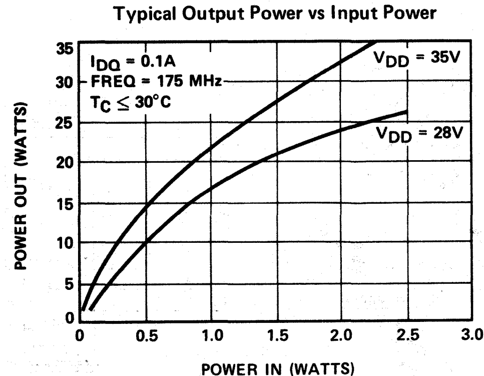
Intermodulation Distortion vs Frequency (Nominal Power Output 12 W PEP)



TEST FIXTURE

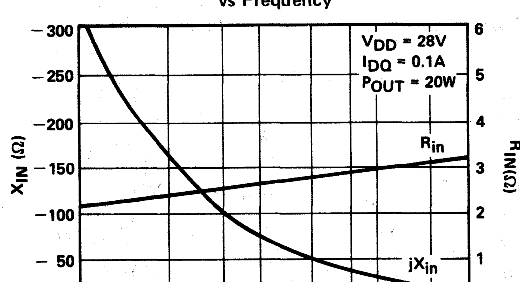
VMP4 175Hz

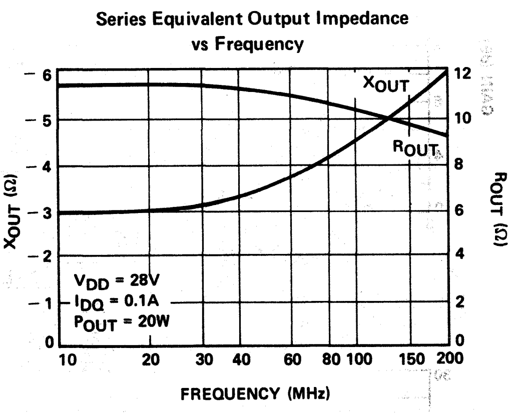




Parts List

C_1, C_3, 5–80 pFd
C_2, C_4, 3–30 pFd
L_1, L_3, 2 turns #20 enamel wire, close wound on 1/4" dia.
L_2, 7 turns #20 enamel wire, close wound on 1/4" dia.

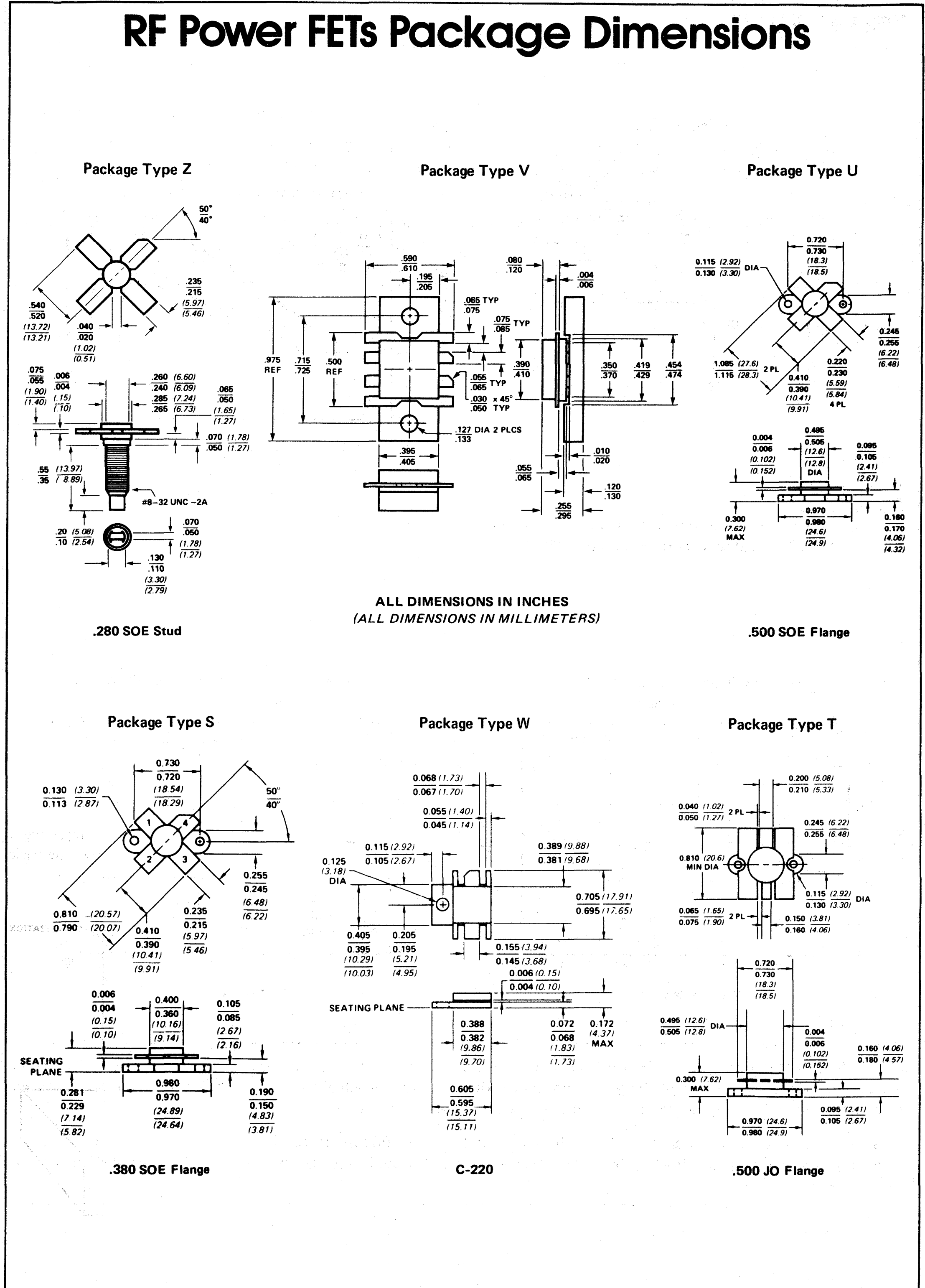




CAUTION: Beryllium Oxide — The top cap of this device is alumina which is harmless. However the ceramic portion between the leads and the metal flange is Beryllium Oxide, the dust of which is toxic. Care must therefore be taken during handling and mounting the device to prevent any damage to this area.

Steps must be taken to ensure that all those who may handle, use, or dispose of this device are aware of its nature and of these necessary safety precautions. In particular the transistor should never be thrown out with general industrial or domestic waste.

RF Power FETs Package Dimensions



Application Note AN80-2

Meet the Power-MOSFET Model

A modeling of the MOSFET transistor for high frequency design

Ed Oxner

Vertical MOS transistors for high frequency applications have, within the past year, mushroomed in popularity partly because of the inherent temperature-related advantages unique to the technology. Such advantages include no thermal runaway, no current hogging and, to a lesser extent, a greatly reduced secondary breakdown phenomenon. As a result of this increased popularity it is important that a model be available that allows the designer the freedom to use CAD (Computer Aided Design) techniques for design optimization. Although VMOS models have been offered by several investigators, none has achieved a fully satisfactory representation that offers viable results over wide ranges of frequencies[1,2].

The principal deficiency of these earlier models appears to lie in the heretofore neglect of the parasitic bipolar transistor inherent in a vertical channel MOS structure [although not discussed in this paper, the published models of the double-diffused DMOS transistor also suffer from this same neglect[3]]. This parasitic npn bipolar transistor arises from the interaction of the p-channel (base), the n+ source (emitter) and the n– drain drift epitaxy (collector).

At DC and frequencies below 5 MHz, it appears that the elements of this parasitic npn bipolar transistor have little affect on amplifier performance. However, as the frequency rises that continued neglect of including this parasitic transistor into the model becomes increasingly severe.

Device Design

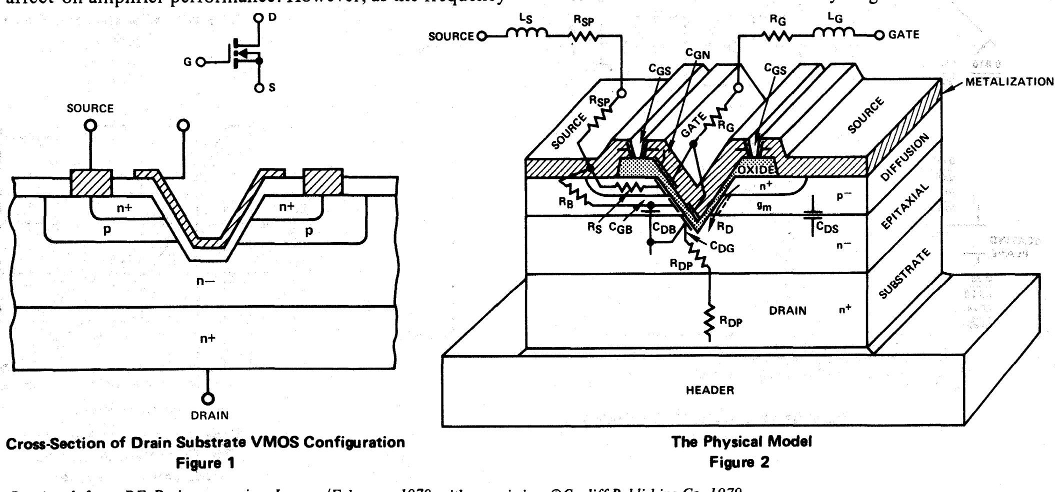
Much has been written offering the casual reader a basic understanding of VMOS design[4,5]. Beginning as a four-layer bipolar transistor all similarity ends when a V-groove is anistropically etched vertically into the structure providing access to the p-channel for an overlay metal gate. Such design offers an opportunity for high-frequency performance not easily possible with planar silicon MOS technology.

To effectively reduce the parasitic npn bipolar transistor effect the p-channel (base) is shorted to the n+ source (emitter) as shown in Figure 1. Generally with the base tied to the emitter an npn bipolar transistor remains in a non-conducting state.

DEVICE SIMULATION

The Physical Model

Once a physical model has been constructed, achieving a workable schematic model is easy. Figure 2 shows the basic



Cross-Section of Drain Substrate VMOS Configuration
Figure 1

The Physical Model
Figure 2

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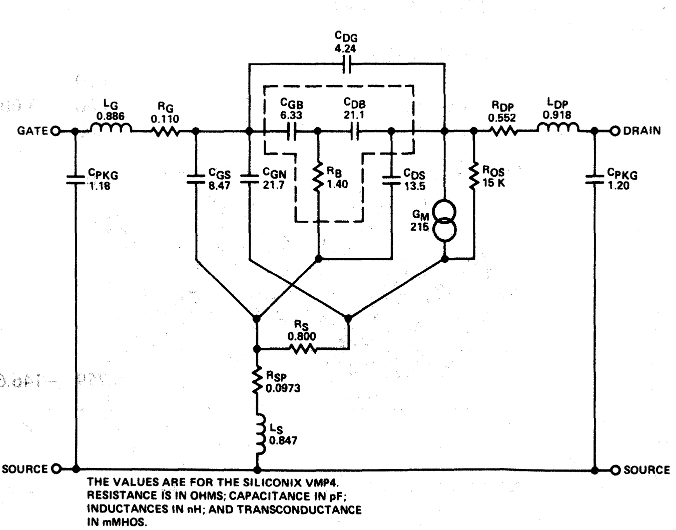
four-layer structure: An n+ substrate – the wafer itself – with an n– epitaxy into which has been diffused, first a p doped layer and then into this p layer n+ diffusion. Needless to say, this figure is not to scale! Left alone this would be the beginning of a typical bipolar transistor. A V-groove, suitable oxide and an overlay metal for gate and source completes the physical model. The model is then mounted on a header – in the case for the Siliconix VMP4 a flanged 380 SOE high-frequency package – and, finally, lead bonds attach the source and gate to their respective package terminals. Adding the parasitic capacitors and resistors is obvious. The result is a physical model of the VMOS high-frequency transistor, VMP4.

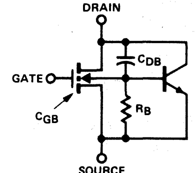
The Schematic Model

Using the physical model one can trace the entire electrical path and place all the parasitic elements that comprise the schematic model of the VMOS transistor. Figure 3 identifies each element of the schematic model. The element, R_{OS} ($1/G_{OS}$), represents the output resistance (conductance) which cannot be physically realized. L_G, L_S and L_{DP} are not intrinsic (that is, not part of the actual semiconductor element) but represent the package parasitic inductances of the Siliconix VMP4. R_G and R_{SP} represent resistive losses in both the gate and source metallizations as well as the lead losses. C_{GS} differs from C_{GN} in that the former is the field capacitance whereas the latter is that parasitic capacitance existing between the gate metal and the n+ source diffusion.

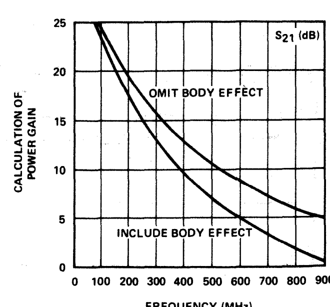
The parasitic npn bipolar transistor evident in Figure 1 must be considered as contributing parasitic elements (R_B, C_{GB} and C_{DB}) as well as being a potential parasitic generator; that is, contributing a finite Beta as an active element. The last is, indeed, possible and some explanation is necessary. Although the VMOS source is metallically tied to the base to reduce the effects of this parasitic npn bipolar transistor, it so happens that the resistivity of the p diffusion, that forms both the VMOS channel and the parasitic transistor's base, has a finite resistance (measured as ohms-per-square). Although at the point of metallic contact the base-to-emitter resistance is effectively zero, nonetheless as the distance is removed from the short the bulk resistance increases, so Figure 1 can be 'corrected' as shown in Figure 4. Should a voltage exist across this base resistance, R_B, it is conceivable that the parasitic npn bipolar transistor can turn on. One obvious means of placing a voltage across this resistance is by coupling the output voltage on the drain through the drain-base capacitor, C_{DB}. However, it was determined that this parasitic npn bipolar transistor, acting as an independent parasitic generator is effectively muted having been found not to be a major contributor to the performance of the VMP4 at HF through VHF (400 MHz). Nevertheless, the contribution of the npn bipolar transistor's parasitic elements, R_B, C_{GB} and C_{BD}, as an RC feedback network are of paramount importance as illustrated in Figure 5 where the intrinsic gain, S_{21} (dB), of the VMOS model is computed both with and without the contribution of these parasitic elements.



The Schematic Model VMOS (VMP4)
Figure 3



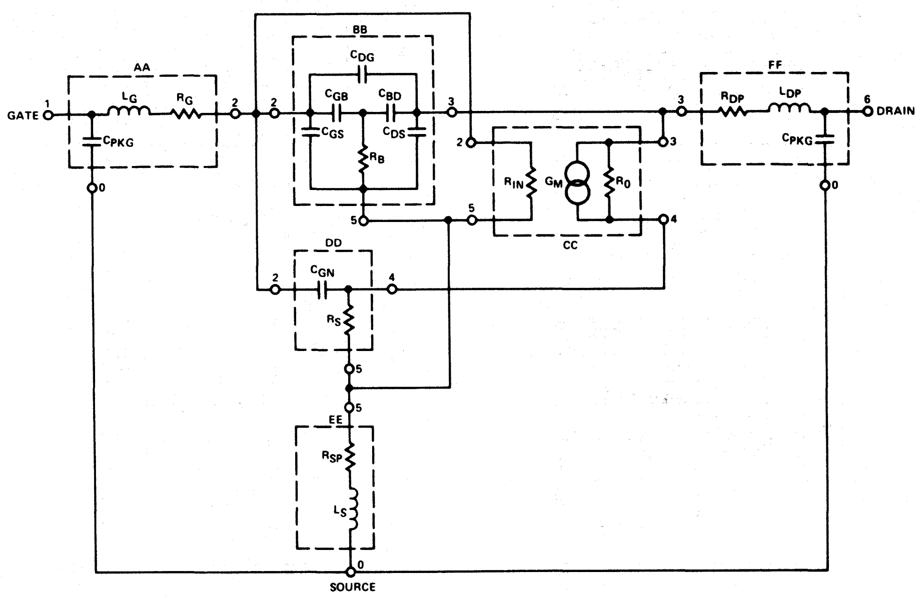
VMOS with a Parasitic npn Bipolar
Figure 4



Effect of Including/Excluding The Body Resistance in the Calculation of S_{21}(dB)
Figure 5

Experimental Results

Measured scattering parameters were used as the basis for establishing an exact model. Nodal analysis using the Circuit Optimization Program, Compact[6] working with 15 variables allowed the interconnection of 3 and 4 port networks as illustrated in Figure 6. In the Compact program variables are identified as negative quantities. The final program used to determine the values of each element of the VMP4 transistor is listed in Figure 7. Please be aware that one does not simply insert measured S-parameters and let the program crank numbers endlessly. No indeed. First you have to have a good idea of 'where you're coming from,' and use good judgment as to the initial values. Compact's values are an optimization of the initial data to arrive at parameter-fitting model.



Nodal Analysis Flow Chart For Compact Synthesis
Figure 6

```
CAP  AA  PA    1.18
SRL  BB  SE   -0.110          -0.886
CAX  AA  BB
CAP  BB  PA   -8.47
CAP  CC  SE   -6.33
RES  DD  PA   -1.40
CAP  EE  SE  -21.10
CAP  FF  PA  -13.50
CAX  BB  FF
CAP  CC  SE   -4.24
PAR  BB  CC
GEN  CC  VC    0.100E+11      0.150E+05   215
CAP  DD  SE  -21.7
RES  EE  PA   -0.800
CAX  DD  EE
SRL  EE  SE   -0.973E-01      -0.847
SRL  FF  SE   -0.552          -0.918
CAP  GG  PA    1.20
CAX  FF  GG
CON  AA  T3    1.00            2.00  0.0
```

```
CON  BB  T3   2.00          3.00  5.00
CON  CC  T4   2.00          5.00  4.00   3.00
CON  DD  T3   2.00          4.00  5.00
CON  EE  T2   5.00          0.00
CON  FF  T3   3.00          6.00  0.0
DEF  AA  T2   1.00          6.00
TWO  BB  S1   50.0
SET  AA  BB
PRI  AA  S1   50.0
END
200
END
0.77  -146.3  2.14  57.5  0.035  -6.0  0.759  -146.6
END
0.001
1     1     1     0.627
END

EOF:
```

Compact Program Including the Parasitic Elements of npn Bipolar in a Nodal Analysis
Figure 7

R_{IN} (in Figure 6) is used simply as a sense element required to realize a 4-port generator. To reduce its effect, a value of 1E10 ohms was assigned. S-parameters measured at 200 MHz were entered into the program and the computed Y-parameters were then compared with measured values and found to be in close agreement as shown in Figure 8.

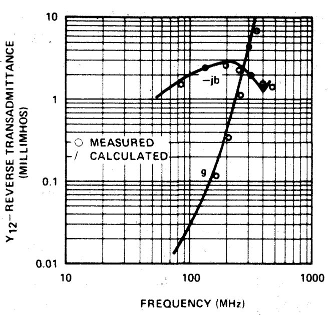


Figure 8(a)

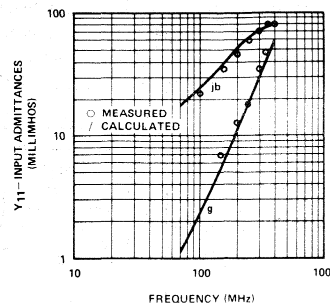


Figure 8(b)

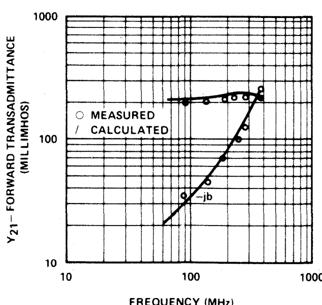


Figure 8(c)

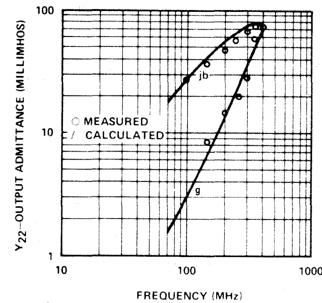


Figure 8(d)

VMP4
Figure 8

CONCLUSIONS

This model offers a designer an excellent start in computer aided design of amplifiers and what-not. To ease the burden of transferring these data into your Compact program, the Siliconix VMP4 S-parameter data file is available in the Compact library under the manufacturer's code 'SIX' and device code 'AA.'

Compact is presently available from 6 networks: NCSS; Control Data/Cybernet; GE/Honeywell; United Computing Systems; Tymshare; and, Computility/Call Data.

Finally, I would like to acknowledge the sacrificing work of my close associate, Larry Leighton for his efforts in assisting the development of this model.

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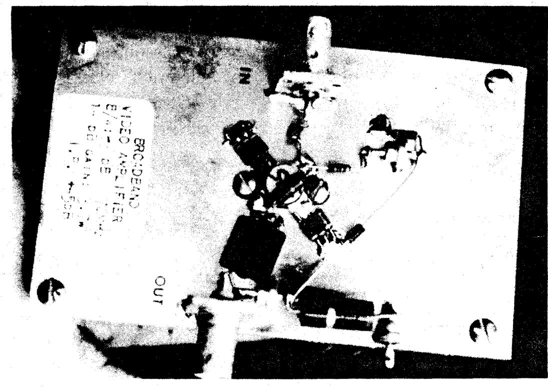
Application Note AN80-3

Build a Broadband Ultralinear VMOS Amplifier

This theory and construction article offers a unique opportunity to use the new power MOSFET. Amplifier two-tone intermodulation products can be as low as 70 dB below the carrier.



A broadband amplifier using the VMP4 VMOS. It has a range from 1-70 MHz.

The high-frequency vertical MOS power transistor is nearest to being the most truly ubiquitous transistor ever to appear in the marketplace. Not only can VMOS perform in the conventional AM and SSB amplifiers, but because of no minority-carrier storage time, it provides superb performance in high-efficiency switch-mode Class E and F amplifiers. In fulfillment of the definition of *ubiquitous,* the VMOS transistor can be used interchangeably either as a power transistor or as a small-signal low-noise transistor.

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What Is VMOS?

VMOS, or more properly, vertical metal-oxide semiconductor field effect transistor, evolved from the double-diffused epitaxial bipolar technology and it's easy to see this evolution in Figure 1. The obvious differences are the V-groove gate region, which has been anisotropically etched into the structure, and the joining of the source (emitter) to the base to assure that the parasitic npn bipolar transistor remains cut off during operation.

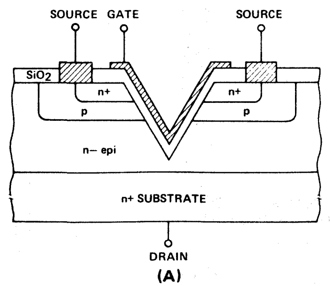
The VMOS substrate of n+ material forms the drain. The n– epitaxial (epi) layer offers increased breakdown and, especially important for high-frequency performance, greatly reduced feedback capacitance. This epi layer also enhances the possibilities for the development of very high-voltage high-frequency power transistors which will soon revolutionize transmitter design.

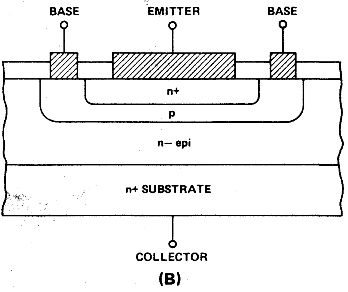
Unlike the more familiar DMOS (double-diffused MOS) technology where a cross section may be viewed (Figure 2) and compared to the VMOS cross-section (Figure 1), for each VMOS V-groove gate, two channels are formed which offer increased current density and, of utmost importance, halving the typical source-drain dynamic ON resistance of the DMOS alternative. Much like DMOS, also a majority-carrier semiconductor with no minority carriers by virtue of the fact that current flow, in the form of electrons, is entirely through the n-type material (the p-channel becoming inverted by the gate bias), the length of the channel plays a critical role in influencing the maximum F_T that is obtainable. Setting aside the deleterious effects of the parasitic elements inherent in any transistor, the calculated F_T for a silicon short-channel device such as either DMOS or VMOS approaches 20 GHz! Of course one cannot set aside these parasitic elements, and as a consequence, the theoretical limits are unattainable.

Why Use VMOS?

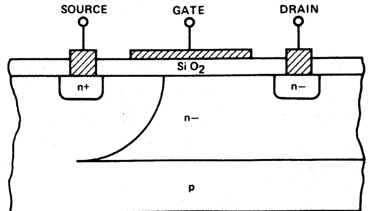
Like all FETs, whether they be junction or MOS, VMOS is a majority-carrier transistor by virtue of the fact that electron flow is entirely through n-type material (speaking, of course, for an n-channel device; for a p-channel device the electron flow would be entirely through p-type material, the n-channel having inverted by virtue of the negatively biased gate-potential). Consequently, an FET is somewhat analogous to an electric field-controlled bulk semiconductor resistor, and therefore, has a positive temperature coefficient. That is, as this semiconductor warms, its resistance rises. This is directly contrary to any bipolar transistor, for its temperature coefficient, by the same definition, would be negative.

All bipolar transistor failure can be traced directly to this negative coefficient which contributes to thermal stress: secondary breakdown, thermal runaway and current crowding. Since both DMOS and VMOS have the opposite characteristic under thermal stress, none of these failures occur. Consequently, with VMOS one does not experience any deleterious effects caused by either paralleling multiple VMOS power transistors or from severely mismatching the load.





A Comparison of Similarities Between a Vertical MOSFET and a Four-Layer Bipolar Transistor (B). EPI Indicates the Epitaxial Layer
Figure 1



Cross Section of a Double-Diffused DMOS Transistor
Figure 2

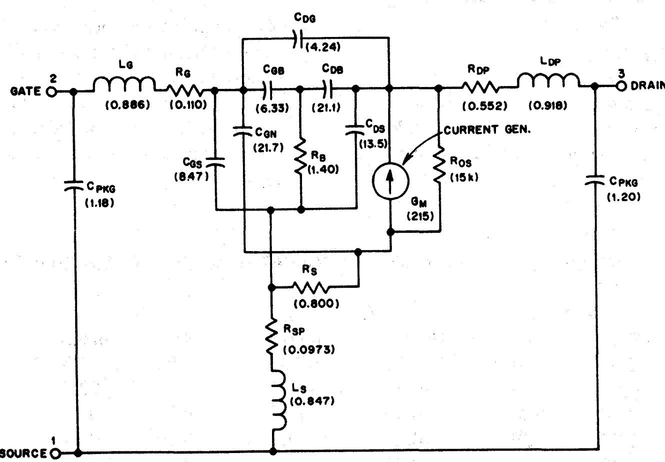
How to Use VMOS

VMOS is an insulated-gate MOSFET differing greatly from the common dual-gate MOSFET. The typical dual-gate MOSFET handles a few milliamperes of drain current whereas VMOS can handle *amperes*. Because of its mass – and coupled with mass, a much higher parasitic capacitance – there is little fear of an inadvertently blown gate. Because of the higher input capacitance, no gate-protection diode is necessary for protection in handling. To allay any arguments to the contrary, in over three years I have not experienced any failures stemming from gate puncture arising from mishandling.

VMOS is a Type C FET, an enhancement-mode MOSFET. That means it remains fully off when either zero bias or negative bias is applied to the non-zenered gate (negative bias *cannot* be applied to a zenered VMOS gate). With the application of a positive potential beyond the threshold voltage (specified as between 0.8 V and 2.0 V), drain current will flow. Once a certain quiescent current is reached, any further increase in gate voltage results in a linear increase in the DC drain current. Biasing VMOS is different than biasing bipolar transistors simply because VMOS only requires a positive potential to activate drain-to-source current flow. A cursory glance at a typical bias network might not appear too different but, unlike the bipolar transistor which requires a moderate to heavy base current, VMOS biasing requires no current at the gate. Consequently, the RF isolation between the gate and the bias network can be a simple high-value carbon resistor. Such a method was used in the video amplifier design described in this article, where a 27 KΩ resistor ties between the 4.7 KΩ voltage divider and the 20 V zener diode.

Modeling the VMOS VMP4

The equivalent circuit for the VMOS transistor has been previously published and is repeated in Figure 3. This

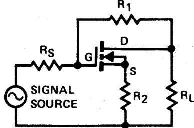


The Vertical-MOS VMP4 Circuit Equivalent. Values in Parentheses are for this Siliconix Unit. Resistance is in Ohms, Capacitance in pF, Inductance in nH and Transconductance is in mmhos. Identification of the Elements (left to right) is Tabulated Below.
Figure 3

C_{PKG} Input and output capacitances of the VMOS package.
L_G Gate inductance.
R_G Gate resistance.
C_{GS} Field capacitance.
C_{GN} Capacitance from gate to n–.
C_{GB} Capacitance from gate to body.
C_{DG} Capacitance from drain to gate.
R_B Body resistance of P diffusion.
C_{DB} Capacitance from drain to body.
R_{OS} The element R_{OS} ($1/G_{OS}$) represents the output resistance (conductance) which cannot be physically realized.
R_{DP} Drain resistance of die attach material and package.
L_{DP} Drain inductance of package material.
L_S Source inductance.
R_{SP} Source resistance.
R_S n^+ diffusion resistance.

L_G, L_S and L_{DP} are not intrinsic (that is not part of the actual semiconductor element) but represent the package parasitic inductances of the Siliconix VMP4. R_G and R_{SP} represent resistive losses in both the gate and source metallizations as well as the lead losses. C_{GS} differs from C_{GN} in that the former is the field capacitance existing between the gate metal and the n+ source diffusion.

model, when properly simulated to include the parasitic npn bipolar transistor elements using a computer simulation program (COMPACT), offered excellent correlation with measured data over a reasonably wide bandwidth. Values of two-port admittance parameters obtained from the computer simulation are offered in Table I. For frequencies below 100 MHz these values must be considered as approximate because the characteristic break-frequency typical of all common-source connected amplifiers using FETs and MOSFETs was not included in the simulation. However, for general design the values in Table I offer the circuit designer sufficient accuracy so that, in all probability, little or no tweaking of the finished circuit is required for optimum performance.



The Simplified Circuit of a Broadband Video Amplifier
Figure 4

Designing the Amplifier

The design goals included the desire to cover 80 through 10 meters with flat gain, low input and output VSWR, and perfect linearity. That is, have the intermodulation products as low as possible. To meet these objectives the basic equivalent circuit shown in Figure 4 was chosen. The resistances, R_S and R_L, represent generator (source) resistance and load resistance, both 50 ohms for this design. Feedback resistor R_1 and source resistor R_2 combine to flatten the gain response and set the input resistance to match 50 ohms. R_1 and R_2 are determined by using the following formulas.

$$R_1 = \frac{\sqrt{R_S R_L}}{2} \cdot \left[\sqrt{G} + \sqrt{G + 4\left(1 + \sqrt{G} \cdot \frac{R_S + R_L}{2\sqrt{R_S R_L}}\right)}\right] \quad (1)$$

$$R_2 = \left(\frac{R_S R_L}{R_1}\right) - \frac{1}{G_M} \quad (2)$$

where

G is the desired stage gain for the amplifier, and

G_M is the forward transconductance value of the transistor expressed in mhos. (Y_{21} real)

Manipulating these formulas for R_1 and R_2, values obtained were a bit different than easily obtained standard resistor values. So R_1 was adjusted to 270 ohms (the calculated value was only 273 ohms), and R_2 to 5 ohms. In the final assembly, R_2 consisted of six 30-ohm resistors in parallel, soldered three to a side from each source lead on the VMP4 to chassis.

TABLE I. COMPUTED TWO-PORT Y-PARAMETER MATRIX IN MILLIMHOS, VMP4

	Y11		Y21		Y12		Y22	
Freq.	**(Real**	**Imag.)**	**(Real**	**Imag.)**	**(Real**	**Imag.)**	**(Real**	**Imag.)**
1.0	0.00	0.24	210.58	−0.30	0.00	−0.03	0.07	0.25
2.0	0.00	0.48	210.58	−0.61	0.00	−0.05	0.07	0.50
5.0	0.00	1.20	210.59	−1.52	0.00	−0.13	0.07	1.24
10.0	0.02	2.39	210.64	−3.05	0.00	−0.27	0.09	2.48
20.0	0.09	4.78	210.84	−6.11	0.00	−0.53	0.17	4.95
30.0	0.20	7.17	211.18	−9.19	0.01	−0.80	0.31	7.43
50.0	0.56	11.97	212.25	−15.47	0.02	−1.31	0.74	12.41
100.0	2.32	24.09	217.24	−32.49	0.11	−2.50	2.88	24.95
120.0	3.42	29.00	220.13	−40.12	0.18	−2.91	4.21	30.01
140.0	4.78	33.94	223.51	−48.43	0.28	−3.27	5.86	35.11
160.0	6.42	38.92	227.33	−57.56	0.43	−3.57	7.85	40.21
180.0	8.40	43.91	231.53	−67.69	0.64	−3.79	10.24	45.31
200.0	10.75	48.88	236.01	−79.01	0.94	−3.93	13.07	50.36
220.0	13.52	53.79	240.62	−91.74	1.36	−3.98	16.39	55.30
240.0	16.73	58.58	245.17	−106.10	1.92	−3.92	20.25	60.06
260.0	20.45	63.15	249.36	−122.30	2.69	−3.76	24.69	64.52
280.0	24.67	67.39	252.81	−140.54	3.71	−3.50	29.72	68.54
300.0	29.40	71.16	255.01	−160.94	5.06	−3.17	35.35	71.95
320.0	34.56	74.26	255.36	−183.50	6.81	−2.81	41.48	74.52
340.0	40.05	76.52	253.13	−208.04	9.04	−2.49	47.97	76.04
360.0	45.63	77.74	247.61	−234.10	11.81	−2.31	54.55	76.29
380.0	51.00	77.81	238.15	−260.90	15.16	−2.40	60.87	75.12
400.0	55.76	76.70	224.34	−287.36	19.10	−2.93	66.44	72.51

The next step, which for most amateurs may not be possible, is to simulate the performance using a computerized optimization program, in this case one called COMPACT (Computer Optimization of Microwave Passive and Active CircuiTs). For those interested in the details, the basic program is offered in Table II and the final analysis showing the theoretical performance of the video amplifier is given in Table III. If we remember that scattering parameters are reflection coefficients, the values of S_{11} (input) and S_{22} (output) suggest that a reasonably good match should be possible. The expanded Smith Chart projections in Figure 5 offer easy visualization of the expected results across the 2 MHz to 30 MHz bandwidth. The overall anticipated performance, taken from Table III data, suggests nearly 13 dB forward power gain ($S_{21}{}^2$) and so-so stability (K greater than 1.0).

TABLE II. THE COMPUTERIZED OPTIMIZATION PROGRAM (COMPACT)

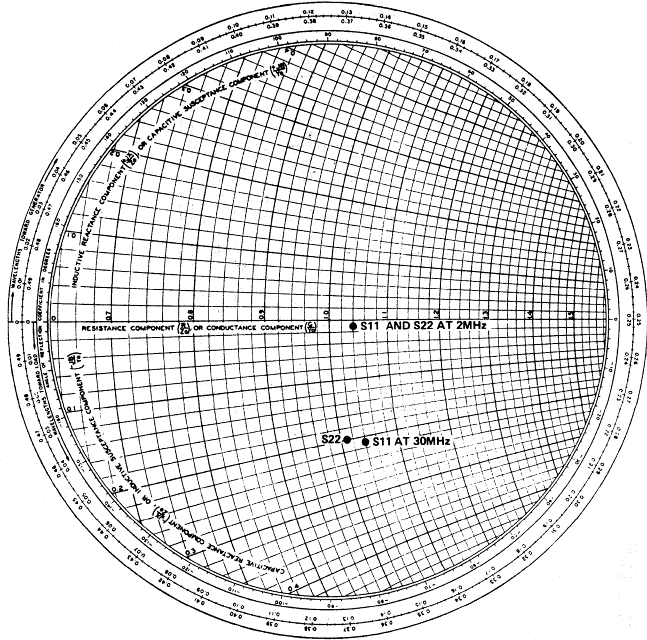
```
RES   AA  SE   -270.0   2     30
TWO   BB  S1     50.0   END
PAR   AA  BB            1.00  -6   20.94  175.5  0.005  85.6  0.99  -6
RES   CC  PA     -5.0   0.81  -72  14.36  125.5  0.054  38.5  0.81  -74
SER   AA  CC            END
PR1   AA  S1     50.0   EOF:
END
```

This program simulates amplifier performance. See text.

TABLE III. COMPUTER PRINTOUT OF THE ULTRALINEAR AMPLIFIER PERFORMANCE

	S_{11}		S_{21}		S_{12}		S_{22}		S_{21}	K
Freq.	(Magn	Angle)	(Magn	Angle)	(Magn	Angle)	(Magn	Angle)	DB	Fact.
2.00	0.02	−17	4.26	178.8	0.159	−0.3	0.02	−18	12.58	1.08
30.00	0.10	−79	4.21	161.3	0.156	−2.4	0.10	−82	12.49	1.06

These are polar S parameters in a 50-ohm system.



These Expanded Smith Chart Projections Offer Easy Visualization of the Expected Broadband Amplifier Results Across a 2 to 30 MHz Bandwidth. The plot of the Calculated Values for S_{11} and S_{22} is Shown

Figure 5

After adding the proper biasing and voltage-isolating capacitors, the final operational circuit emerges as shown in Figure 6. Performance is graphically offered in Figure 7. Additional measurements include a 1 dB saturation output power of 3.7 watts and a spot noise-figure measurement of 4 dB at 30 MHz.

There is little explanation needed for the constructor. Layout is not overly critical. Leads should be kept short, in particular for R_1 and the batch paralleling R_2 which, incidentally, should be carbon-composition resistors. The heat sink shown is unquestionably an overkill but using one equal in size to the copperclad board is a great convenience.

I acknowledge the diligent efforts of my colleague, Larry Leighton, WB6BPI. For his contributions to the success of this project, I express my gratitude.

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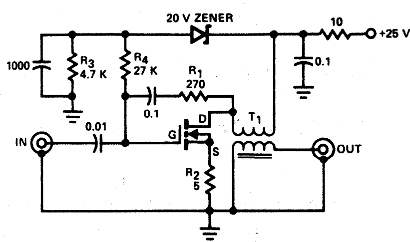
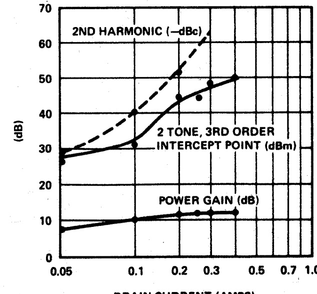


Schematic Diagram of a Broadband Video Amplifier. T_1 Consists of 9-1/2 Turns of No. 30 Enameled Wire Bifilar Wound on a Stackpole No. 57-9130 Balun. Resistance is in Ohms and Capacitance is in µF.

Figure 6



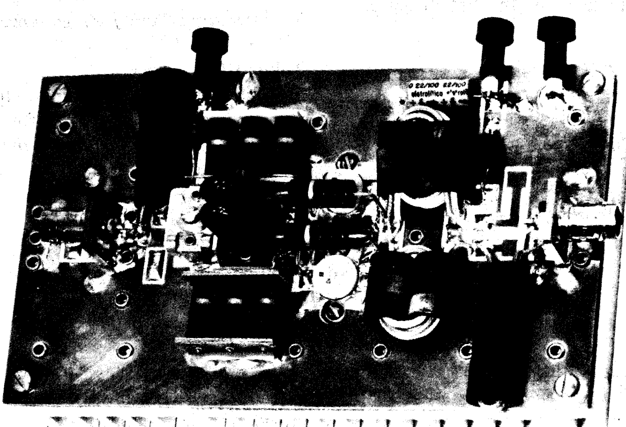
A Graphical Representation of Performance of the 2 to 30 MHz Ultralinear VMOS Amplifier

Figure 7

Siliconix

Application Note AN80-4

VHF Power Amplifier Design Using VMOS Power FETs



The goal isn't simply to fit VMOS into a VHF amplifier but to first derive a basic equation that will assist us in formulating a technique to simplify VHF power amplifier design when using VMOS. Secondly, we will design a power amplifier using a real RF VMOS power transistor. This amplifier should offer both high fixed gain and a low input VSWR across the military communications band of 30 MHz to 88 MHz.

Deriving the Formula

A good VMOS power FET has constant low-frequency g_m, high input impedance and unusually low feedback. Because of these unique features the well-known general expression for power gain can be further simplified to provide what amounts to a "cookbook" formula for power amplifier design.

The general expression for power gain for any linear amplifier is:

$$Gp = \frac{|y_{21}|^2 \, Re(Y_L)}{|Y_L + y_{22}|^2 \, Re\left(y_{11} - \dfrac{y_{12}\, y_{21}}{y_{22} + Y_L}\right)} \qquad (1)$$

To begin our derivation we first set y_{12} equal to zero and the remaining imaginary admittance terms (b_{11}, b_{21}, b_{22}) also to zero. Later we'll justify this action.

It should be noted that within the general expression (Equation 1) is the formula defining the input admittance, Y_{in}, of the amplifier.

$$Y_{in} = y_{11} - \frac{y_{12}\, y_{21}}{y_{22} + Y_L} \qquad (2)$$

Since we opted to equate y_{12} to zero, we immediately find that $Y_{in} = y_{11}$. One design objective is to provide a low input VSWR, or in other words a power match, so

$Y_{in} = Y_S^*$(source admittance).

Interestingly, with the reverse transadmittance, y_{12}, set to zero, by definition the input admittance is unaffected by the load, Equation 1 can be rewritten

$$\frac{|y_{21}|^2 \, Re(Y_L)}{|Y_L + y_{22}|^2 \, Re(Y_S)} \qquad (3)$$

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Equation 3 can be further simplified by first substituting

$(y_{21})^2 = (g_m)^2$
$\text{Re } Y_L = 1/R_L$
$\text{Re}(y_{22}) = 1/R_{out}$
$\text{Re } Y_S = 1/R_S$

where

R_L is the load resistance;
R_S is the source resistance; and,
g_m is the forward transconductance of the VMOS power transistor.

which results in:

$$G_P = 10 \log \left[\frac{g_m^2 \ R_S}{R_L \left(\frac{1}{R_{out}} + \frac{1}{R_L} \right)^2} \right] \quad (4)$$

Solving for R_S:

$$R_S = \frac{10^{\left(\frac{dB}{10}\right)} \left[R_L \left(\frac{1}{R_L} + \frac{1}{R_{out}} \right)^2 \right]}{g_m^2} \quad (5)$$

where $R_{out} = 1/\text{Re}(y_{22})$ (taken from Table I of small signal Y parameters).

Now fixing a resistor, R_S, across the gate-to-source terminals of the VMOS FET the gain and input impedance (hence source impedance) are set independent of the operating frequency within the VHF bandwidth of the amplifier

Why Get Excited about VMOS Design?

What with the prospects that power VMOS FETs offer in high-frequency amplifier design, one might conclude that VMOS is the designer's choice. See what you think.

1. Stability
Within the VHF region the shunt input impedance loading requirements are constant since the transconductance of the VMOS power FET exhibits little change with frequency. *Very little feedback is required to ensure total stability.*

Because little feedback is required *the overall efficiency is improved* and out-of-band stability is enhanced.

Because VMOS RF power FET admittance parameters are little affected over the operating drain current *small-signal Y parameters become increasingly useful in establishing basic stability criteria for high-power design.*

2. Input Admittance
A stable quiescent drain current (I_D) regardless of drive or operating temperature (T_A) offers a near-constant input impedance *governed mainly by the input impedance of the matching circuit and not by the reflective load impedance.*

3. Gain
Without benefit of feedback and with a fixed load the amplifier offers flat gain across the entire 30 MHz to 90 MHz bandwidth. *Reverse gain exceeds −35 dB.*

4. Power Output
VMOS Power FETs, exhibiting a constant $R_{DS(On)}$ [$V_{DS(sat)} = R_{DS(on)} I_D$] regardless of frequency, will provide a leveled saturated output power. Most importantly: *they can withstand a 20:1 VSWR at any phase angle.*

5. Noise Figure
Because VMOS is a bulk semiconductor without the bipolar's base-emitter diode it appears that the measured small-signal noise figure represents *what can be expected when used in a power amplifier.*

In addition to these are the now well-known thermally-related benefits that VMOS offers: *no thermal runaway* and *no current hogging.*

Frequency Contraints

VMOS FETs possess a finite and frequency invarient input capacitance. There is an upper frequency at which this

TABLE I. TWO-PORT Y-PARAMETER MATRIX IN MILLIMHOS USING DV2880, 28 V, 1.6 A

Freq.	Y11		Y21	Y12	Y22	
10.0	0.2	10.1	697.2 – 16.0	0.0 – 1.2	14.9	8.2
20.0	0.7	20.1	697.7 – 32.1	0.0 – 2.3	15.3	16.3
30.0	1.6	30.2	698.5 – 48.4	0.1 – 3.5	16.0	24.5
40.0	2.8	40.3	699.5 – 64.8	0.1 – 4.6	17.0	32.6
50.0	4.4	50.3	700.8 – 81.5	0.2 – 5.6	18.3	40.7
60.0	6.3	60.4	702.4 – 98.5	0.4 – 6.7	19.8	48.8
70.0	8.6	70.5	704.2 – 116.0	0.5 – 7.7	21.7	56.7
80.0	11.4	80.5	706.2 – 133.9	0.7 – 8.6	23.9	64.7
90.0	14.5	90.5	708.4 – 152.3	0.9 – 9.5	26.4	72.5
100.0	18.1	100.4	710.6 – 171.4	1.3 – 10.2	29.3	80.2

capacitance reactance will become appreciable with respect to R_S resulting in mismatch loss. Consequently, any designed increase in gain which also raises R_S (Equation 5) will adversely affect the input Q thus limiting the input frequency response.

Furthermore, as the frequency rises, y_{12} should not be equated to zero. From Equation 2 y_{12} affects Y_{in}, which, in turn, affects R_S which adversely affects mismatch loss. The limiting upper frequency is established by the maximum permissible input VSWR.

Into the Design

Our objective is to design a push-pull amplifier capable of at least 12 dB of power gain and outputting 100 W, at a drain voltage of 28 V across the 30 MHz to 88 MHz band. Input VSWR not to exceed 1.5.

The first step is to define the load line using the classic formula

$$R_L = \frac{[V_{DD} - V_{DS(on)}]^2}{2P} \qquad (6)$$

The Siliconix RF VMOS transistor, DV2880, is rated to output 80 W minimum at a power gain of 10 dB at 175 MHz with total dissipation of 160 W. $R_{DS(on)}$ is typically 0.5 ohm. We felt that this represented a comfortable margin and selected it for our design.

A push-pull design establishes that each VMOS should supply 50 W minimum if we assume that the matching transformers are lossless. With a drain supply of +28 V and the estimated peak drain current of approximately 3.6 A, we can calculate $V_{DS(on)}$:

$$V_{DS(on)} = R_{DS(on)} I_D = 0.5 \times 3.6 = 1.8 \text{ V}.$$

Using Equation 6 the load line is calculated at 6 ohms.

The most convenient way to establish this load line is by using ferrite transmission-line transformers. However, were the load line to output port impedance not an integer ratio, the match would require a more complicated design effort. In this design the 6 ohm load line can be closely achieved with the relatively simple combination of a 1:1 unbalanced-to-balanced balun followed by a 4:1 balanced-to-balanced transformer. Together this combination provides a balanced 6.25-0-6.25 ohms across the drains of the push-pull FETs.

With the drain load design complete, next establish the amplifier's gain and this is done with resistive input loading, R_S. Having gone through the exercise designing the output load we are very close to having the necessary information to calculate R_S. All that remains is to select a value for R_{out} [$Re(y_{22})$] which we take from Table I. To ensure our gain over the entire passband, it's wise to select worse-case $Re(y_{22})$ and that value is found at 90 MHz to be 0.026 mhos, or R_{out} = 38 ohms. Using Equation 5:

$$R_S = \frac{10^{\left(\frac{12}{10}\right)} \left[6.25 \left(\frac{1}{6.25} + \frac{1}{38}\right)^2\right]}{(0.7)^2} = 7 \text{ ohms.}$$

Ideally we would need an input matching structure stepping down from 50 to 7 ohms which for this broadband amplifier would be both costly and unwieldy. Rather than complicate the design let us opt for a 'near match' by using the transmission-line transformer combination 1:1/4:1, 50 ohm unbalanced to 6.25-0-6.25 ohm balanced. By not meeting the value of R_S (6.25 ohms in lieu of the calculated R_S of 7 ohms) we will need to reaffirm what gain to expect from the amplifier. Using Equation 4:

$$G_P = 10 \log \left[\frac{(0.7)^2\, 6.25}{6.25 \left(\frac{1}{38} + \frac{1}{6.25}\right)^2}\right] = 11.5 \text{ dB.}$$

PARTS LIST

RFC – Ferroxcube P/N VK200 09/3B

T_1, T_6 – Two turns of RG-196 A/μ 50 Ω coax wound on three balun cores placed end on end cores are Stackpole P/N 57-0973.

T_2, T_3 – Two turns #22 twisted pair, four turns per inch, wound on two balun core. Core is Stackpole P/N 57-1503.

T_4, T_5 – Three turns of 25 Ω coax wound on 6 torroid cores. Cores are configured similar to balun style core, three cores per side. Two 50 Ω coax RG-196 A/μ were paralleled to simulate 25 Ω coax. Cores are Indiana General P/N F627-8-Q2.

The Matching Transformers

For both the input and output balanced-to-unbalanced 1:1 baluns, 2 turns of RG-196 A/μ coaxial were wound through 3 Stackpole balun cores, 57-0973, placed end-to-end. The drain load 4:1 transformer was wound with 3 turns of *parallel-connected* RG-196 A/μ (for an equivalent 25 ohms) through a balun-style core made by using 6 Indiana General torroidal cores, F627-8-Q2, 3 cores per side. The input 4:1 transformer was wound with 2 turns of twisted (4 turns per inch) #22 AWG Beldsol 8051 through a pair of Stackpole baluns 57-1503, also placed end-to-end.

Building the Amplifier

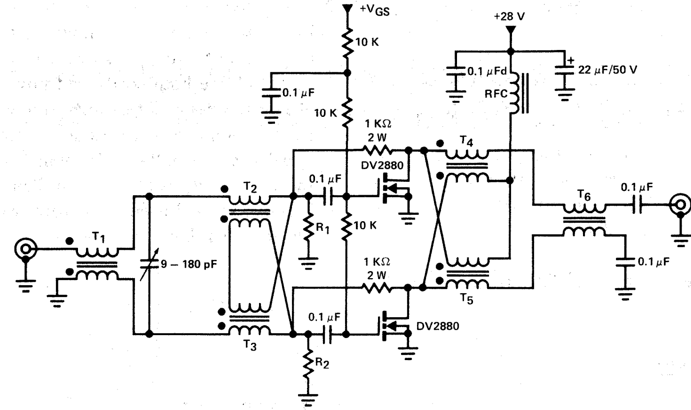
The construction is uncomplicated. Two problems are worth mentioning. First, the shunting resistors, R_S, made of 3

parallel-wired 2 W composition resistors (R_1 and R_2 in Figure 1) appear slightly inductive and fortuitously help compensate for the input capacitance of the VMOS transistors at the high end of the passband. Secondly, the input matching transformer requires a compensating trimmer capacitor, C_1.

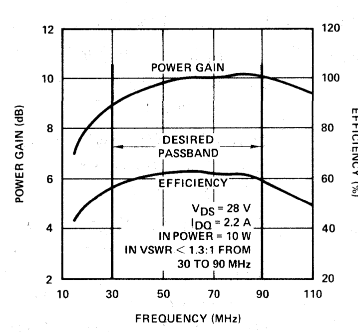
CONCLUSIONS

The performance of the finished amplifier (Figures 2 through 5) confirms the usefulness of Equation 5 in establishing both the desired gain and input VSWR. The latter is especially gratifying since VMOS power transistors offer a high input resistance across the VHF band. The combined loss of the matching transformers amounts to 1 dB.

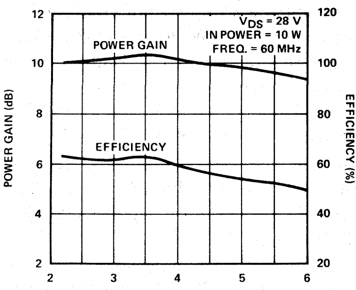
In operating the amplifier into a high output mismatch you will observe low level spurious oscillations which can be effectively removed by adding 1 KΩ feedback resistors. These resistors will not affect gain, gain flatness or input VSWR.

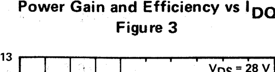


100 Watt Broadband VMOS Power Amplifier Using Siliconix DV2880 FETs
Figure 1

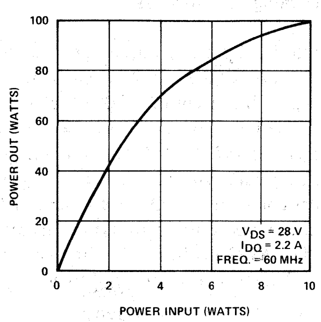


Power Gain and Efficiency vs Frequency
Figure 2

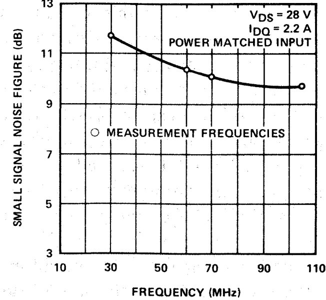




Power Gain and Efficiency vs I_{DQ}
Figure 3



Power Output vs Power Input
Figure 4



Small Signal Noise Figure vs Frequency
Figure 5

Application Note AN80-6

AGC for the VMOS RF Power Amplifier

The principles, circuitry and test results of AGC action on a VMOS 30-90 MHz 100 watt amplifier are detailed

Introduction

Power VMOSFETs are bulk semiconductors where majority carriers are controlled directly from a gate potential. There is no diode drop between gate and source characteristic of the bipolar transistor. VMOS is not inhibited by either a low forward or reverse breakdown; consequently, we are able to achieve considerable dynamic range by applying an AGC voltage to the gate of the power VMOSFET.

This paper offers measured data taken on a broadband 30-90 MHz VMOS Power Amplifier which is capable of 100 watts output under non-AGC conditions.

Wide dynamic range capability offers unique features heretofore unavailable in RF bipolar amplifier design. Furthermore, by the use of special feedback techniques it is possible to achieve high-efficiency low-level AM modulation.

Principles of AGC

VMOSFET drain current, I_D, is related to the applied gate voltage, V_{GS}, by a relationship called the transfer function. For VMOSFETs this transfer function may be closely approximated as:

$$I_D = K_5 \left[V_{GS} - V_{th} \right] \quad (1)$$

where $V_{GS} > V_{th}$; and K_5 is a constant.

This is in sharp contrast to the transfer function of both JFET and the bipolar transistor, respectively.

$$\text{[JFET]} \quad I_D = K_3 \left[1 - \frac{V_{GS}}{V_p}^{2} \right] \quad (2)$$

$$\text{[BJT]} \quad I_C = K_4 \left[e^{V_{BE}} - 1 \right] \quad (3)$$

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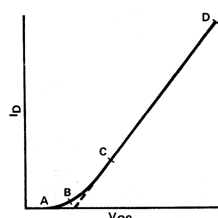
A plot of (1) overlaid by measured data, as shown in Figure 1 shows remarkable tracking. At the low $V_{GS} - I_D$ levels we see the transfer function decay from linear (C-D) to a square law region (B-C) to a sub-threshold region (A-B).



Transfer Curve of VMOS Transistor (Theory vs Measured)
Figure 1

Since we are not inhibited by narrow breakdown voltage limits between the gate-to-source we deduce from Figure 1 that by modulating the gate bias, V_{GS}, we can expect a reasonably wide dynamic range.

Figure 1 should be recognized as the static transfer characteristic of VMOS. A dynamic transfer characteristic would show saturation at high gate-to-source voltages, V_{GS}. Basing our AGC performance on gate bias we should see a power curve of similar form.

Power Output Versus V_{GS}

The quiescent drain current, I_{DQ}, of the push-pull power amplifier of Figure 2 was set at 2.2 amperes with a supply voltage of 28 volts. The gate supply voltage was 6.81 volts. With an input drive level of 8.5 watts the output power was measured at 100 watts at band center (60 MHz).

As the gate supply voltage decreased the RF output power followed suit as is shown in Figure 3.

Of special note in Figure 3 is that output power can be reduced to zero with a negative bias sufficient to overcome the self-bias that was caused by the RF drive. VMOSFETs are enhancement-mode transistors which turn OFF whenever their gate voltage reaches the threshold level, V_{th}.

During the measurements that gave us the results depicted in Figure 3 the operating drain current dropped from 5.4 amperes at an output power of 100 watts to less than 0.32 amperes when the output power reached 0.5 watt and finally to zero at 0 watt output.

Throughout the entire AGC range the input VSWR remained unchanged.

Power Output Versus I_D

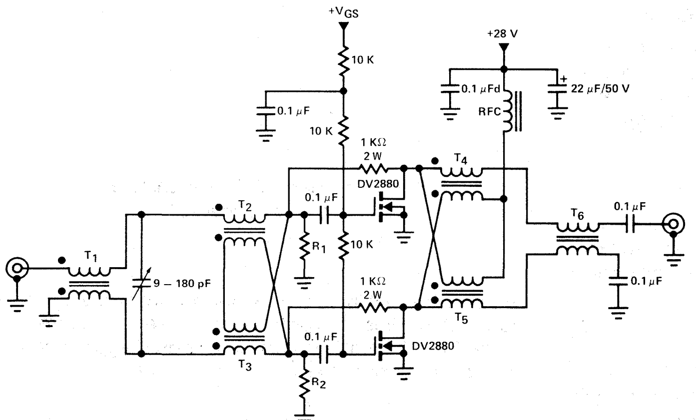
The broadband amplifier of Figure 2 performs over a 1.5 octave bandwidth with reasonably flat gain. Because of the usual idiosyncrasies inherent in the fabrication of matching transformers, the resulting performance of the amplifier showed a positive gain slope with increasing frequency.

Fixing a quiescent drain current of 2.2 amperes (by setting the gate bias at 6.81 volts) and establishing an RF drive level of 8.5 watts, the measured performance across the 30-90 MHz band is tabulated in Table 1.

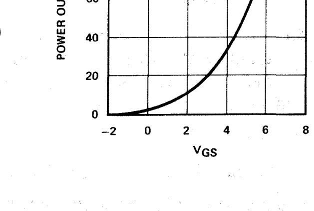
Note from Table 1 that as the drain current increases with increasing frequency the power output follows suit. This current-power tracking is characteristic of VMOSFETs as a result of the linear transfer characteristics shown in Figure 1.

Table 1
Power Output and Drain Current vs Frequency

Freq. (MHz)	I_D (A)	P_{OUT} (W)
30	4.99	84
40	5.13	89
50	5.25	95
60	5.43	100
70	5.58	102.5
80	5.83	105
90	6.00	107.5



100 Watt Broadband VMOS Power Amplifier
Figure 2



Output Power vs Gate-to-Source Bias
Figure 3

Since output power follows drain current we can presume that fixing the drain current will also stabilize the output power. Drain current was fixed at 5.46 amperes and the results are plotted in Figure 4 where they are compared against the power output when the drain current is allowed to float; that is, when V_{GS} is fixed.

AGC By I_D Control

Since power output can be stabilized by fixing the drain current which, in turn can be regulated by gate bias, then a feedback mechanism working entirely from the DC mains can provide effective AGC action.

The simple AGC circuit shown in Figure 5 was built around the broadband amplifier of Figure 2. The circuit sensed drain current variations and adjusted V_{GS} as the frequency swept from 30 to 90 MHz. The resulting power output was leveled to within ±0.1 dB as shown in Figure 6.

One precautionary note is that this AGC circuit senses the voltage developed across a 0.1 ohm resistor. In a laboratory environment one must guard that hook-up leads to and from the power supplies do not contribute to this voltage drop. Otherwise the AGC circuit will hopelessly try compensating for these losses.

Conclusions

AGC without RF sampling has been demonstrated to be effective when using VMOS in power amplifier design. Low-level gate modulation would be a natural outgrowth of this concept.

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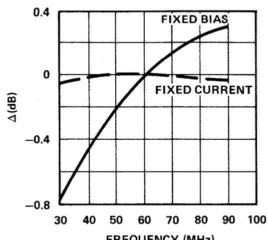
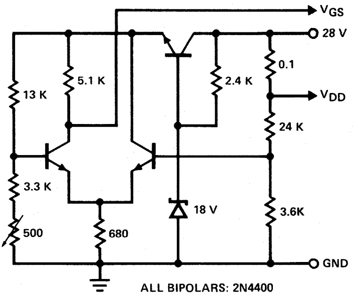
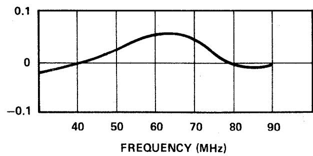


Fixed Bias and Fixed Current Power Output vs Frequency
Figure 4



Simple AGC Circuit
Figure 5



AGC-Controlled Power Output
Figure 6

MOSPOWER

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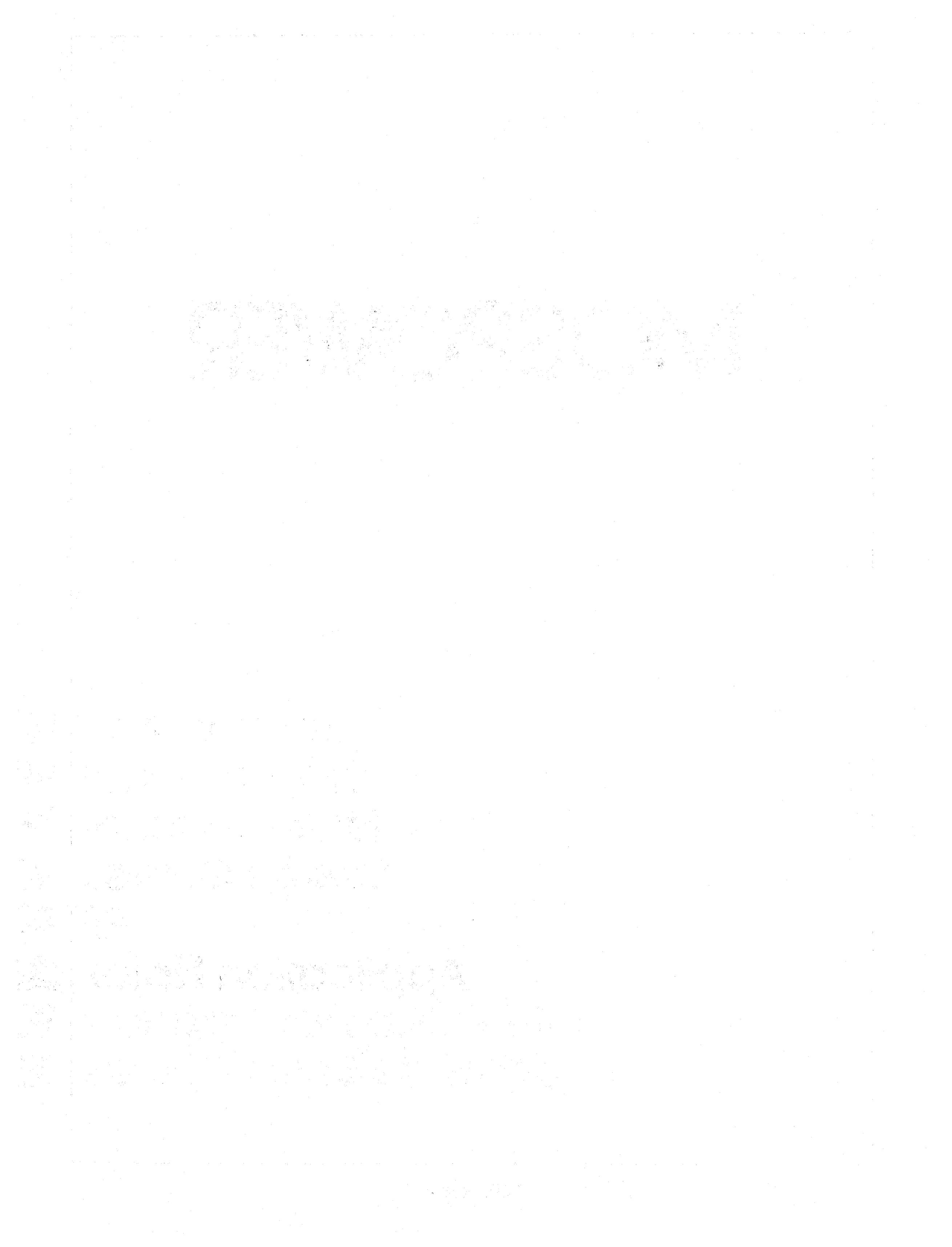


What is MOSPOWER?

Ed Oxner

What is MOSPOWER?

Vertical Metal-Oxide-Semiconductor Field-Effect Transistors uniquely combine the advantages of the power bipolar transistor with those of the MOSFET. The result is a high-power, high-voltage, high-gain power transistor with no minority-carrier storage time, no thermal runaway and a greatly inhibited secondary breakdown characteristic, all of which are contributing to the spectacular rise in the popularity of the MOSPOWER FET.

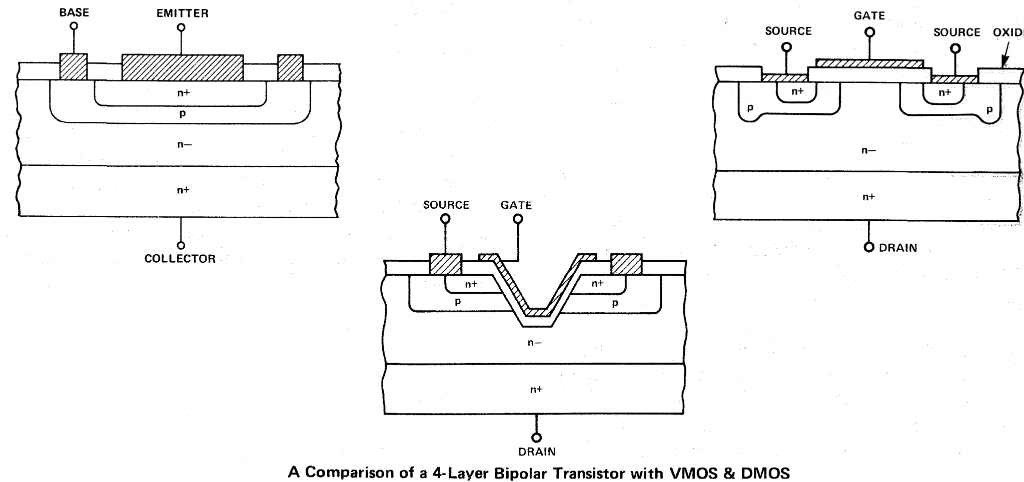
Construction of the MOSPOWER FET

Within the MOSPOWER FET family there are two basic topologies: a low-voltage V-groove structure, commonly called VMOS, and a high-voltage double-diffused planar structure called DMOS. In their initial stage of fabrication both closely resemble the double-diffused epitaxial power transistor with an n^+ substrate followed by an n^- epitaxial into which is first diffused a *p* and then an n^+ layer forming a 4-layer structure.

One distinguishing feature of VMOS, as shown in Figure 1, is the anistropically-etched V-groove cut normal to the surface that extends through both the n^+, *p* and penetrates slightly the n^- epitaxial region. By virtue of this V-groove easy access is provided for the gate to overlay the *p*-diffusion which acts as the current conducting channel.

DMOS resembles planar topology even though the drain current path penetrates through the n^- epitaxy and the n^+ substrate to the backside contact. The current path through the *p* diffusion channel is established exactly as it is for the VMOS structure. A positive gate potential (for an *n*-channel MOSPOWER FET) inverts the *p*-channel and the resulting electron-enhanced *n*-channel, extending from the n^+ source to the n^- epi, offers an uninterrupted, low resistance current path devoid of the thermal properties associated with the typical bipolar transistor.

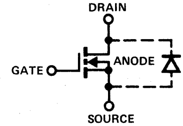
Another distinguishing feature is the electrical bonding of the uppermost n^+ diffusion (source) to the p diffusion (body). In the bipolar model this would tie the base to the emitter; for the MOS model it ties the source to the body. Without this electrical bond there would exist a parasitic 4-layer npn bipolar in parallel with the MOSPOWER FET thus masking the beneficial features with the problems encountered with bipolar transistors. However, with this electrical bond, a source-drain parasitic diode appears in parallel with the MOSPOWER FET.



A Comparison of a 4-Layer Bipolar Transistor with VMOS & DMOS
Figure 1

The "Beneficial" Parasite — The Body-Drain Diode

All power MOSFETs, irrespective of topology (or tradename) have a body-drain *pn* junction that appears in shunt with the channel as shown schematically in Fig. 2. Fortunately, by virtue of the polarity of this parasitic diode, performance is virtually unaffected under normal operation. This parasitic is of mixed blessing; on the one hand, a parasitic element is undesirable from an aesthetic viewpoint, but practically speaking, a reverse polarity diode intrinsic to the FET structure becomes a useful snubbing diode when the power FETs are arranged in a totem-pole configuration such as in motor control applications. If, however, the power FETs are to be used as low resistance analog switch gates then care must be taken to arrange their polarity to achieve high OFF isolation, as shown in Fig. 3. For detailed application information the reader is encouraged to review Application Note AN77-2 "Don't Trade Off Analog Switch Specs."



Schematic Representation of VMOS Showing Body-Drain Diode
Figure 2

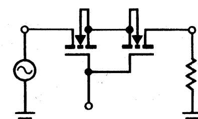


Figure 3

The vertical MOS structure, like the power bipolar transistor, offers a large surface area for source metal and the entire backside of the chip for the drain. This is of great importance as it allows maximum current carrying capacity unavailable to a nonvertical structure.

Early in the history of power MOSFETs some indecision existed relative to the need of static gate protection and for a short time lower power MOSFETs were found with zener gate protection. Although highly recommended for small-signal MOSFETs, power MOSFETs with substantial gate-to-source capacity do not need alternative means for static protection.

The absence of the zener offers considerable freedom. Where before, with the zener-protected gate, the user was cautioned never to allow the gate polarity to reverse (swing negative for an *n*-channel MOSFET), now without the zener the gate is free to swing as far as its breakdown rating in either polarity.

Controlling the MOSPOWER Transistor

Operationally, MOS is unique among power transistors. Channel conduction is proportional to gate *voltage, not* to any sort of injection current, typical of the bipolar transistor. Whatever input current that does exist beyond that attributed to leakage may be identified as the charging current necessary to overcome the input capacitance in very high-speed switching situations. Because the steady-state gate current is negligible, the familiar parameter, *Beta*, is of little importance. Consequently, MOS exhibits a high input resistance that makes it ideal for many logic control applications.

Gate-Source Breakdown

Some confusion exists with respect to the maximum allowable gate-to-source voltage a power MOSFET can safely handle. *It is seldom equal to the absolute maximum drain-gate voltage.*

Several operating parameters of the power FET—among them the gate control voltage—depend upon the oxide thickness that separates the gate from the bulk semiconductor: the MOSFET structure itself. To achieve control with reasonable voltages the gate to source voltage—predicated by the oxide thickness—is limited to $\pm 30V$.

This means that if the power FET is perched atop a high-voltage rail, such as the uppermost device in a totem-pole configuration, you must be careful to keep the gate voltage within the safe limits with respect to the *source of the same FET*. This same precaution also applies for some source-follower applications and for many gating applications especially when the source is riding on a rail voltage in excess of 30V.

There are a variety of procedures for driving a power MOSFET sitting high above the safe operating voltage limits and the reader is encouraged to review Application Notes AN79-4, "Driving the MOSPOWER FET," AN80-1, "MOSPOWER FETs—A Key to the Advancement of SMPS Technology."

MOS as a Switch: Turning it ON

Driving MOS from logic requires an appreciation of the gate drive power needed to actuate, or turn *on*, the MOS power transistor. First, the driver must be able to deliver sufficient current during the transition (from *off* to *on*) to adequately charge the input capacitor in the desired time. Two familiar equations show that to achieve a high speed switch driving the gate from a low impedance, high current source is certainly desirable.

$$t = 2.2\ R_g \cdot C_{in}$$

$$i = C_{in}\ dV/dT$$

where R_g = input resistance
C_{in} = input capacity
dV/dT = rate of voltage change

As this driving voltage ramps upward another phenomenon occurs called *Miller effect*. Once the threshold voltage of the MOS transistor is passed it begins to draw increasingly heavier drain current. In Figure 4 the rapid use of drain current with respect to the gate voltage is clearly illustrated. As the drain current rises, the transconductance rises rapidly to saturation as shown in Figure 5. Concurrent with this rise in transconductance is a proportional rise in gain and the once low feedback capacitance now swells to enormous proportions appearing as an addition to the input capacitance.

$$C_{in} = C_{iss} + (1 + A_V)C_{gd}$$

where C_{iss} = common-source input capacitance
C_{gd} = gate-drain capacity
A_V = voltage gain

If the driver is deficient in its reserve of drive current the MOS transistor's switching speed suffers and the waveform shown in Figure 6 is the inevitable result. On the other hand, if the driver can deliver the required charging current the switching speed is determined solely by just how fast the driver *can* deliver.

Turning the Switch OFF

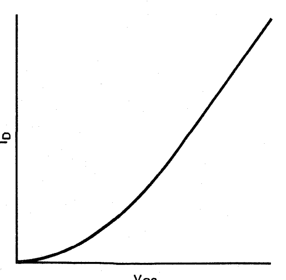
Turn off is another story where the MOS power transistor outperforms its equivalently-rated power bipolar transistor. MOS, a majority-carrier transistor begins to turn off immediately upon the removal of gate voltage. Again the speed is limited by the rate of discharge of the input capacitor through the driver. For ultra-high speed switching special charge transfer circuits are recommended for dumping current both into and out of the MOS gate. Upon the removal of the gate voltage the MOSPOWER FET 'shuts down' (a fail-safe feature?), the resistance between drain and source rises to a very high value and whatever current flow that remains is limited to leakage. This, of course, precludes that the breakdown voltage is not reached.

The Characteristics of MOS

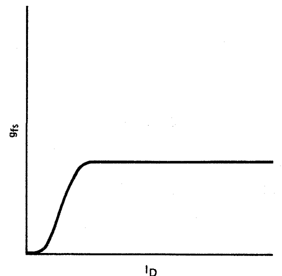
Closer examination of Figure 1 reveals that MOS, unlike the conventional low power MOSFET, has a very short channel where, as the drain-source current flow increases, electron velocity saturation results. The consequences resulting from this velocity saturation are three-fold: the output characteristics assume a constant-current plateau, the forward transconductance saturates and, most important, a linear transfer characteristic results. All of these effects are shown collectively in Figures 4, 5 and 7.

The Importance of Threshold Voltage

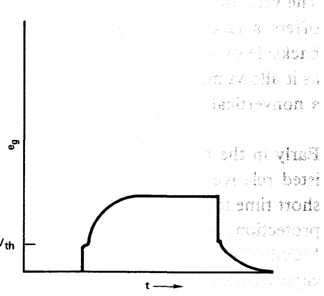
As an enhancement-mode MOSFET, we see what appears as a delayed turn-on when a voltage ramp is applied to the gate. This apparent delay is, in reality, caused by the threshold voltage level, below which the channel remains nonconducting and above which drain current begins. A logic-compatible MOS is one whose threshold voltage is set so that in the low state [0] the MOS is *off* and in the high state [1] the MOS is *on*. It is important to note that a low threshold voltage is undesirable for high power MOS devices for a number of reasons. High power MOS transistors generally operate at higher chip temperatures for optimum efficiency. Since threshold is temperature dependent (a coefficient of approximately −5 mV/°C) a high threshold is mandated to assure operation in the enhancement region. Furthermore, high-power devices have large input capacitance which necessitates a substantial drive. The wisdom of a high threshold precludes the possibility of driver noise causing false triggering of the MOS. This noise immunity is especially important when working in switching power supplies and motor control applications.



Transfer Characteristics of VMOS Showing Linear I_D/V_{GS} Relationship
Figure 4



Transconductance vs Drain Current
Figure 5



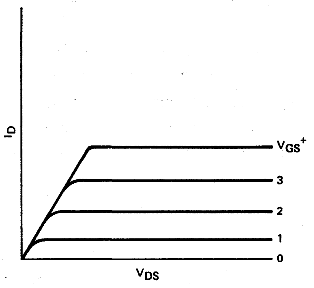
Effect in Input Waveform When Miller Effect Loads Driver Excessively
Figure 6

Temperature Effects of MOS

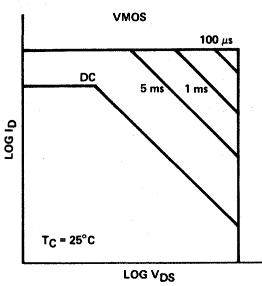
The negative temperature coefficient of gain characteristic of FETs is certainly a valuable asset when using MOS in linear applications, for it greatly simplifies the biasing circuitry. As a bulk semiconductor the resistance of the silicon exhibits a positive temperature coefficient of 0.6%/°C.

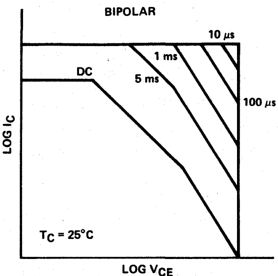
The benefits from this unique thermal property are twofold. MOS offers an exceptionally stable SOA *(safe operating area)* in comparison to equivalently-rated power bipolar transistors as shown in Figure 8. Secondly, paralleling MOS for increased current handling presents no problem. Any intrinsic unbalance between MOS transistors does not result in current hogging because the negative temperature characteristic acts to equalize the current flow.

Always be careful to keep MOS power transistors within their operating temperature limits. If heat sinks are advisable, use them.



Output Characteristics of VMOS
Figure 7





Typical Safe Operating Area
Comparison Between MOS and Bipolar
Figure 8

Siliconix

Application Note AN79-6

Using Power MOSFET Transistors to Interface from IC Logic to High Power Loads

VMOS transistors are an ideal element to interface power loads to integrated circuit logic. Although circuit design is simple, there are a few rules and precautions to observe in order to minimize power dissipation and to have reliable operation, which are not obvious at first glance.

Topics considered are (1) the nature of the load, (2) general driving requirements of VMOS, and (3) the output characteristics of the logic element.

LOAD CONSIDERATIONS

Freedom from second breakdown limitations makes driving highly inductive or capacitive loads a natural application for VMOS. Inductive loads include transformers, solenoids or relays. High current inrush loads such as incandescent lamps, pulse forming networks, and motors also are generally handled easily. Some attention must be given to the load characteristics, however.

In common with bipolar semiconductor devices, VMOS transistors can be damaged if their voltage ratings are exceeded. Although their avalanche energy capability is much better than that of bipolar transistors, it is not good design practice to have the VMOS absorb inductive energy unless the part is rated for this type of service. The spikes generated from inductive loads may have tremendous energy content and usually some means of limiting their amplitude must be provided.

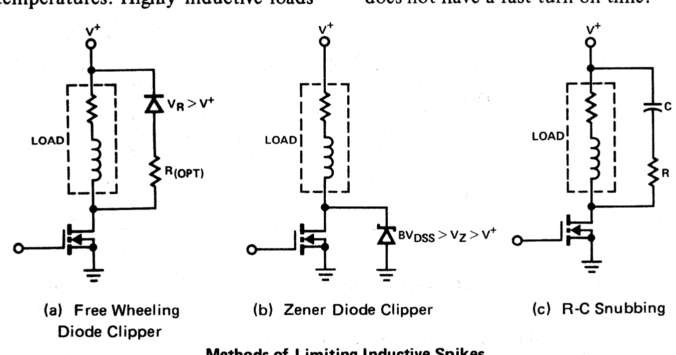
In addition the transient power generated during the turn-on and turn-off intervals must be determined in order to check for excessive channel temperatures. Highly inductive loads may generate significant power on turn-off, whereas capacitive-like loads cause power surges on turn-on. The power waveform should be obtained, a suitable rectangular model derived, and peak junction temperature computed using techniques discussed elsewhere[1,2]. This calculation is especially important for incandescent lamp and motor loads as their current surges last from tens to thousands of milliseconds which causes a significant surge in the temperature of the VMOS power driver.

Inductive Loads

Usually with inductive loads the peak voltage spike should be limited to a value below the breakdown rating of the transistor. Three techniques are commonly employed: free-wheeling diodes, peak clipping and snubbing. Typical circuits are shown in Figure 1.

The spikes caused by most electromechanical inductive loads such as solenoids or relays are effectively handled by the free-wheeling diode in part (a). The low impedance of the diode usually causes the current to have a long decay time, however, which may be intolerable in some applications. Speed may be traded for overshoot voltage, by using a resistance, R, in series with the diode[3].

The free-wheeling diode may be an inexpensive rectifier such as the 1N4002. However, junction rectifiers do exhibit a turn-on transient which may allow excessive overshoot if the VMOS transistor is being driven off rapidly. For high speed switching, a Schottky or low voltage ion-implant rectifier is required; the ordinary fast recovery rectifier does not have a fast turn-on time.



(a) Free Wheeling Diode Clipper (b) Zener Diode Clipper (c) R-C Snubbing

Methods of Limiting Inductive Spikes
Figure 1

Often the safest and least expensive limiting technique is to use a zener diode as shown in part (b). The zener responds in picoseconds and can protect the VMOS from supply transients as well as the inductive spike; consequently, zener limiting is particularly attractive on raw power buses. In a manner similar to using a resistor in series with a free-wheeling diode, faster decay of load current is achieved by clipping at a level above the supply voltage.

The R-C snubber is commonly used in power conversion circuits to limit spikes caused by transformer leakage inductance and wiring inductance. It also reduces power dissipation by shaping the load line to appear more resistive. Resistor R, in series with the capacitor, is required to limit the current surge on turn-on (a good idea even when VMOS is used) and to insure that the circuit is adequately damped. Since the circuit is basically a resonant tank, it will exhibit a damped oscillation unless the circuit Q is 1/2 or less. Values are usually empirically determined. The peak voltage across the network will not exceed that calculated using the energy relationship: $1/2\ LI^2 = 1/2\ CV^2$. Solving for the voltage, it is found that

$$V = I\sqrt{L/C}$$

The resonant frequency can be calculated from the usual relationship and R selected so that $Q \simeq 1/2$ by using

$$R = 4\pi fL$$

The equations and experience indicate that larger values of C lower the peak voltage and resonant frequency and consequently the resistor R also must be reduced. An optimum value exists for a given L-C combination which results in minimum overshoot. Another consideration is to minimize the power dissipation in the transistor; various techniques are discussed elsewhere(4,5).

Capacitive and High Inrush Loads

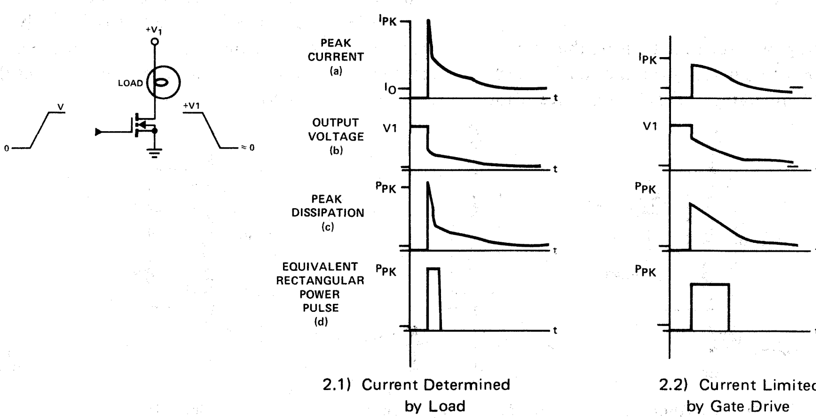
Usually no auxiliary circuitry is required with capacitive-like loads. Although VMOS has no failure mode akin to secondary breakdown, it is necessary to observe the safe area curves of the VMOS transistor in order to avoid excessive temperature excursion during current inrush. When inrush power is excessive, usually increasing the gate drive will reduce it and may hold it within bounds. A lamp circuit and waveforms are shown in Figure 2.

Figure 2.1 illustrates the typical transient current, voltage and transistor dissipation of an incandescent lamp load being driven by a VMOS circuit that is not drive limited – it can supply all the current that the load demands while maintaining operation in the ohmic region. Under these conditions, the output voltage quickly swings from its off state (V_1) to on state in a time dictated by the transient gate drive current and the VMOS capacitances. The peak current is a function of the lamp's cold resistance and decays quasi-exponentially as the lamp filament heats and resistance increases.

The transistor dissipation waveform is similar to the power waveform of Figure 2.1(c); this can be equated to the rectangular power pulse of 2.1(d) to simplify peak and average power calculations.

The case where the power transistor is drive limited (where it cannot supply all of the peak current that the load demands) usually – but not always – results in greater transistor dissipation. This is illustrated in the transient waveforms of Figure 2.2 where the peak current is much less than in the previous example, but also where transistor operation does not enter the ohmic region initially during the switching transition. The resulting power dissipation pulse is greater and may be destructive.

VMOS transistors make ideal drivers for incandescent lamps because they can handle high current surges without failure caused by secondary breakdown. Lamp drivers may need to handle two types of surges, cold resistance inrush and flashover.



Waveforms When Driving an Incandescent Lamp, High Inrush Loads Develop Similar Waveforms
Figure 2

Cold resistance inrush occurs on all lamps during turn-on; the peak is between 12 and 18 times the steady state current. Furthermore, the inrush current may be from 2 to 5 times rated current 5 milliseconds after power application. The inrush depends somewhat upon the lamp's design and the cold temperature of the bulb, which in turn is dependent upon the lamp's operating duty cycle and ambient temperature. Since the turn-on surge is a repetitive transient, for maximum VMOS reliability, it is usually desirable to have sufficient gate drive to place the operating point in the ohmic region during the surge in order to minimize VMOS power dissipation.

The flashover surge occurs during failure of a gas-filled lamp. (All lamps over 60 watts designed for 120 or higher voltage lines contain some gas for improved efficiency and life). As the filament burns out, an arc is developed causing an extremely high surge on the order of 80 to 200 amperes with a baseline of 2 to 4 milliseconds. Coping with this surge is a real problem for the circuit designer when bipolar devices, such as junction transistors or thyristors, are used. If a device rated adequately for the steady state and inrush current is used, the flashover surge will cause failure. If a device rated to handle the flashover is used, cost is usually out of bounds because the device ratings far exceed those required for normal use. Semiconductor fuses can be used, but these are quite expensive. With VMOS power devices, the flashover surge will not cause failure even though the junction temperature may momentarily exceed its rating.

Driving Grounded Loads

In many cases, the load is connected to ground and cannot be arranged as shown in Figures 1 and 2. Driving a grounded load forces the VMOS to be used in a source follower circuit. The difficulty with a follower is that, to keep the VMOS in the ohmic region with a large drain current flow, the gate must be about 10 volts above the source potential, which is only slightly lower than the supply. Therefore, the gate drive voltage must come from a voltage source which is about 10 volts above the supply voltage. If such a voltage is available, no significant problem exists other than insuring that the driver circuit has a sufficient voltage rating. When no fixed voltage source is available, it may be generated using the bootstrap technique.

A bootstrap circuit is shown in Figure 3. Operation is as follows: when the driver bipolar is on, the gate potential is near ground and the VMOS is off. Capacitor C is charged to V_{DD} through the load and diode D_1. When the driver goes off, the gate voltage rises, turning on the VMOS transistor which raises the source potential. If C is many times larger than the input capacitance of the VMOS, it acts as a voltage source in series with the VMOS source terminal potential, thereby providing a gate-source voltage close in value to V_{DD}. The capacitor C will lose charge with time through the reverse resistance of diode D_1, so that it becomes impractically large if the load must be held on more than a few seconds, unless a strobing technique is used as discussed in the following paragraph. However, many loads, such as hammer drivers in high speed printers, are actuated for under a millisecond so that capacitors in the range of 0.1 μF are adequate. In cases when the load is a solenoid, it may be permissible for the VMOS to come out of the ohmic region as a result of a partial loss of gate drive after the solenoid has pulled in, because the hold-in current is very low. However, the power dissipation of the VMOS may increase significantly unless the drop in gate drive reduces drain current to a rather low value.

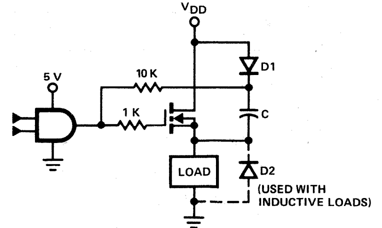
When the load must remain actuated at full power for a long period of time, a pulsed signal may be applied to the drive circuit instead of a DC level. When load current is to flow, the driver is off, except for occasional brief on periods during which the VMOS source voltage drops to ground allowing C to recharge to V_{DD}. The source for this strobe signal could be a system clock signal or the AC line. The higher the pulse repetition frequency, the smaller C may become, but C should usually be at least ten times the C_{iss} of the VMOS device to avoid transferring more than 10% of the charge on C to the VMOS gate during turn-on.

GENERAL DRIVING CONSIDERATIONS

Regardless of the type of logic or network used to drive a VMOS transistor, consideration must be given to VMOS properties such as:

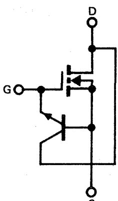
1. The input protection zener diode
2. The high frequency response
3. The capacitive input impedance

The input protection zener diode integral with some devices places restrictions on the drive levels. The positive voltage on the gate with respect to the source should not exceed the maximum voltage rating of the zener diode nor should the zener become forward biased by allowing the gate-to-source voltage to become negative.



Driving Loads Connected to Ground by Using Bootstrapping
Figure 3

The reasons for these restrictions are evident from the circuit of Figure 4 where it is seen that the zener is actually the base-emitter junction of a bipolar transistor whose collector is connected to the drain. Consequently, the zener exhibits a negative resistance characteristic similar to the BV_{CEO} of a transistor. Above a few hundred micro-amperes, the voltage may switch from, for example, 20 volts to 8 volts. The lower voltage will limit the amount of current available from the VMOS transistor and excessive dissipation in the zener and drive circuitry may occur.



A Parasitic npn Transistor in Zener Protected MOSFETS
Figure 4

If the drive circuit can cause a negative gate-source voltage – a common situation with a source follower driving a capacitive load – the bipolar becomes turned on in the forward direction causing a flow of current from the drain terminal to the gate terminal. Damage to the device from excessive current may result if the impedance of the current loop is very low, but this is usually not a problem unless the drain-source voltage is high enough to cause the bipolar to operate in a $BV_{CEO(SUS)}$ mode. Since the BV_{DSS} rating of the FET is essentially the BV_{CBO} rating of the bipolar, $BV_{CEO(SUS)}$ is approximately one half of BV_{DSS}. Consequently, a second breakdown failure of the zener bipolar may occur when the drain-source terminal voltage exceeds one half of BV_{DSS}. If negative gate voltages are unavoidable a VMOS part that does not have an input zener diode should be used.

The carrier transit time through the channel is under 1 ns for most VMOS structures resulting in cut-off frequencies on the order of a gigahertz. Consequently, very fast switching is readily achieved, but parasitic oscillations can be troublesome if certain precautions are not observed.

Usually oscillations are prevented by observing one or more of the following guidelines:

1. Keep lead and trace lengths short.
2. Place ferrite beads on the gate lead close to the gate terminal or use a resistor of 10 to 1000 ohms in series with the gate.
3. Avoid a layout which may couple output signal to the input.
4. Surround the VMOS transistor with a ground plane and shield output from input.

Since VMOS gate input resistance is essentially infinite, many VMOS transistors can be driven from a CMOS or TTL output. However the input impedance of VMOS is capacitive and the drain current essentially follows the voltage on the gate. Although switching speed, per se, is not important when driving a lamp or electromechanical load, the limited transient current available from the logic element may result in switching slow enough to cause significant transient power dissipation, particularly when a number of VMOS stages are being driven in parallel. Accordingly, a transient analysis of some sort is usually required.

A fairly simple, yet quite accurate analysis is to use a charge control approach as described by Evans and Hoffman[6]. For any particular time interval,

$$\Delta t = \frac{(\Delta V_{GS})(C_{in})}{I_G}$$

where

ΔV_{GS} is the gate-source voltage change

C_{in} is the effective input (gate-source) capacitance

I_G is the average gate current during switching

(all values must be determined for the time interval of interest).

Table I shows the appropriate quantities to use in the equation. For completeness, turn-on and turn-off delay relations are included, but these intervals are rarely of interest in power circuits. However, dissipation may be a problem during rise and fall time.

TABLE I. PERTINENT SWITCHING RELATIONSHIPS

Interval	Symbol	Gate Voltage Change	Capacitance
Turn-On Delay	$t_{d(on)}$	$V_{G(TH)} - V_{G(off)}$	C_{iss}
Rise Time	t_r	$V_G @ I_{D1(on)} - V_{G(TH)}$	$C_{iss} + \frac{\Delta V_{DS}}{\Delta V_{GS}} C_{rss}$
Turn-Off Delay	$t_{d(off)}$	$V_{G(on)} - V_G @ I_{D2(on)}$	C_{iss}
Fall Time	t_f	$V_G @ I_{D2(on)} - V_{G(TH)}$	$C_{iss} + \frac{\Delta V_{DS}}{\Delta V_{GS}} C_{rss}$

Capacitance values used are the average values as V_G varies over the ranges shown for the time interval of interest. Appropriate V_{DS} values must also be used to determine the capacitance. Key V_{GS} points are:

- $V_{G(off)}$ = Off state gate voltage prior to turn-on
- $V_{G(TH)}$ = Threshold gate voltage
- V_G @ $I_{D1(on)}$ = V_G corresponding to the peak value of drain current for capacitive or resistive loads or the value of drain current when the drain voltage enters the ohmic region for inductive loads.
- $V_{G(on)}$ = On-state gate voltage prior to turn-off
- V_G @ $I_{D2(on)}$ = V_G corresponding to the value of drain current flowing prior to turn-off.

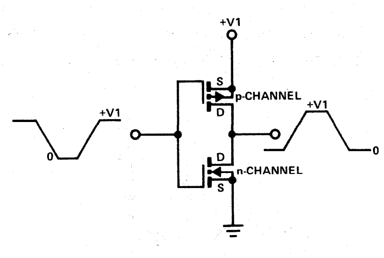
Driving From CMOS Logic

The widely used CMOS logic elements are ideal for direct coupling to VMOS power transistors because CMOS can operate with supplies up to 15 volts, a level which provides ample drive for VMOS. Since VMOS switching speed and transient load handling capability is related to the output impedance of the drive source, a brief examination of the CMOS circuit follows.

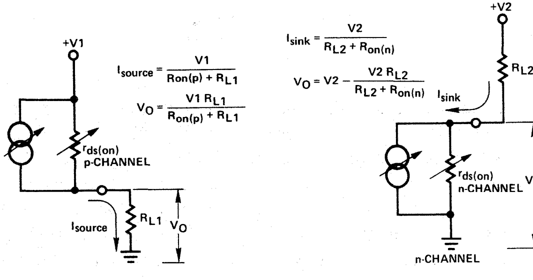
All CMOS circuits usually have an output configuration as shown by the inverter of Figure 5. The inverter consists of a p-channel MOSFET connected in series with an n-channel FET (drain-to-drain) with the gates tied together and driven from a common signal – hence, the name CMOS (complementary MOS). When the input signal goes positive (+V), the p-channel FET is essentially off and conducts only I_{DSS} (picoamperes). The n-channel unit is forward biased but since only I_{DSS} is available from the p-channel, V_{DS} is very low. Conversely, when the input goes low (zero), the p-channel device is turned full on, the n-channel device is off, and the output will be very near +V. Since the current (without a load) is extremely small, the inverter dissipates almost no power in either stable state; the only dissipated power of consequence occurs during the switching transitions as capacitances are charged. Due to the extremely high input impedance of VMOS, the CMOS gate has the capability of interfacing with many VMOS power transistors when only static conditions are considered.

The DC resistance between drain and source when the device is turned on is generally labeled "ON resistance, R_{ON}" or $r_{DS(on)}$. However the CMOS gate has a limited output capability determined by the gain of the n and p-channel devices. Equivalent circuits of the CMOS output are shown in Figure 6.

A look at the characteristic curves of CMOS transistors will provide insight into the dynamic driving source impedance presented to the VMOS gate. Figure 7 shows the characteristic curves of n-channel and p-channel enhancement mode transistors typically found in CMOS circuits. Referring to the curve of V_{GS} = 15 V (gate-to-source voltage) for the n-channel transistor, note that for a constant drive voltage

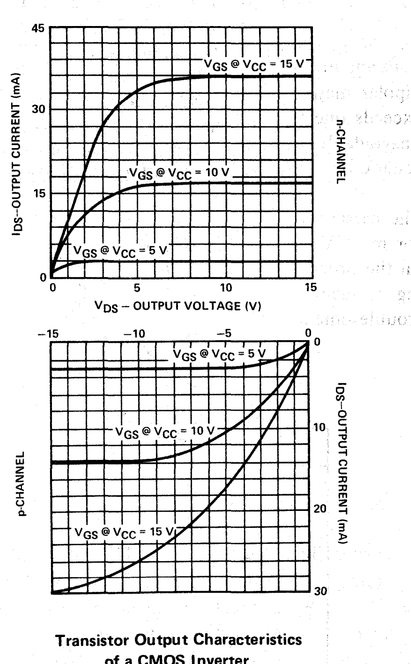


CMOS Inverter
Figure 5



(a) Sourcing Current (b) Sinking Current

CMOS Source/Sink Capabilities
Figure 6

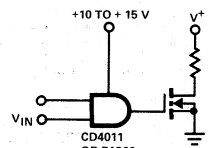


Transistor Output Characteristics of a CMOS Inverter
Figure 7

V_{GS}, the transistor behaves like a current source for drain-to-source voltages greater than $V_{GS} - V_T$ (V_T is the threshold voltage of an MOS transistor – on the order of a volt or two). For a V_{DS} below $V_{GS} - V_T$, the transistor behaves essentially like a resistor. Similar curves are obtained for lower values of V_{GS} except that the magnitude of the current is significantly smaller and, in fact, I_{DS} increases approximately as the square of increasing V_{GS}. The p-channel transistor exhibits similar, but complemented, characteristics with less gain and a more gradual transition from a current source to a resistor.

When driving a capacitive load the initial voltage change across the load will be a ramp due to the current source characteristic, followed by a rounding off due to the resistive characteristic dominating as V_{DS} approaches zero. For fastest turn-on and therefore lower dissipation in the VMOS transistor, the peak output current should be achieved while the CMOS inverter is operating in the constant current mode. To accomplish this, the maximum current from the VMOS is that which corresponds to a V_{GS} that is a few volts below the CMOS supply voltage, V_1. From Figure 7, note that operating the CMOS driver at higher V_{CC} will have a profound effect on VMOS switching speed because the CMOS output current increases roughly as the square of V_{GS} and the voltage where rounding occurs has been pushed to a higher level.

Therefore, the optimum interface from CMOS to VMOS is shown in Figure 8. In this configuration, the turn-on current is supplied from the p-channel FET which has the poorest characteristics of the CMOS pair, but when operating at 15 volts, serious rounding of the VMOS gate waveform can usually be made to occur at a level above that required to handle the load current. The turn-off current is supplied from the n-channel FET; it maintains good drive capability down to the threshold voltage of the VMOS gate which minimizes tailing of the VMOS drain current.

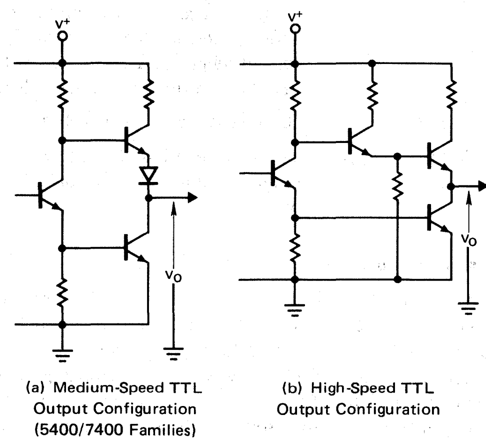


Driving VMOS with a CMOS Gate
Figure 8

Driving from TTL Logic

The lower logic levels used in TTL make it much less satisfactory than CMOS for direct coupling to VMOS; however, TTL can be directly coupled to VMOS when lower output currents are required, or some additional circuitry can be added to make the match more universally applicable. The coupling problems are readily appreciated by analyzing the output circuit of TTL.

Figure 9 shows the totem pole output circuit configurations commonly used in TTL. When the driver is off, the output is high, however, the output is slightly over two diode drops below the supply voltage for either configuration. Since the nominal supply is 5 volts, the output is approximately 3.5 volts, a level too low to fully utilize a VMOS transistor.

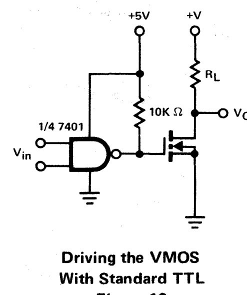


(a) Medium-Speed TTL Output Configuration (5400/7400 Families)

(b) High-Speed TTL Output Configuration

Basic TTL Output Configurations
Figure 9

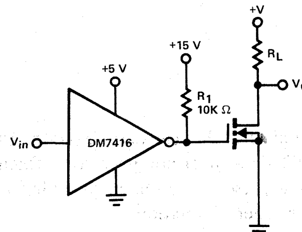
When the driver is on, the lower output transistor is also on; the output is low, on the order of a few tenths of a volt. The low level is satisfactory to ensure VMOS cutoff, in most cases, but the high level needs to be raised.



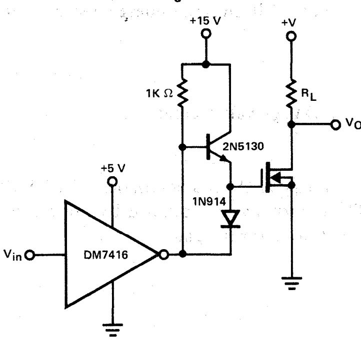
Driving the VMOS With Standard TTL
Figure 10

A method of boosting the TTL output level is shown in Figure 10. The external resistor allows the full supply voltage to be applied to the VMOS gate, but in doing so, the TTL output transistor becomes cut-off as the level increases above 3.5 volts. Consequently the high drive capability and low output impedance of TTL is not effectively utilized, as the drive to the final value of gate voltage must come solely from the pull-up resistor. To maintain a reasonably fast rise time, it is necessary to limit the peak drain current to the value obtained for a particular VMOS type when the gate voltage is at 3.5 volts: the additional 1.5 volts is used as overdrive to place the operating point in the ohmic region.

Full utilization of VMOS transistors is achieved with open collector TTL as shown in Figure 11. The open collector circuits do not have the top transistors and the lower transistors are designed to be used with supplies up to 15 volts. The VMOS rise time is now mainly dependent upon the external resistor used. For fast rise time, the lower resistance values required may cause objectionable dissipation when the TTL output is low; use of the circuit of Figure 12 will provide high speed and low dissipation. It essentially restores the totem pole output to the TTL circuit using an external high voltage transistor. Since the bipolar transistor does not saturate, a general purpose transistor with a high f_T will provide fast drive signal to the VMOS gate.



Open Collector TTL is Used to Provide Greater Enhancement Voltage
Figure 11



A "Totem Pole" Driver Increases Switching Speed and Reduces Dissipation
Figure 12

SUMMARY

VMOS power FETs can easily interface power loads to integrated circuit logic. Spikes from inductive loads usually must be limited to a level below the breakdown voltage of the VMOS transistor. High inrush, capacitive-like loads usually require high gate drive to place operation in the ohmic region during inrush.

To avoid deleterious operation and insure fast switching, consideration must be given to the VMOS input protection zener diode – if present – and capacitive input impedance. Direct coupling to CMOS is usually very satisfactory if the IC supply is 10 to 15 volts. With T^2L, open collector elements are usually required to obtain sufficient gate voltage for the VMOS.

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Siliconix

Application Note AN79-3

Dynamic Input Characteristics of a MOSPOWER FET Switch

INTRODUCTION

The driver-power requirement for a MOSFET switch is a function of how fast we want to turn it ON and OFF.

The DC input resistance of a MOSPOWER FET is in excess of 10^{12} ohms. When used as a switch, the power required to keep it ON or OFF is negligible. However, energy is required to change it from one state to the other. The turn-ON and turn-OFF speeds will determine the input power requirement.

If the FET equivalent input capacitance, C_{in} and the change in V_{gs} are known, the required energy can be estimated:

$$W = 1/2\ C_{in}\ \Delta V_{gs}^2 \text{ watt-seconds} \qquad (1)$$

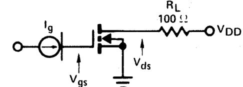
C_{in} is a function of V_{gs} and V_{ds}. During switching it changes during the transition from the ON state to the OFF state. Typically the capacity characteristics specified on the FET data sheet are given for a fixed bias condition. This may present a problem in trying to estimate C_{in} for the above energy equation.

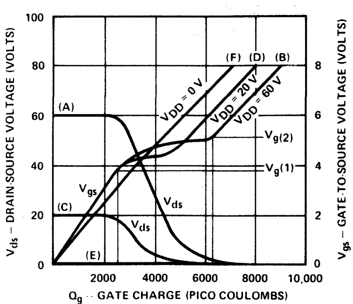
A better method is to determine the gate charge, Q_g, as a function of V_{gs}. The difference in Q_g for the ON state and the OFF state will give the energy required to make the change:

$$W = 1/2\ (\Delta Q_g)\ (\Delta V_{gs}) \text{ watt-seconds} \qquad (2)$$

Figure 1 shows V_{gs} vs Q_g characteristics of a VMOS type VN64GA. These curves were obtained by using a switched, constant-current drive for the gate.

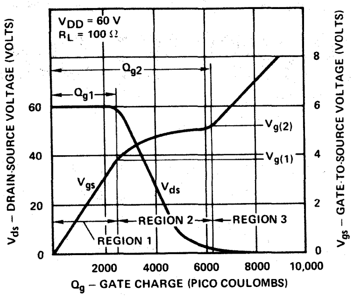
CURVE	V_{DD}	CHARACTERISTIC
A	60 V	V_{ds} vs Q_g
B	60 V	V_{gs} vs Q_g
C	20 V	V_{ds} vs Q_g
D	20 V	V_{gs} vs Q_g
E	0 V	V_{ds} vs Q_g
F	0 V	V_{gs} vs Q_g





VMOS Input (V_{gs}) and Output (V_{ds}) Characteristics
Figure 1

The curves for V_{DD} = 60 volts are reproduced in Figure 2 for further discussion. Three regions are obvious on the input characteristic curve. In region 1 V_{gs} is below threshold and the FET is OFF. In region 2, as V_{gs} exceeds V_{g1}, drain current begins to increase until, at V_{g2}, V_{ds} saturation is reached. In region 3 V_{ds} is saturated and no further change in I_D or V_{ds} occurs.



VMOS Input and Output Characteristics
Figure 2

Capacitance in region 1 is fairly constant as indicated by the constant slope. Its value is approximately:

$$C_{in(1)} = \frac{Q_{g1}}{V_{g1}} \quad (3)$$

$$= \frac{2450 \text{ pC}}{3.8 \text{ V}} = 645 \text{ pF}$$

In region 2, C_{in} increases because the FET begins to turn ON and V_{ds} begins to change, thus increasing the rate of change of V_{gd}. The MILLER EFFECT on C_{gd} causes C_{in} to increase. This effect stops after the device is fully ON and V_{ds} ceases to change. The approximate capacitance in this region is:

$$C_{in(2)} = \frac{Q_{g2} - Q_{g1}}{V_{g2} - V_{g1}} \quad (4)$$

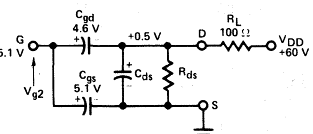
$$= \frac{(6250 - 2450) \text{ pC}}{(5.1 - 3.8) \text{ V}} = 2923 \text{ pF}$$

In region 3 V_{ds} is saturated at a low value and is no longer changing. The FET channel is ON and C_{in} is higher than it is in region 1, but not as high as in region 2. No MILLER EFFECT is occurring. The characteristic shows:

$$C_{in(3)} = \frac{\Delta Q_g}{\Delta V_{gs}} = 875 \text{ pF} \quad (5)$$

$C_{in(1)}$ and $C_{in(3)}$ correspond to C_{iss}, and are approximately equal to C_{gs} + C_{gd}. They differ in magnitude because of the differences in V_{dg} in regions 1 and 3. Figure 3 shows the bias conditions for C_{gs} and C_{gd} at the end of region 1 ($V_{gs} = V_{g1}$) and at the beginning of region 3 ($V_{gs} = V_{g2}$) (we assumed $V_{ds(sat)} \simeq 0.5$ V).

Bias condition at end of region 1

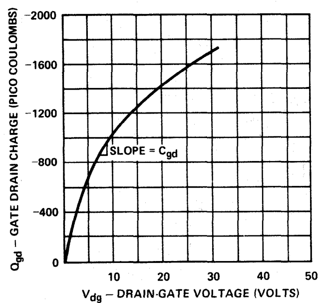


Bias condition at start of region 3

Cgd 4.6 V, +0.5 V, RL 100 Ω, G, D, 5.1 V, VDD +60 V, Vg2, Cgs 5.1 V, Cds, Rds, S

Bias Conditions for C_{gd}, C_{gs} and C_{ds}
Figure 3

There is a large change in the bias on C_{gd}. In region 1 the drain area under the gate is depleted of carriers, thus C_{gd} is greatly reduced. In region 3 the drain region under the gate is flooded with carriers because the device is ON, thus is much greater. Figure 4 shows the characteristic Q_{dg} vs V_{gd} for a typical VN64GA.



Gate-Drain Capacitance Characteristic
Figure 4

The typical C_{iss} given in the VN64GA specification sheet is 640 pF. This agrees with $C_{in(1)}$ estimated above from Figure 3. In both cases the device is OFF and C_{gd} has a large reverse bias.

In region 2, where the FET is in the process of switching, C_{in} is approximately:

$$C_{in(2)} \simeq C_{iss} - A_V C_{rss} \quad (6)$$

Where $A_V = \Delta V_{ds}/\Delta V_{gs}$, and $C_{rss} = C_{gd}$.

For our example, using typical values for C_{iss} and C_{rss} from the data sheet and ΔV_{ds} as indicated in Figure 3, we get:

$$C_{in(2)} = C_{iss} - \frac{\Delta V_{ds}}{\Delta V_g} C_{rss} \quad (7)$$

$$= 640 - \left(\frac{-59.5\ V}{1.3\ V}\right) 50$$

$$= 2928\ pF$$

which agrees with the value estimated with Figure 2 and Equation 4.

A turn-ON delay occurs in region 1 while the gate is being charged up to threshold V_{g1}. Then turn-ON of the FET channel starts and is completed when V_{ds} saturation occurs at V_{g2}.

Overdrive is occuring in region 3. The excess charge in region 3 causes a turn-OFF delay. Turn-ON and turn-OFF delays could be decreased by pre-biasing the gate to a V_{gs} just below V_{g1} and by avoiding overdriving into region 3. This, however, would decrease the switching circuit noise-margin and would require closer control of the gate drive voltage and $V_{gs(th)}$ of the VMOS.

Figure 2 shows that $C_{in(1)}$ and $C_{in(3)}$ are fairly constant. $C_{in(2)}$ increases as V_{ds} decreases because C_{gd} increases. For the purpose of estimating the time of region 2 we can assume the average value given by Equation 4.

If the gate is being driven by a current source, I_g, the times t_1 and t_2 can be determined by:

$$t_1 = \frac{Q_{g1}}{I_g}; \quad t_2 = \frac{Q_{g2}}{I_g} \quad (8)$$

For drivers with a resistive source the times can be estimated by the Equations: (see Appendix for derivation)

$$t_1 = -\frac{Q_1}{V_{g1}} R_{gen}\ \ell n\left(1 - \frac{V_{g1}}{V_{GG}}\right) \quad (9)$$

$$t_2 - t_1 = -\frac{Q_2 - Q_1}{V_{g2} - V_{g1}} R_{gen}\ \ell n\left(1 - \frac{V_{g2} - V_{g1}}{V_{GG} - V_{g1}}\right) \quad (10)$$

where V_{GG} is driver open-circuit voltage and R_{gen} is driver output resistance.

For example, assume a 10 volt driver has an output resistance, R_{gen}, of 10,000 ohms. From the input characteristic curve of Figure 2 we get:

Q_{g1} = 2450 pC,
Q_{g2} = 6250 pC,
V_{g1} = 3.8 volts
V_{g2} = 5.1 volts.

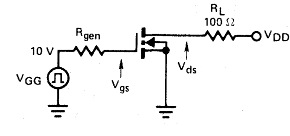
Using Equations 9 and 10 we calculate:

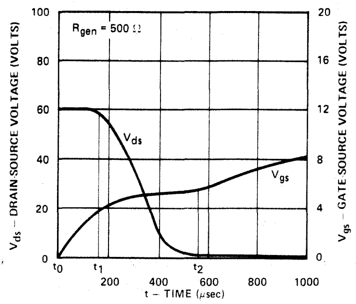
$t_1 = 3.08\ \mu sec$
$t_2 - t_1 = 6.88\ \mu sec$

Turn-ON time (time to drive the VMOS into saturation) is t_2 which is approximately 10 μsec. Reducing R_1 to 500 ohms reduces t_{ON} to approximately 500 nsec. Further reductions in t_{ON} can of course be achieved by reducing R_1 even more.

Turn-OFF times can be calculated in a similar manner. From the ON state V_{gs} starts at V_{GG}. A delay occurs until V_{gs} drops to V_{g2}. Below V_{g2}, V_{ds} begins to come out of saturation, and the FET will be completely OFF when V_{gs} drops below the threshold voltage V_{g1}.

Figure 5 shows input and output characteristics for R_{gen} = 500 ohms. Measured t_1 and t_2 were four to eleven percent higher than the calculated values. Measured and calculated times are shown in Table I.





VMOS Switch Characteristics
Figure 5

TABLE I

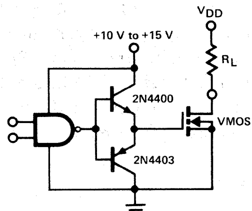
TIME	R_{gen} = 10,000 Ω		R_{gen} = 500 Ω	
	CALCULATED	MEASURED	CALCULATED	MEASURED
t_1	3.08 μsec	3.2 μsec	154 nsec	160 nsec
$t_2 - t_1$	6.88 μsec	7.2 μsec	344 nsec	395 nsec
t_2	9.96 μsec	10.4 μsec	498 nsec	555 nsec

Since gate input-power is needed only during the switching transitions, a driver that has low stand-by power but is capable of supplying high current pulses during switching transitions is desirable if high-speed switching is needed. For the VN64GA as shown in Figure 2, 6250 pC is needed to charge the gate to V_{g2} which drives the output to saturation. Equation 8 shows that to achieve a t_{ON} of 20 nsec:

$$I_g = \frac{6250 \cdot 10^{-12}\ C}{20 \cdot 10^{-9}\ s} = 313\ mA.$$

One solution is to use a MOS clock driver such as the MH0026. These units are designed to deliver high peak currents to capacitive loads and have low standby power.

Another solution is to buffer the logic driver with a complementary emitter-follower as shown in Figure 6.



Driver with Emitter-Follower Buffer
Figure 6

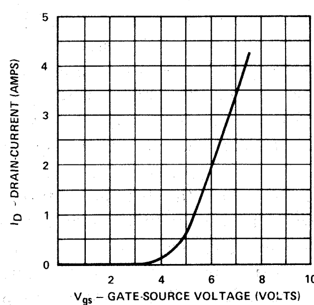
Effect of Drain Load on Q_{g2}

The characteristics presented thus far were with a drain load resistance of 100 ohms. With V_{DD} = 60 volts the maximum I_D = 600 mA.

For different values of $I_{D(max)}$ the required V_{g2} can be obtained from the FET transfer characteristic curve I_D vs V_{gs}. Then with this value of V_{g2}, Q_2 can be estimated from the appropriate V_{DD} curve of Figure 1.

For example, assume a saturated load current of 2 amperes is needed and V_{DD} is 60 volts. The transfer curve of Figure 7 indicates for I_D = 2 amperes that $V_{gs} \simeq 6$ volts. The 60 volt V_{DD} curve of Figure 1 (curve B) shows that Q_g is about 7000 pC.

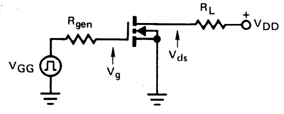
The drain load has practically no effect on Q_{g1} and thus no effect on t_1.



VNG Transfer Characteristic
Figure 7

APPENDIX

In the derivation of Equation 9 and 10 we assumed that $C_{in(1)}$ is constant for $V_{gs} \leqslant V_{g(1)}$ and that $C_{in(2)}$ is constant for $V_{g(1)} \leqslant V_{gs} \leqslant V_{g(2)}$. Figure A1 shows a pulse generator having an open circuit voltage V_{GG} and an output resistance R_{gen}, driving a capacitor C_{in}.



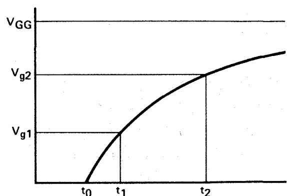


Figure A-1

For a constant C_{in}, V_g as a function of time is:

$$V_g(t) = V_{GG}\left[1 - \exp\left(\frac{-t}{R_{gen}\, C_{in}}\right)\right] \quad \text{(A1)}$$

$$\frac{V_g(t)}{V_{GG}} = \left[1 - \exp\left(\frac{-t}{R_{gen}\, C_{in}}\right)\right] \quad \text{(A2)}$$

Solving Equation A2 for t_1:

$$t_1 = (C_{in(1)}\, R_{gen})\ \ell n\ 1 - \frac{V_{g1}}{V_{GG}} \quad \text{(A3)}$$

The time: $t_2 - t_1$

$$t_2 - t_1 = (C_{in(2)}\, R_{gen})\ \ell n\left(1 - \frac{V_{g2} - V_{g1}}{V_{GG} - V_{g1}}\right) \quad \text{(A4)}$$

In our example from Figure 2

$$C_{in(1)} = \frac{\Delta Q_g}{\Delta V_g} = \frac{Q_{g1}}{V_{g(1)}} \quad \text{(A5)}$$

and

$$C_{in(2)} = \frac{\Delta Q_g}{\Delta V_g} = \frac{Q_{g2} - Q_{g1}}{V_{g(2)} - V_{g(1)}} \quad \text{(A6)}$$

therefore:

$$t_1 - t_0 = \frac{Q_{g1}}{V_{g(1)}}\ R_{gen}\ \ell n\left(1 - \frac{V_{g(1)}}{V_{GG}}\right) \quad \text{(A7)}$$

and

$$t_2 - t_1 = \left[\frac{Q_{g(2)} - Q_{g(1)}}{V_{g(2)} - V_{g(1)}}\right] R_{gen}\ \ell n\left(1 - \frac{V_{g2} - V_{g1}}{V_{GG} - V_{g1}}\right) \quad \text{(A8)}$$

Since C_{in} changes at $V_{g(1)}$ we use this two-step method to determine the total turn-ON time t_2.

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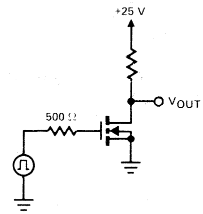
Application Note AN79-4

Driving MOSPOWER FETs

INTRODUCTION

Using VMOS Power FETs you can achieve performance never before possible–if you drive them properly. This article describes circuits and suggests design methods to be used in order to obtain the performance from VMOS that you need.

When designing with VMOS there are some facts that must be kept in mind in order to get optimum results with every circuit. The first fact is that VMOS is a very high frequency device. The cut-off frequency for all VMOS FETs is several hundred megahertz. Most power designers are not used to designing with extremely high frequency devices because with bipolars the frequency response decreases as the power increases. The very high frequency response of VMOS is the basis for many of its advantages but it must be kept in mind while designing. With improper circuit design VMOS can oscillate. This oscillation can be eliminated, though, by exercising two simple precautions. First, minimize lead and trace lengths whenever possible, especially leads associated with the gate of the FET. If it is not possible to have short leads to the gate place a ferrite bead on the gate lead or a small resistor in series with the gate. The ferrite bead or the resistor must be very close to the gate. Second, because of the extremely high input impedance of VMOS (in excess of 10^{12} Ω) drive circuits may be designed which are very high impedance. Under these conditions it is possible for the gate node to get enough positive feedback from the gate-to-drain capacitance or just from stray fields in the circuit to cause oscillation. This must be kept in mind in the design of the circuit.



A Typical VMOS Switching Circuit
Figure 1

When driving VMOS it must be kept in mind that the dynamic input impedance is very different than the static input impedance. The input of a VMOS device is capacitive. The DC input impedance is very high but the AC input impedance varies with frequency. Because of this effect, the rise and fall times of VMOS are dependent on the output impedance of the circuit driving it. The first approximation of the rise or fall time is simply

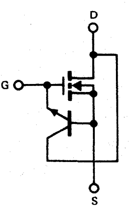
$$t_r \text{ or } t_f = 2.2 \cdot R_{OUT} \cdot C_{iss} \quad (1)$$

where R_{OUT} is the output impedance of the drive circuit. This equation is valid only if the drain load resistance is much larger than R_{OUT}. Knowing this fact, along with the fact that there is no storage or delay time with VMOS, it is very easy to calculate the rise and fall times and set them to any desired value. For example, if you wanted to calculate the 10% to 90% rise or fall time for the circuit shown in Figure 1 using Equation 1 the rise time is equal to:

$$t_r = (2.2)(500)(50 \times 10^{-12}) = 55 \text{ nsec}$$

The dynamic input characteristics of VMOS are covered very thoroughly in Siliconix' application note AN79-3.[1]

A last thing to remember when you are driving VMOS is the input protection zener diode. When putting a positive voltage on the gate with respect to the source, the maximum voltage rating of the zener diode should not be exceeded. It is more important, however, that you do not forward bias the zener diode by putting a negative voltage on the gate while the VMOS is operating in a circuit. The reason for this is most easily explained by referring to Figure 2. As can be seen in the figure, the zener diode is actually the base-emitter junction of a bipolar transistor. If a negative voltage greater than 0.6 V is placed on the gate, the base-emitter junction of the bipolar will be forward biased which will turn on the bipolar transistor. When the bipolar is turned on, current will flow from the drain through the bipolar and out the gate. This operating condition is very likely to be destructive. If negative voltages must be placed on the gate it is recommended that you use a VMOS part that does not have an input zener diode. Non-zenered equivalents are available for most of Siliconix' zenered devices.



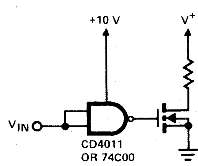
A Parasitic NPN Transistor in Zener Protected MOSFETS
Figure 2

Of all operating modes the common-source configuration is the simplest to drive. Because of the high input impedance of VMOS it can be driven directly from many logic families. When driving from a CMOS gate as shown in Figure 3, rise and fall times of about 60 nsec can be expected due to the limited source and sink currents available from the CMOS gate.[2] If faster rise and fall times are required there are several ways to obtain them. One easy way is if there are extra gates in the package that is driving the VMOS simply put the extra gates in parallel with the gate already being used. The additional current available will cut down the rise and fall times. If no extra gates are available an emitter-follower buffer can be used as shown in Figure 4. With this circuit the current available to the VMOS will be the output current of the CMOS multiplied by the beta of the bipolars. Because the bipolars are operating as emitter-followers there will still be no storage time to worry about and the frequency limit will be determined by either the CMOS gate or the f_T of the bipolars, whichever comes first.

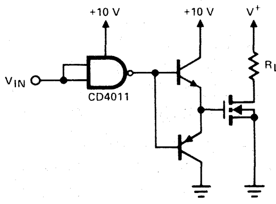
VMOS can also be driven directly from TTL gates. Because the output voltage of TTL is limited, the output current of the VMOS will be limited to some value less than its maximum rated current. The output current that can be expected can be determined from the transfer characteristic of the device being used. For example, if a TTL gate is driving VN46AF the minimum output current of the VMOS will be approximately 250 mA. This value was obtained by using the minimum output voltage of the TTL gate (3.2 V) for a high level output and referring to the transfer characteristic for the VNAZ which is the VMOS geometry used in the VN46AF. If more than 250 mA is required the output of a standard VMOS gate can be pulled up to the 5 V rail as shown in Figure 5. With a full 5 V on the gate the VN46AF will typically sink 600 mA.

For very high speeds a capacitive driver such as the MH0026 can be used as shown in Figure 6. With this drive configuration typical rise and fall times are less than 10 nsec.

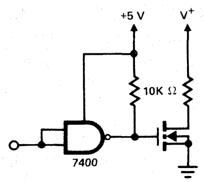
When operated in the common-drain mode VMOS is somewhat more difficult to drive than when in the common-source mode. Because of VMOS' high input impedance, though, it is considerably easier to drive common-drain than a bipolar would be when operated common collector. Common-drain circuits can be used when the load needs to be connected to ground, when an active pull-up and pull-down is required (totem pole circuit), or in bridge type circuits. For the purpose of this discussion all examples will be shown with totem pole circuits.



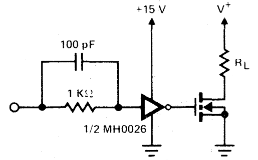
Driving VMOS with a CMOS Gate
Figure 3



An Emitter-Follower Circuit Will Decrease VMOS Rise and Fall Times
Figure 4

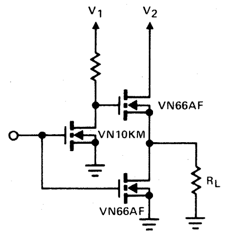


Pulling Up a TTL Output Will Increase the Sink Current of the VMOS
Figure 5



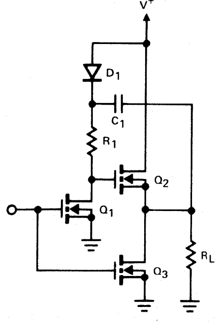
Using an MOS Clock Driver to Drive VMOS
Figure 6

The difficulty with common-drain circuits occurs because as the voltage across the load increases the enhancement voltage of the common-drain device decreases. Referring to Figure 7, as the voltage across R_L approaches V_2 the enhancement voltage for the upper VN66AF decreases. If V_1 is not greater than V_2 then the voltage across R_L can never reach V_2. For this reason whenever a common-drain circuit is used it is always necessary to have or to generate a voltage that is greater than the voltage which is desired to be impressed across the load. The amount the voltage has to be above the desired drain voltage is dependent upon the current the VMOS must source and can be determined from the transfer characteristic of the VMOS being used. If no supply voltage is available other than the one the load is to be pulled up to, one can be generated. This can be done very easily because of the very low drive current requirements of the VMOS.



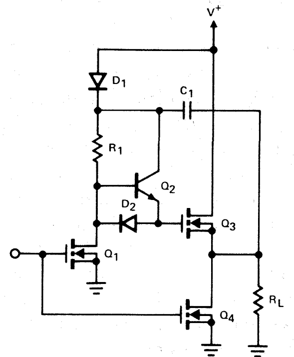
VMOS in Totem-Pole Configuration
Figure 7

One way of generating the required gate voltage is the bootstrap circuit shown in Figure 8. In the circuit, when Q_1 and Q_3 are on, C_1 is charged to the supply rail through D_1. When Q_1 and Q_3 are turned off, the gate voltage on Q_2 goes to the supply rail. As the source of Q_2 begins to pull R_L up, the voltage across C_1 will be maintained, therefore, the gate-to-source voltage of Q_2 will be maintained. The size of C_1 should be large enough so that when it charges the gate capacitance of Q_2 a minimum voltage equal to the required enhancement voltage of Q_2 will be

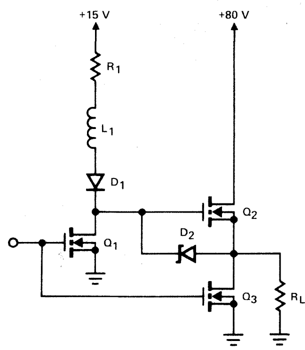


VMOS Bootstrap Circuit
Figure 8

maintained across it. A good rule of thumb is to make C_1 equal to ten times the C_{iss} of the FET. Figure 9 shows the same bootstrap circuit with some added components to improve the rise and fall times. In the circuit Q_2 acts as an emitter-follower to increase the peak gate current to Q_3. D_2 will be forward biased when Q_1 turns on and serves as a low impedance path to discharge the gate of Q_3.



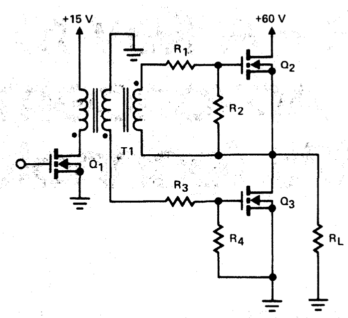
Bootstrap Circuit with Emitter-Follower for Improved Rise Times
Figure 9



Inductive Kickback Drive Circuit
Figure 10

Another method to drive a common-drain VMOS FET is shown in Figure 10. Rather than charging a capacitor and then feeding a signal back from the output as was done in the bootstrap circuit, this circuit stores the required charge in an inductor. When Q_1 is turned off a flyback voltage is generated across the inductor. This voltage is used to maintain an enhancement voltage equal to the voltage of zener diode D_2 across the VMOS FET. Once the Q_2 has been fully turned on and the voltage on R_L is at the rail a negligible amount of energy is required to keep Q_2 on. Q_2 will remain on until Q_1 is turned on, or until the leakage currents of Q_1 and D_2 discharge the gate capacitance of Q_2.

Another method that can be used to drive a common-drain VMOS is transformer drive. A transformer drive circuit is shown in Figure 11. In this circuit the transformer is used in the flyback mode when turning on the upper FET. R_1 and R_3 are used to suppress ringing and R_2 and R_4 are used to assist with turn-off of the FETs. When driving with a transformer, care must be taken to design the transformer so that the secondary inductance in conjunction with the input capacitance of the FET does not create ringing of oscillation problems.



Transformer Drive Circuit for VMOS
Figure 11

SUMMARY

The very high input impedances of VMOS Power FETs greatly simplify the drive requirements as compared to bipolars. The input drive requirements for both common-source and common-drain configurations were discussed in detail. With common-source circuits the requirement that needs to be kept in mind is the rise and fall time required. With common-drain circuits a method of maintaining an adequate enhancement voltage must be considered in addition to required rise and fall time requirements.

REFERENCES

1. A. Evans, D. Hoffman, "Dynamic Input Characteristics of a VMOS Power Switch" AN79-3.
2. D. Hoffman, L. Schaeffer, "VMOS – A Breakthrough in Power MOSFET Technology" AN76-3.

6

Siliconix

Application Note AN80-1

MOSPOWER FETs—A Key to the Advancement of SMPS Technology

In recent years many engineering man hours have been dedicated to refining the switching mode power supply (SMPS). As a result of this effort, significant advances have been made in switching mode power supply technology. At this point there are undoubtedly more advances possible for SMPS using present components.

The major factor affecting size and cost of SMPS is the switching frequency. As the frequency of operation increases, the size of the magnetic components and filter capacitors comes down (cost usually accompanying them). However, power losses in the switching elements go up as a function of operating frequency. Thus further improvements in SMPS technology will come, most probably, in improved switching elements.

The DMOS (or Power MOS) transistor has speed and drive characteristics which will allow a new generation of SMPS designs improving cost, weight and performance factors. This new power control device does not have the secondary breakdown problems of bipolar devices nor the di/dt and dv/dt problem of the SCR.

At this time the great majority of switching power supplies available is restricted to a narrow band of power outputs that is much narrower than the market desires. Very high power switching power supplies are pushing the old semiconductor technology to the limit in performance.

The limitations of the bipolars and SCR's are not the only things in the way of higher power. As power increases the size and cost of transformers, filter capacitors and inductors, and many other of the output components increase very rapidly. One solution to this problem is increasing the operating frequency. Unfortunately, it is very difficult to significantly increase the operating frequency using bipolars or SCR's.

Low power switching supplies present a different type of problem. Excellent low power supplies can be developed using the old bipolar or SCR technologies. The problem is making these small power supplies cost effective. The new switching regulator controller ICs have helped considerably with this problem. The drive and protection circuits for the bipolar output transistors still present a major obstacle to cost effectiveness.

There are two obvious methods to decrease the cost of a low power switcher. The first is to reduce the total number of components and the second is to decrease the cost of the components that are needed. These methods are used in many well designed power supplies, but low power switchers are still not cost effective. Once again, as in high power switchers, raising the operating frequency can be used as a solution. With the reduced size of many of the power supply components made possible by the higher operating frequency, much lower costs are possible.

All of the switching power supply requirements discussed so far, along with the difficulties in achieving these requirements have been known for some time. It becomes apparent after looking at these problems for a while that the major bottleneck impeding the solution to these problems is the power switching device presently being used. DMOS Power FETs were designed with switching power supply designers' problems in mind. The result of this effort is a power transistor with characteristics that are near-perfect for switching power supply use.

In order to take advantage of these new devices, it is necessary to understand a few of their basic characteristics.

The DMOS or Power FET is a *field effect* device whose control element changes the electrostatic field existing over the source-drain channel of the device. This control element or "gate" is insulated from the source-drain channel and has the characteristics of a capacitor.

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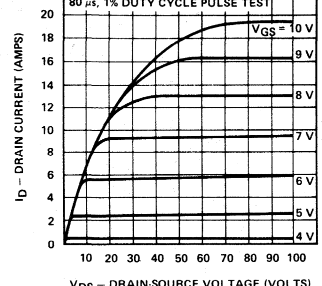
So far, all DMOS devices made are enhancement mode. This means that with zero volts from gate-to-source no current will flow from drain-to-source. If you are accustomed to working with bipolars an easy way to visualize the operation of DMOS is to think of it as a npn bipolar transistor. The only difference is that the collector-to-emitter (drain-to-source) current is controlled by a positive voltage on the gate instead of a current into the base. This first characteristic is a tremendous advantage in high efficiency systems because very little power is required to drive DMOS.

The second characteristic that needs to be understood is the output characteristic curve of the device. This can be best understood by referring to Figure 1. This set of curves actually shows several characteristics which are very important in switching regulators. Each curve in the set is for one gate voltage. As can be seen, there are two distinct regions in each curve. The near vertical portion is called the linear region and the horizontal portion is called the current saturation region. When DMOS is used as a switch it is almost always operated in the linear region. In the linear region the device is fully enhanced and presents the lowest ON resistance and, therefore, the lowest voltage drop. When operating in the linear region, the device looks like a resistor and the drop across the device will be proportional to the current through it. In the saturation region a DMOS FET acts as a constant current source. In this constant current region the drain current is independent of the drain voltage. What makes the DMOS unique is that when operating in the current saturation region, as the junction temperature rises the drain current will decrease. This self protecting feature does not occur in a bipolar. In a bipolar the collector current rises as the junction temperature increases leading to possible runaway and destruction of the device.

The next characteristics of DMOS important to switching power supplies are the very fast rise and fall times. As can be seen in Figure 2, the VN4000A is specified at a maximum of 100 nanoseconds for turn-on and turn-off. It is important to note, however, that these rise and fall times are with a specified driver source impedance. Because of the absence of minority carrier storage time in DMOS FETs the rise and fall times are governed entirely by how quickly the input capacitance can be charged or discharged. The major limiting factor in this charge rate is the source resistance of the DMOS driver. This means that the rise and fall times can be controlled accurately by the user to be as fast or as slow as is desired. By lowering the source impedance driving the VN4000A below the specified data sheet test value (50 Ω), switching times as fast as 10 nanoseconds can easily be obtained.

Another important characteristic of DMOS FETs to be aware of is the threshold voltage. Below the gate threshold voltage a change in the gate-to-source voltage will have no effect on the drain current – it will remain at zero. As the gate-to-source voltage increases above the threshold voltage the drain current begins to increase above zero. With DMOS or with any FET the threshold is controlled by how the device is processed. On the VN4000A the decision was made to keep the threshold in the three to five volt range instead of allowing it to go lower. This higher threshold offers the switching power supply designer major advantages. Because changes in gate-to-source voltage below the threshold voltage do not affect the drain current, for every volt added to the threshold voltage a volt of noise immunity is added. The interior of a switching power supply is a very high noise environment and high noise immunity components offer significant design simplifications along with increased reliability. Turn-off time is also improved with higher thresholds. A DMOS drive circuit has an almost purely capacitive load. On turn-off, therefore, the gate is essentially a capacitor discharged through a resistor to ground. It is clear then that the higher the threshold, the sooner the device will turn-off. Turn-on time is not significantly affected by raising the threshold voltage because of the high gain of the device. The VN4000A offers these high threshold advantages while still maintaining CMOS compatibility.

One last characteristic of DMOS that should be mentioned briefly is the safe operating area. As was mentioned earlier, most designers of high power switchers allow a significant over-design in the ratings of the bipolar power devices used



Output Characteristics of the Siliconix VN4000A Device
Figure 1

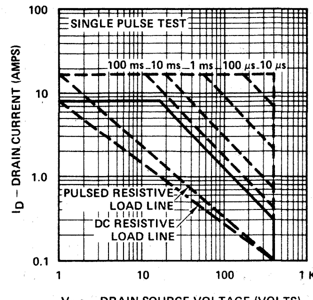
		CHARACTERISTIC	MAX	UNIT	TEST CONDITIONS
1	DYN	t_{on} Turn-ON Time	100	ns	V_{DS} = 35 V, I_D = 8 A, R_L = 4.3 Ω, R_S = 50 Ω
2		t_{off} Turn-OFF Time	100		

Electrical Characteristics of the VN4000A
Figure 2

to allow for irregularities in the safe operating curves caused by second breakdown problems. Figure 3 is the safe operating area curve of the VN4000A, a 400 volt 8 ampere device produced by Siliconix. Superimposed on the SOA curves are resistive load lines for both DC and pulsed loads. A resistive load, however, is not a particularly strenuous test for a switching device—even a bipolar is able to switch a resistive load at the full voltage or current rating. An inductive load is much more difficult. When switching an inductive load the easiest method of protection for the switching device is placing a free wheeling diode across the load. The free wheeling diode alone is usually not adequate for bipolar devices, however, because the diode allows the switching device's voltage to go up to the rail voltage before there is any significant current decrease. This type of operating condition will usually cause second breakdown in a bipolar. As can be seen from the SOA curve the DMOS device can be operated at the full voltage and full current ratings simultaneously. The only derating is for maximum power dissipation. There is no second breakdown.

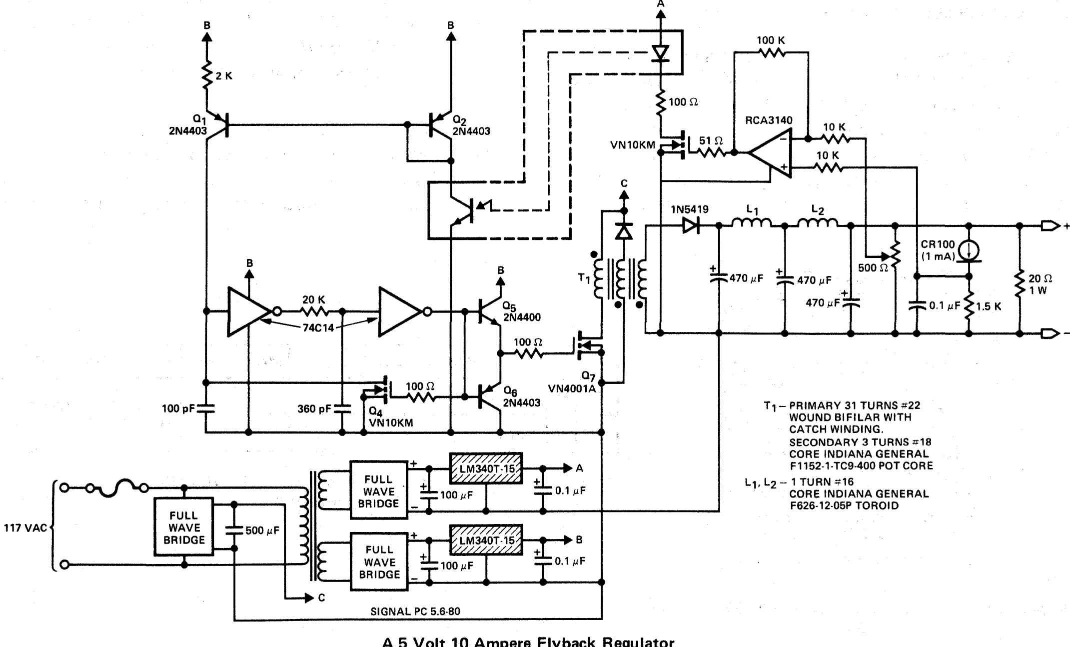
An added advantage of the DMOS device is that there is an inherent diode from drain-to-source in the structure. This diode can be used as the free wheeling diode for currents up to the full current rating of the DMOS device.

Many switching regulators have been built at Siliconix. The first switchers were used as vehicles for gathering information to add to other information obtained from the field on what characteristics were needed for the ideal switching regulator device. Now several switching power supplies have been built simply to demonstrate how easily switching regulators can be designed using DMOS. Three of these regulators will be discussed in the remainder of this article. The first regulator is an example of a very simple, low cost flyback regulator. The second is a half-bridge regulator capable of quite a bit more output power. The half-bridge supply also offers multiple outputs suitable for microprocessor applications. The last switcher is an example of a fairly high power full-bridge design.



Safe Operating Area of the VN4000A Also Showing DC and Pulsed Resistive Load Lines
Figure 3

A schematic for a 5 volt 10 ampere output off-line flyback regulator is shown in Figure 4. The primary goals in this design were simplicity and low cost. Some trade-offs had to be accepted to meet these goals, but overall performance of the supply is still excellent.



A 5 Volt 10 Ampere Flyback Regulator
Figure 4

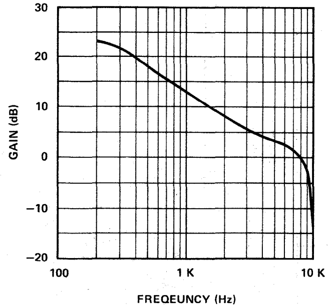
In operation the supply was designed to maintain a constant ON time for the DMOS FET. The operating frequency of the supply is varied to change the duty cycle. ON time for the FET is approximately 7 microseconds and the operating frequency varies from 5 kilohertz to 100 kilohertz. This circuit configuration was chosen because of its ease of implementation and low parts count. There are two disadvantages associated with this circuit. The filter requirements are much more stringent because of the wide range of operating frequencies, and as with all flyback regulators, a larger core than usual must be used because of increased energy storage requirements. These disadvantages are far outweighted by the simplicity offered by this configuration for a low power, low cost switching supply.

In the circuit, two inverters from a hex Schmitt inverter package are used to form a constant ON time variable frequency oscillator. The frequency of the oscillator is controlled by the amount of current flowing from the current mirror consisting of Q_1 and Q_2. The output of the CMOS oscillator is buffered by a pair of emitter followers to drive the DMOS power transistor. The emitter followers create a low output impedance driver to charge and discharge the DMOS gate capacitance rapidly. The output transformer, T2 is an Indiana General pot core with three windings. Because of the high frequency operation of this inverter, care must be taken in the construction of the transformer to avoid excessive leakage inductance. The transformer is wound using fifteen turns of #22 bifilar wire followed by the 3 turn secondary and then sixteen more turns of the bifilar wire. The two wires of the bifilar pair form the primary and the catch windings. By interleaving the secondary in the primary, losses are reduced to a minimum and excellent performance is obtained.

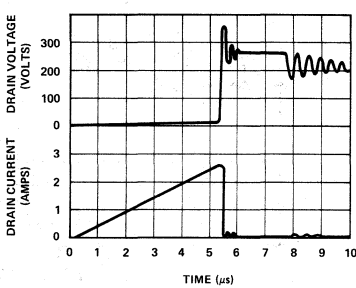
Because the operating frequency of this power supply varies with load, the output filter is more complex than is commonly used. The frequency response obtained from the supply is more than adequate, however. Figure 5 is a plot of the closed loop gain of the supply vs. frequency.

The drain voltage and current waveforms for the output transistor are shown in Figure 6. Switching times are very good and waveforms are close to ideal.

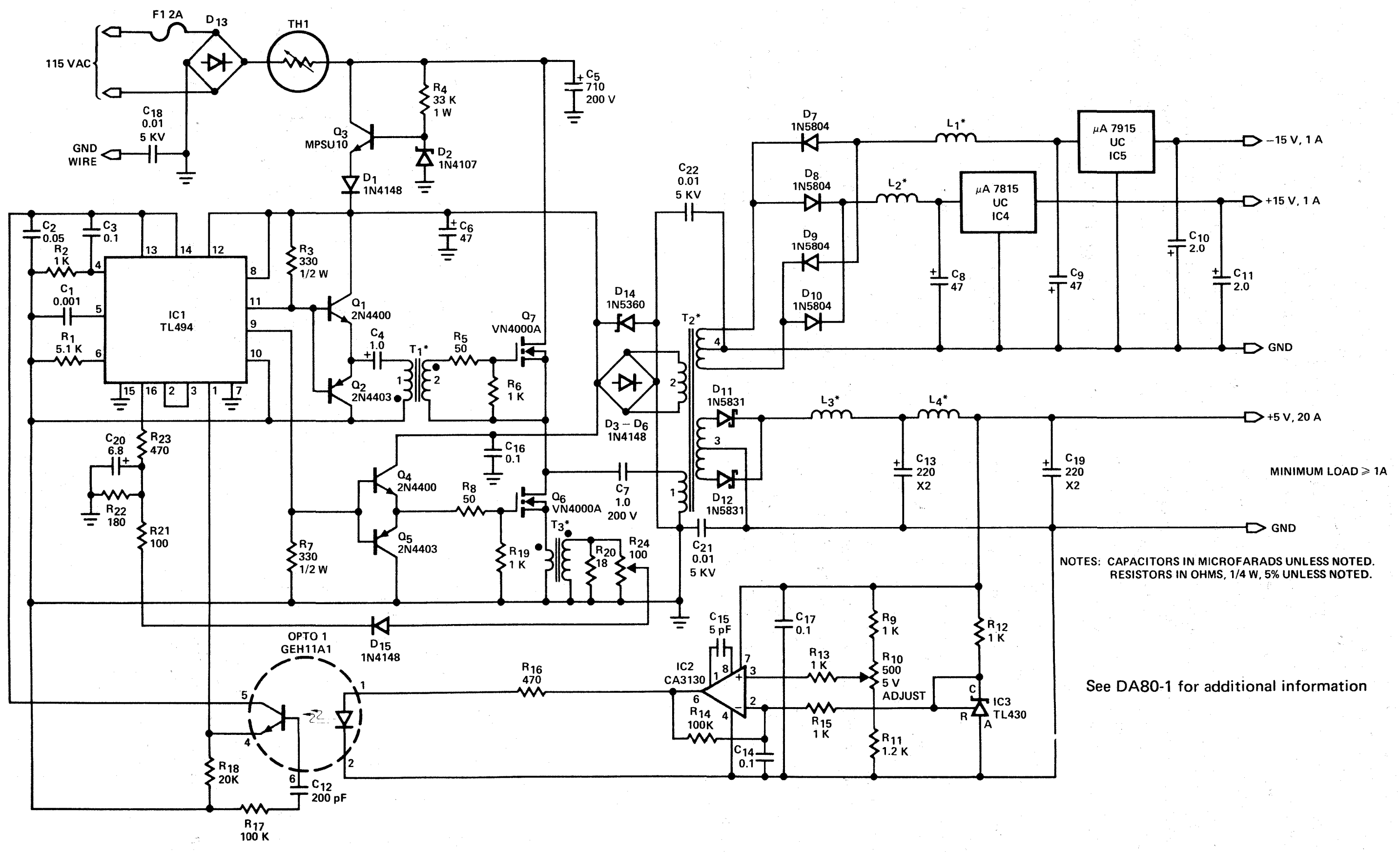
A flyback regulator offers advantages at low power because of its very low parts count. As output powers increase, however, it becomes increasingly difficult to design a practical flyback regulator. There are many alternatives to the flyback regulator that are more practical for higher power designs. Figure 7 is a schematic for a 150 watt half-bridge configuration regulator. This type of design is practical for switchers in the 100 to 500 watt range. The circuit operates at a constant frequency and uses pulse width modulation to control the output voltage. A Texas Instruments TL494 switching regulator controller integrated circuit is used as the main control element.



Closed Loop Frequency Response of the 50 Watt Flyback Regulator
Figure 5



Operating Waveforms of the 50 Watt Flyback Regulator
Figure 6



100 KHz, 150 Watt Half-Bridge Switching Power Supply
Figure 7

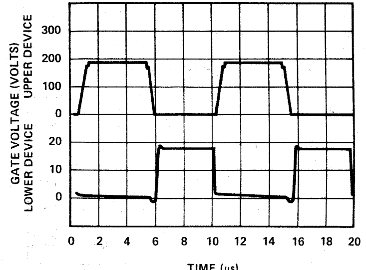
With DMOS, half-bridge and full-bridge circuits are a very attractive alternative to the push-pull configuration often used. In a push-pull circuit the power transistors are exposed to twice the primary voltage. This requires the use of very high voltage, more expensive transistors. This disadvantage is tolerated because at the low operating frequencies required in bipolar regulators, it is difficult to efficiently level shift the signal necessary to drive the upper device in a totem pole. With DMOS, because of the high operating frequencies and extremely low drive power requirements this level shifting is very simple. In the half-bridge circuit shown, level shifting is done using a small pulse transformer. The complementary emitter followers once again allow high peak currents to charge and discharge the gate capacitance quickly. Figure 8a shows the gate waveforms of both the upper and lower DMOS devices. The upper trace is the upper device and is shown at 100 volts per division. Figure 8b shows the drain voltage and current waveforms. Capacitor C_7 of the transformer primary supplies a pseudo-ground at one-half of the power supply voltage.

This design still maintains a fairly low parts count and is therefore a low cost circuit. The ±15 volt +5 volt outputs make this supply an ideal low cost microprocessor system power supply. This design is discussed in greater detail in Design Aid 80-1 "A Low Cost Regulator for Microprocessor Applications".

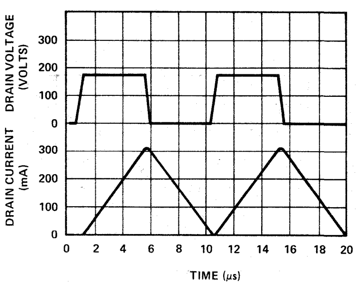
Most experienced power supply designers, when first presented with DMOS as an alternative to bipolars in the switching power supply, immediately see most of the advantages of the devices. A common area of concern, though, is the saturation voltage. The saturation voltage of DMOS when operating at the maximum rated current is typically four to ten times higher than a bipolar with equivalent ratings. This single fact, without considering other characteristics of DMOS, would appear to make DMOS not practical to use in a switching power supply from an efficiency standpoint. When drive requirements and transition losses are considered together with the saturation losses, however, DMOS transistors are nearly always more efficient than bipolars when used in switchers.

An analysis of the power losses associated with the output devices in the half-bridge regulator will serve well to illustrate this point. The saturation losses, transition losses and drive losses will be calculated and compared for this DMOS circuit and for an equivalent circuit using bipolars. In order to simplify the DMOS analysis all the circuitry after output devices in both the bipolar and the DMOS version will be assumed to be 100 percent efficient. Drain (or collector) average current will be assumed to be 1.3 amperes and supply voltage will be 340 volts. Losses for the DMOS design will be calculated first:

$$\text{Saturation Loss} = R_{DS(ON)} \times I_{AVG}$$
$$= 1.0\,\Omega \times 1.3\text{ A} = 1.3\text{ W}$$



Gate Voltage Waveforms of the 150 Watt Half-Bridge Supply
Figure 8a



Drain Voltage and Current Waveforms of the 150 Watt Half-Bridge Supply
Figure 8b

Figures 9a and 9b show the rise and fall times for the VN4000A in the microprocessor power supply circuit. By graphically integrating the area under these curves and making the assumption that the current stays constant during the switching interval the transistor losses are found to be 0.94 watts. This number corresponds well to the number yielded by the equation[1]:

$$\text{Transition Losses} = (0.556)(V)(I_c)(t_{OFF})(f)$$
$$= 1.04\ \text{W (for this example)}$$

Drive losses are slightly more complicated. There are two components to the driving losses. First, there are the losses in the DMOS devices themselves – these are CV^2f losses in the input capacitance. Second, there are the losses in the current buffers and level shifting network. The input capacitance of the Siliconix VN4000A is about 800 pF. At 20 KHz the CV^2f losses per transistor are:

$$P = (800 \times 10^{-12})(15)^2(20 \times 10^3) = 3.6\ \text{mW}$$

therefore, the loss in the DMOS is negligible.

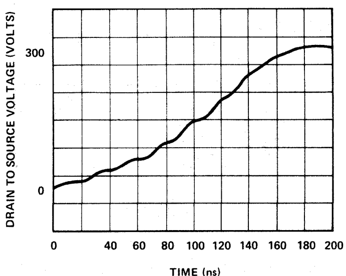
The major loss in the drive circuit is in the level shifting network. Assuming operation at 50 percent duty cycle these losses total 5 watts. Total losses, therefore, are 7.3 watts.

Analysis of the bipolar equivalent will be done using a 2N6671. At 1.3 amperes, the saturation voltage of this device is rated at 0.9 volts. This yields a saturation loss of about 1.2 watts. As expected, this is better than could be achieved with the DMOS.

Rise and fall times on the 2N6671 are rated at 0.5 microseconds. Using the same assumptions and the same equation that were used before with the additional assumption the drive circuit used is capable of driving the devices that quickly, the transition losses turn out to be 4.3 watts.

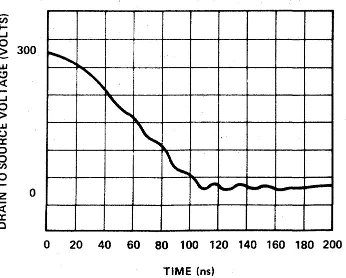
Beta on this device is guaranteed to be 10 minimum. Assuming this beta, drive current required will be an average 1.3 amperes/10 = 130 mA. Because the bootstrap circuit is not practical with this amount of current, a floating power supply is a common way of obtaining the power to drive the devices. Assuming a power supply voltage of 10 volts and efficiency of 60 percent, the drive would require about 2 watts x 2 devices = 4 watts. A level shifting network will still be needed to control the device from the control IC which is not floating. If similar techniques to the ones used in the DMOS level shifter are used, and keeping in mind that only a control signal must be level shifted, 3 watts is a reasonable power to expect to be used. This gives the bipolar version a total power loss of 9.5 watts.

These figures give the DMOS design an edge over the bipolar even at a 20 KHz operating frequency.



Drain Voltage Rise-Time Waveform for the Microprocessor Supply

Figure 9a



Drain Voltage Fall-Time Waveform for the Microprocessor Supply

Figure 9b

At the higher operating frequencies made possible with DMOS, transformer, inductor, and capacitor size and cost will be reduced. These cost reductions along with the savings in the drive circuit give the DMOS design a significant edge over the bipolar.

Figure 10 is the schematic of the output circuitry of a full-bridge switching power supply. This full-bridge configuration is ideal for supplies in the 300 to 1500 watt range. Because of the need for four output transistors, this circuit is not economically practical for lower power designs. Similar techniques to those used for level shifting on the half-bridge design were used. The level shift transformers used were Indiana General pot cores. This level shifting technique is very simple and the same circuit can be used for nearly any size DMOS FET allowing wide ranges of output powers with no drive circuit changes. The power supply's operating waveforms are shown in Figure 11.

CONCLUSIONS

Both analytical data and data taken from actual circuits shown in this paper show the large advantages DMOS power devices offer in switched mode power supply design. These advantages include lower costs, increased performance, better reliability and simplified circuit design.

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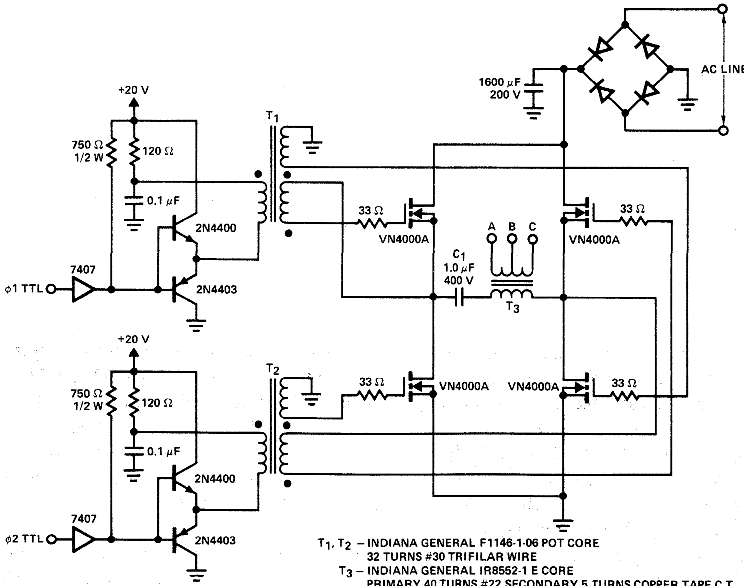
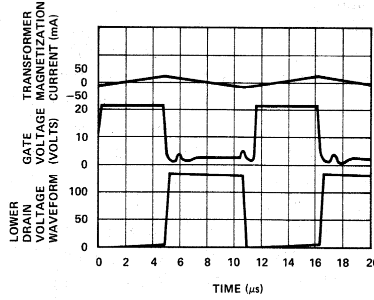


A 300 Watt Full-Bridge, Off-Line Power Output Stage
Figure 10



Operating Waveforms for the 300 Watt Off-Line Supply
Figure 11

Siliconix

Design Aid DA80-1

A Low Cost Regulator for Microprocessor Applications

Build a 100 KHz multiple output switching regulator

INTRODUCTION

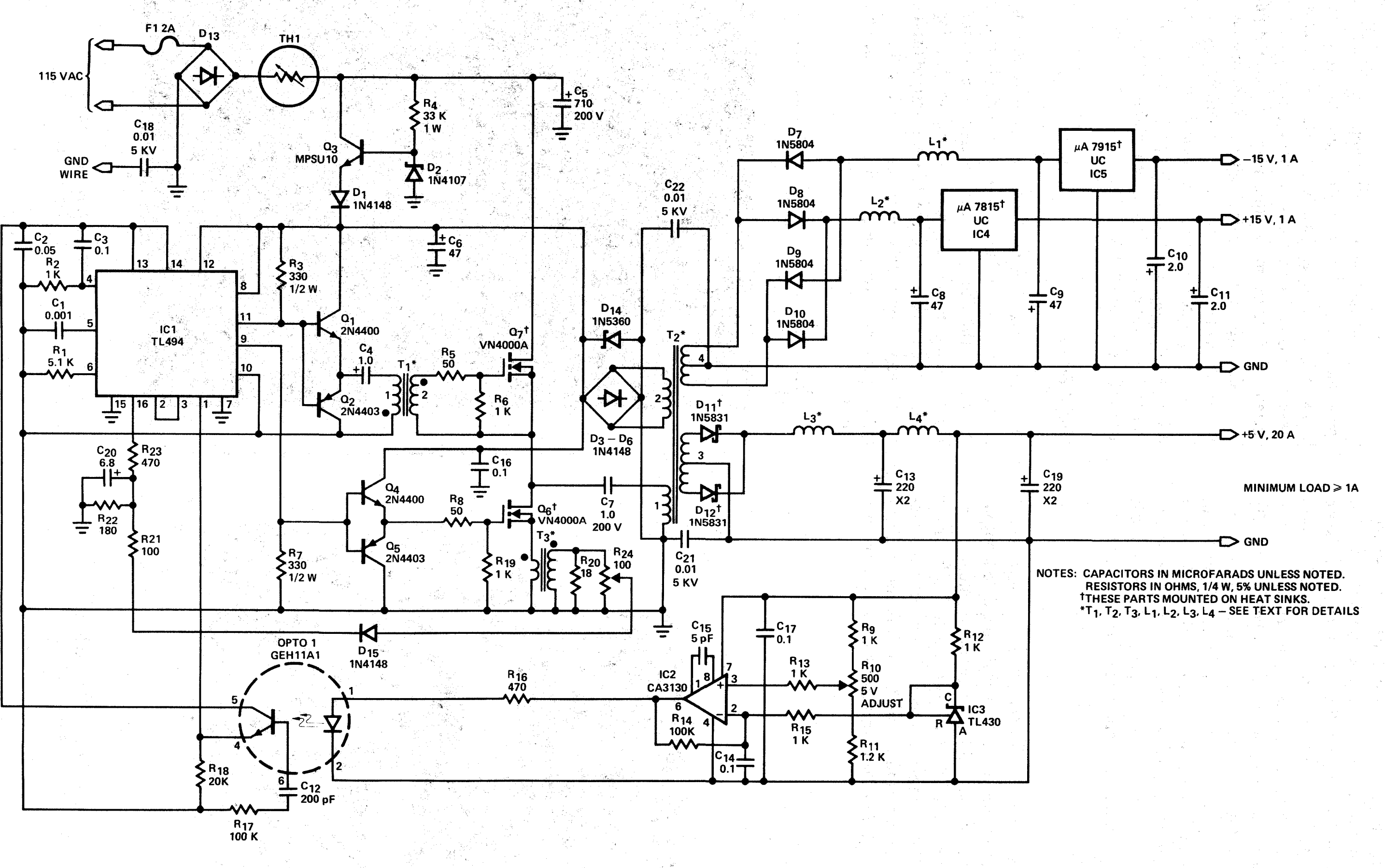
Commercial switching power supplies typically operate at frequencies from 20 KHz to 40 KHz and achieve efficiencies as high as 70% to 75% at a reasonable size and weight. These same efficiencies or better can be realized by increasing the operating frequency to 100 KHz and above when using MOSPOWER® FETs as the power switching transistors. At these higher frequencies much smaller reactive components are necessary thus decreasing the cost, size and weight of the power supply while maintaining the same output power. The main factor limiting the operating frequency of conventional switching supplies is the inherently slow switching times of the power bipolar transistors due mainly to minority carrier storage time. MOSPOWER FETs are majority carrier devices and therefore do not have storage time. The VN4000A series of 400 volt MOSPOWER FETs have maximum switching times of 100 ns thus enabling efficient switching rates up to 500 KHz and above.

This higher operating frequency results in a reduction of the size and cost of ferrites and capacitors needed for the same power transfer and filtering capability. Since DMOS is a voltage controlled device, drive circuits are much simpler and consume less power than high current bipolar drives. DMOS' rectangular safe-operating area means that maximum rated voltage and current can be controlled simultaneously with no fear of second breakdown. Snubbers add extra cost and dissipate excess power in bipolar designs – none are needed to protect MOSPOWER FETs. Catch diodes are required for totem-pole switch configurations such as full-bridge and half-bridge power supplies to catch high voltage inductive spikes. These diodes must be added externally to bipolar designs at extra cost, but they are already built into MOSPOWER FETs.

Their rugged safe-operating area, built-in catch diodes and simpler drive circuits make designing with MOSPOWER FETs simple and economical.

Power Supply Overview

The power supply presented here uses two VN4000A 400 volt MOSPOWER FETs in a half-bridge power switch configuration (Figure 1). Outputs available are +5 volts at 20 amperes and ±15 volts (or ±12 volts) at 1 ampere each. Since linear three terminal regulators are used for the low current outputs, either ±12 or ±15 volts can be made available with a simple change in the transformer secondary windings (see Construction Details). A TL494 switching regulator IC provides pulse width modulation control and drive signals for the power supply. The upper MOSPOWER FET (Q_7) in the power switch stage is driven by a simple transformer drive circuit. The lower MOS (Q_6), since it's ground referenced, is directly driven from the control IC.



100 KHz, 150 Watt Half-Bridge Switching Power Supply
Figure 1

6

For initial start-up, a linear regulator (Q_3, R_4 and D_2 in Figure 1) supplies about 14 volts from the full-wave rectified line voltage for all the drive and control circuitry. Once the power supply starts up, the voltage from a separate secondary winding (#2) is rectified and filtered and used to supply all power to the control IC and drive circuitry. When this supply reaches full voltage (about 18 volts) diode D_1 is reverse biased thus automatically turning-off the less efficient linear regulator used for start-up. A minimum current of one ampere must be drawn from the +5 V output to assure turning off the linear start-up regulator. If less current is drawn from this output, the control circuitry will be powered by the linear regulator and excess power will be dissipated in Q_3.

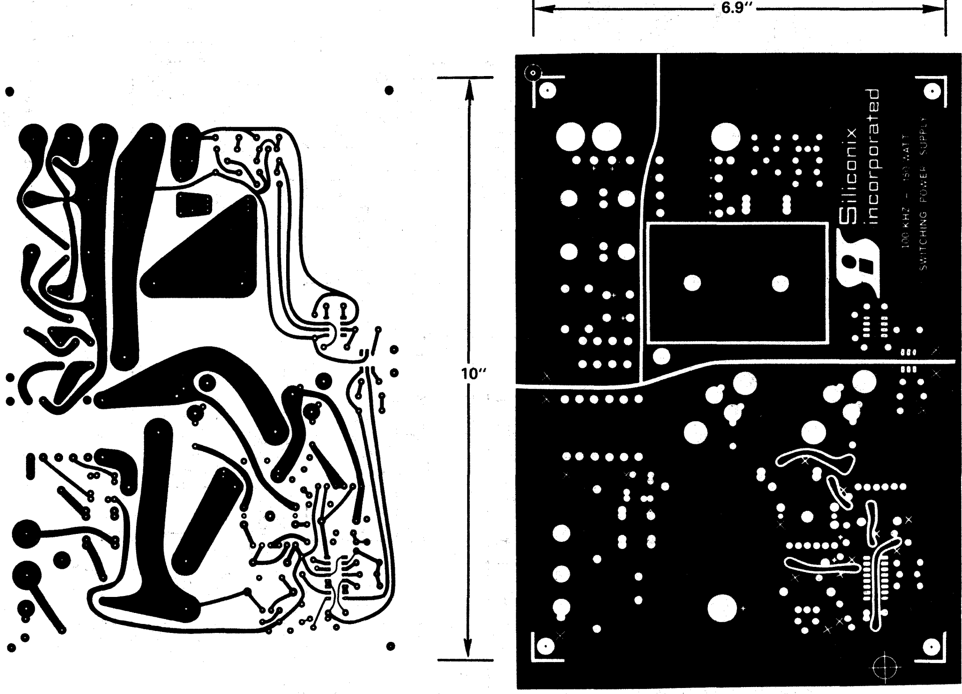
All outputs are isolated from the AC power line. The 5 volt output was chosen to be the main regulated output controlled by the pulse width modulator. Feedback from this output is optically isolated from the line side of the power supply. The complete supply is over-current protected by sensing the source current in the lower MOSPOWER FET (Q_6) and using this signal to shut down the supply.

CONSTRUCTION DETAILS

Careful circuit board layout is very important for the proper operation of high power, high-frequency switching regulators. Single point grounding is absolutely necessary to prevent ground loops from rendering the circuit totally unstable or inoperable. Ground planes are also required to lessen the effects of electromagnetic interference on the circuit. Presented here is a circuit board layout which is known to operate correctly and reliably. Use of this layout will make the construction of this power supply much simpler and will speed your evaluation of the VN4000 series of high-voltage MOSPOWER FETs.

Circuit Board

The circuit board layout (Figure 2) uses double sided construction. Most of the traces are on the bottom side of the board while the top side is used as a ground plane. Three ground planes are used – one for the input and control circuitry, one for the ±15 volt outputs and one for the +5 volt output. If a common ground is desired for all DC outputs, both output ground planes may be connected together.



Circuit Board (Bottom Side)
Figure 2a

Circuit Board (Top Side)
Figure 2b

Plated-through holes are not necessary for making the circuit board, but they would be useful. If plating-through is not used, all of the components connecting to top traces or the ground plane must be soldered on top of the board in addition to any soldering necessary on the bottom. There are a few connections from one side of the circuit board to the other side that do not have components mounted in them. If plating-through is not used, a short piece of wire must be soldered in these holes to both sides of the board. All solder points on the top side are indicated by an 'X'. Table I shows the recommended drill sizes to be used for drilling the circuit board.

TABLE I. RECOMMENDED DRILL SIZES

The following drill sizes should be used on the circuit board:

#66	IC1-IC3, 1/4 W resistors, disc capacitors, opto-isolator, Q_1-Q_5, D_1-D_6, C_6, C_{13}
#60	T_1 bobbin leads, 1/2 W resistors, C_8, C_9, T_3 secondary, TH_1, F_1, C_{18}, C_{21}, C_{22}, D_2, D_{14}
#57	1 W resistors, T_2 bobbin leads, D_7-D_{10}, C_7, D_{13}, C_{13}, C_{19}
#54	R_{10}, IC4, IC5, L_1–L_4, R_{24}, T_3 primary
#44	TO-3 lead sockets, line cord
#23	F_1, IC4, IC5 and TO-3 screw-mount holes, 5 V CT
3/16"	D_{11}, D_{12}
1/4"	C_5
5/16"	Banana jacks

Transformers

Three transformers are used in this power supply: 1) DMOS drive transformer, 2) power transformer and 3) current sense transformer. The winding details explained here should be closely followed, especially for the power transformer T_2.

T_1 – DMOS Drive Transformer

Using the correct bobbin and pot core (see parts list), wind the following:

Primary (1) – 20 turns of #24 enamel wire

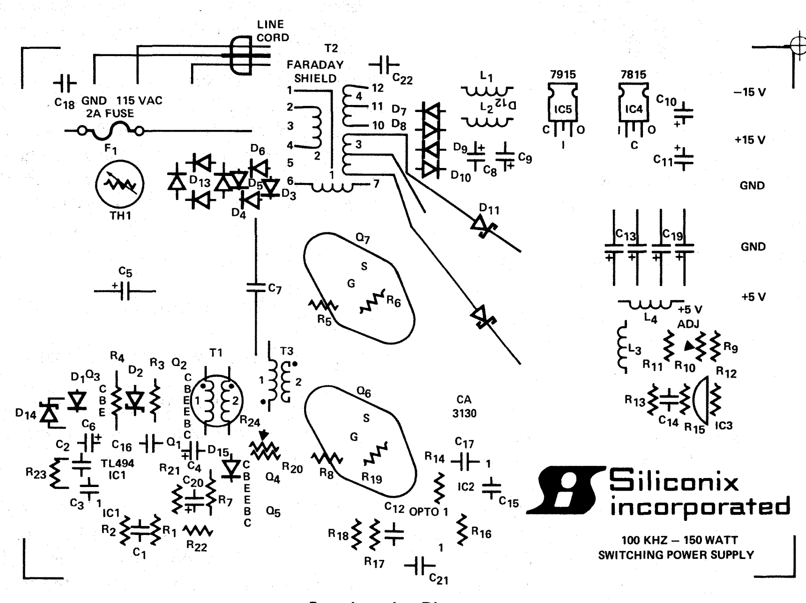
Secondary (2) – 30 turns of #24 enamel wire

Make all connections to the bobbin according to the parts placement diagram (Figure 3).

T_2 – Power Transformer

Using the appropriate bobbin, wind the following (pin 1 of the bobbin has a notch for identification):

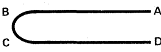
Primary (1) – The primary is made up of a type of litz wire using several strands of regular enamel wire (refer to Figure 4). Cut 8 strands of #28 enamel wire (about 6 feet long) and place them together in parallel. Twist the ends only together (not the whole length), but do not solder. Fold this twisted bundle of wires in half and wind 8 turns of this doubled over bundle onto the bobbin. Cut the folded over end of the bundle so that there are now 4 ends coming out of the bobbin. Twist the ends of each newly cut bundle. Next, connect one of the beginning bundles (D) to the end of the other (B). This effectively connects the bundles in series, wound in the same direction, to form a single 16 turn primary. The purpose of winding in this manner is to equalize the flux across the transformer core. There should now be two ends of the wire free and two ends connected to each other. Connect the free ends to the bobbin as shown in Figure 3. Make sure all windings are wound tight and neat – do not waste any space. Now put a layer of transformer tape to cover the primary.



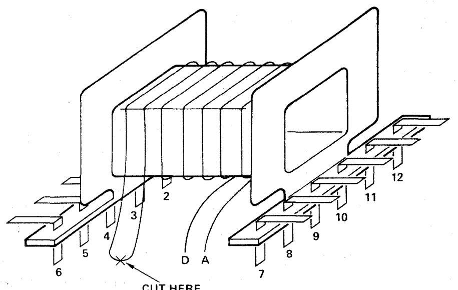
Parts Location Diagram
Figure 3

Step 1 – Parallel 8 strands #28 wire

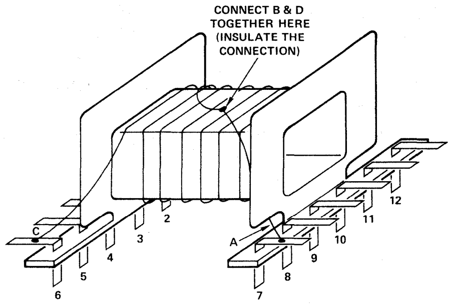
Step 2 – Fold in half



Step 3 – Wind on bobbin



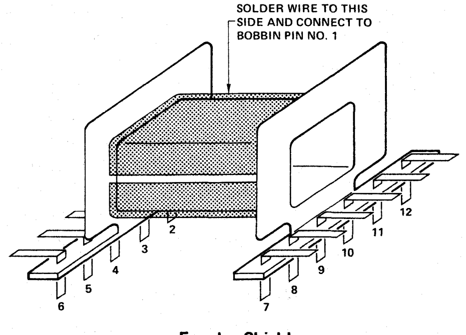
Step 4 – Connect C and A to pins 6 and 7



Primary Power Transformer
Figure 4

Secondary (2) – Start-up Winding: Wind 4 1/2 turns of #24 enamel wire (about 20 inches long) evenly on top of the primary winding. Connect the ends as shown in Figure 3. Put a single layer of transformer tape over the start-up winding.

Faraday Shield – This is a shield used to minimize radiated electromagnetic interference (EMI). Cut a piece of 5/8 inch copper tape about 3 inches long and wrap this around the existing windings (refer to Figure 5). Do not make a complete loop – leave about 1/4 inch between the ends so that they can't touch. Solder a small stranded wire (#20) onto the shield and connect it to the bobbin as shown in Figure 3. Put a layer of transformer tape over the Faraday shield.



Faraday Shield
Figure 5

Secondary (4) – ±15 volt secondary. Make another litz wire similar to the primary but this time parallel 6 strands of #28 enamel wire about 40 inches long (refer to Figure 6). Twist the ends together and double the bundle over itself. Wind 5 turns of this doubled over bundle neatly on the bobbin (4 1/2 turns for ±12 V outputs). Cut the double end and connect B and D together and connect to bobbin pin #11. Connect the two free ends of the bundle to the other bobbin pins. Put a layer of transformer tape over these windings.

Secondary (3) – 5 volt secondary: Make up some insulated copper tape by placing transformer tape on one side of a 10 inch long piece of 5/8 inch wide, 2 mil copper tape (refer to Figure 7). Make two of these insulated tapes. Make sure the transformer tape is slightly wider than the copper tape so that the windings don't short to each other. Wind both of these insulated tapes at once (like bifilar tape) for two turns. Connect the beginning of one tape (A) to the end of the other tape (D) – this is the 5 volt center tap. Connect three #18 stranded wires (or #18 ribbon cable) in parallel to each of the free copper tape ends and to the center tap. Spread out the stranded wires flat when soldering to the copper tape – this makes a much neater and less bulky connection. Connect the ends of these paralleled wires to the output rectifiers and P.C. boards as shown in Figure 3. Wrap a final layer of transformer tape to hold everything together.

T_3 – Current Sense Transformer

Place the windings directly on the toroid:

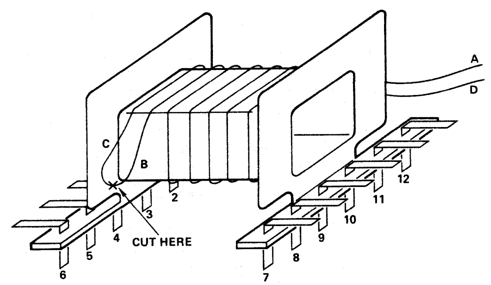
Secondary (2) – Wind the secondary first. Wind 7 turns of #20 enamel wire (about 10 inches long) onto one side of the toroid (Figure 8).

Primary (1) – Form the primary by soldering 2 strands of #16 enamel wire to the circuit board connections (Figure 3). Run these strands through the center of the toroid. This forms the one turn primary. Solder the secondary into the board as shown (Figure 8).

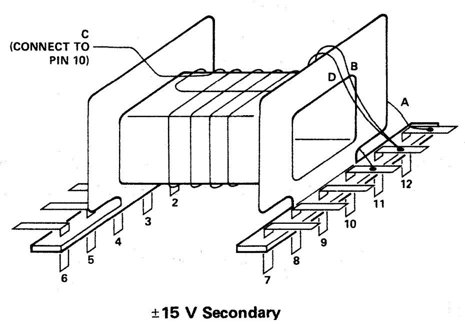
Step 1 – Parallel 6 strands #28 wire

Step 2 – Fold in half

Step 3 – Wind on bobbin

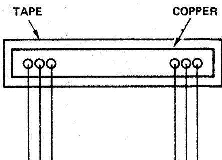


Step 4 – Connect the free ends to bobbin pins #10, 12. Connect doubled over end to pin 11.

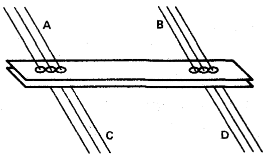


±15 V Secondary
Figure 6

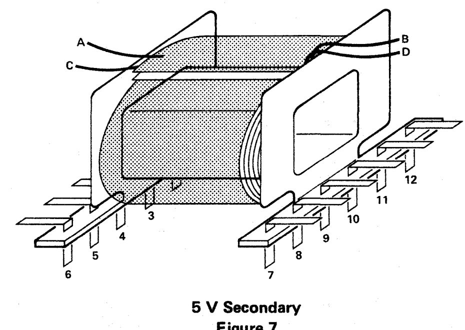
Step 1 – Make two insulated copper straps



Step 2 – Place one strap on top of the other with leads on opposite sides.



Step 3 – Wrap two turns of this double copper tape onto the bobbin. Connect A to D and solder this center tap into the circuit board. Connect the other free ends, B and C, to diodes D_{11} and D_{12}.



5 V Secondary
Figure 7

Output Inductors

L_1 and L_2 are identical. Wind one turn of #18 enamel wire through each core and solder to the circuit board.

L_3 is also one turn, but use three strands of #18 in parallel.

L_4 is an air core inductor. Close wind 10 turns of #16 wire on a 5/16 inch diameter form.

Heat Sinks

Mount the TO-3 heat sinks off the board with 1/4 inch spacers (to make space for R_5, R_6, R_8 and R_{19}). No insulating washers are needed, but heat sink compound should be used.

Mount IC4 and IC5 onto their heat sinks with thermal compound. IC5 should be insulated from the heat sink. Use metal screws for mounting IC4 and IC5 and use plastic screws for the other mounting screws for the TO-66 heat sinks. Cut off the center lead of each regulator and insert the other two pins into the circuit board.

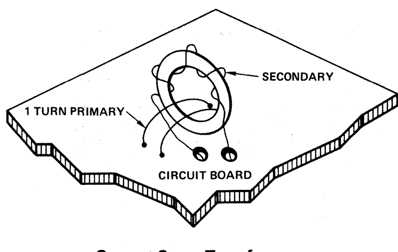
Schottky rectifiers D_{11} and D_{12} mount directly on the heat sink with thermal compound. Use star washers for a good electrical connection when bolting rectifiers D_{11} and D_{12} to the board.

Miscellaneous

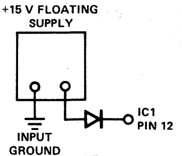
Use star washers on both sides of the board when mounting C_5. IC sockets may be used for IC1, IC2 and Opto 1.

ALWAYS use an isolation transformer when connecting an oscilloscope to look at waveforms on the primary side of the power supply.

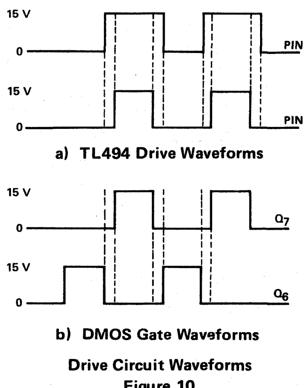
Do not mount Q_3 until after the initial test procedures.



Current Sense Transformer
Figure 8



Power-Up Connection
Figure 9



Drive Circuit Waveforms
Figure 10

Power-Up Procedures

Even though this is a proven circuit board, the control circuitry should be checked separately before powering up the complete supply. To do this, connect an isolated +12 volt supply through a diode between pin 12 of IC1 and ground (Figure 9). Use an oscilloscope to check the drive signals at pins 9 and 11 of IC1. These signals should be in-phase, quasi-square waves at a frequency of 100 KHz (Figure 10a). When these signals check OK, look at the gate waveforms of the MOSPOWER FETs. These waveforms should be out of phase (Figure 10b). Q_7's waveform may have some overshoot. With Q_3 still out of the circuit board, connect a variac or a high voltage DC power supply to the AC input. Slowly increase this power supply voltage (the control circuitry is still running with the floating 12 V supply) while monitoring the output voltage. When the 5 volt output gets somewhere between 4.5 volts and 6.5 volts the supply should begin regulating and further increases in the input voltage will not change the output. No significant current should be flowing from the high voltage supply at this time. Check the ±15 volt outputs for the correct voltage.

While monitoring the supply voltage on pin 12 of IC1 (using a floating voltmeter) connect a load to the 5 volt output to draw about 1 ampere. The supply voltage on pin 12 should increase to about 15-20 volts if the power supply winding #2 on T_2 is working correctly. If everything works correctly so far, disconnect all power supplies and install Q_3 in the circuit board. Using a variac or DC power supply and a floating voltmeter (or an isolation transformer and a non-floating meter), increase the input voltage to the line cord to about 20 VDC or 40 VRMS while monitoring the supply voltage on pin 12 of IC1. This voltage should level off around 10-12 volts. Connect a minimum load to the power supply (5 Ω, 5 W) and increase the line voltage to full voltage. IC1's supply voltage should increase to about 15-20 volts.

The power supply is now ready for use. Adjust the output voltage to 5 volts using R_{10}. Adjust the current limit R_{24} with the ±15 volts fully loaded and the +5 volt output delivering about 25 amperes. A minimum current of about 5 amperes must be drawn from the 5 volt output for the ±15 volt outputs to be able to deliver 1 ampere each.

The power supply may now be plugged in directly to the power line for operation. The only requirement necessary is to have a minimum load of about 1 ampere at all times on the +5 volt output.

Power Supply Features and Specifications

5 Volt Output
- 20 Amperes output current
- 0.2% line regulation (±20% line variation)
- 0.4% load regulation (no load to full load)
- < 100 mVp-p ripple and noise at full load
- Output over-current protection
- ≤ 0.5 ms transient response time (no load to full load)
- Over-current protected

15 Volt Outputs
- 1 Ampere output current each
- 0.2% line regulation
- 1.0% load regulation
- < 10 mV ripple
- Short circuit current limiting

VN4000A Features
- 400 volt BV_{DSS}
- < 1 ohm on-resistance
- < 100 ns switching times
- Rugged safe-operating area
- No secondary breakdown

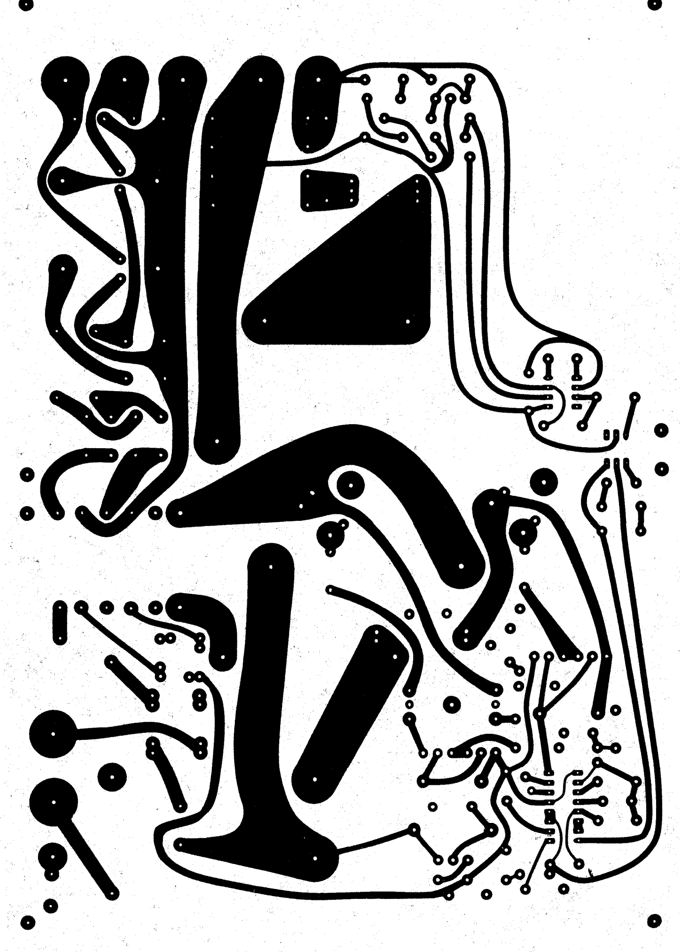
PARTS LIST

Part #	Quantity	Description	Recommended Mfg.
Resistors			
R_1	1	5.1 KΩ ±5% 1/4 W Resistor	Allen Bradley
$R_2, R_6, R_9, R_{12}, R_{13}, R_{15}, R_{19}$	7	1 KΩ ±5% 1/4 W Resistor	
R_3, R_7	2	330 Ω ±10% 1/2 W	
R_4	1	33 K ±10% 1 W	
R_5, R_8	2	50 Ω ±5% 1/4 W	
R_{10}	1	500 Ω ±10% Trimpot	
R_{11}	1	1.2 KΩ ±5% 1/4 W	
R_{14}, R_{17}	2	100 KΩ ±5% 1/4 W	
R_{16}, R_{23}	2	470 Ω ±5% 1/4 W	
R_{18}	1	20 KΩ ±5% 1/4 W	
R_{20}	1	18 Ω ±10% 1 W	
R_{21}	1	100 Ω ±5% 1/4 W	
R_{22}	1	180 Ω ±5% 1/4 W	
R_{24}	1	100 Ω ±10% Trimpot	
Capacitors			
C_1	1	0.001 μF Ceramic Disc	
C_2	1	0.05 μF Ceramic Disc	
$C_3, C_{14}, C_{16}, C_{17}$	4	0.1 μF, 25 V Ceramic Disc	
C_4	1	1.0 μF, 25 V Electrolytic	
C_5	1	710 μF, 200 V Electrolytic (32D)	Sprague
C_6, C_8, C_9	3	47 μF, 25 V Electrolytic	
C_7	1	1.0 μF, 400 V TRW-35	TRW
C_{10}, C_{11}	2	2 μF, 25 V Tantalum	
C_{12}	1	200 pF Mica	
C_{13}, C_{19}	4	220 μF, 10 V Tantalum	Mallory 227K010P1G
C_{15}	1	5 pF Mica or Ceramic	
C_{18}, C_{21}, C_{22}	3	0.01 μF, 5 KV Ceramic	
C_{19}	1	10 μF Electrolytic	
C_{20}	1	6.8 μF Electrolytic	
Integrated Circuits			
IC1	1	TL494 PWM IC	Texas Instruments
IC2	1	CA3130 Op-Amp	RCA
IC3	1	TL430 Voltage Reference	Texas Instruments

PARTS LIST (CONTINUED)

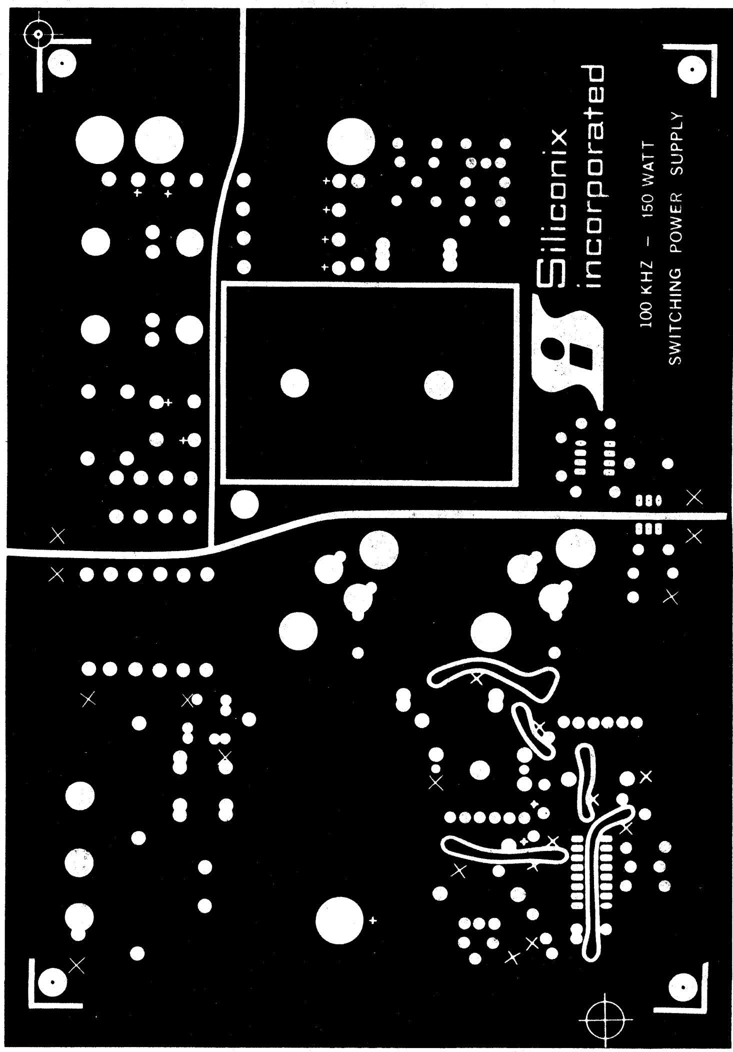
Part #	Quantity	Description	Recommended Mfg.
Integrated Circuits (continued)			
IC4	1	μA7815UC +15 V Regulator (μA7812UC +12 V)	Fairchild
IC5	1	μA7915UC −15 V Regulator (μA7912 −12 V)	Fairchild
Diodes/Rectifiers			
$D_1, D_3–D_6, D_{14}, D_{15}$	6	1N4148 Diode	Motorola
D_2	1	1N4107 Zener	Motorola
$D_7–D_{10}$	4	1N5804 Fast Recovery	Unitrode
D_{11}, D_{12}	2	1N5831 Schottky	Unitrode
D_{13}	4	1N5406 Rectifier	Motorola
D_{14}	1	1N5360 Zener	Motorola
Transistors			
Q_1, Q_4	2	2N4400	Motorola
Q_2, Q_5	2	2N4403	Motorola
Q_3	1	MPSU10	Motorola
Q_6, Q_7	2	VN4000A MOSPOWER FET	Siliconix
Ferrites & Accessories			
T_1	1	F1146-1-06 Pot Core	Indiana General
T_1 Bobbin	1	B475-1	Indiana General
T_2	1	IR8031-1	Indiana General
T_2 Bobbin	1	B680-2	Indiana General
T_3	1	BBR7727-1 Toroid	Indiana General
L_1, L_2	2	F1146-1-TC9-315	Indiana General
L_3	1	F2037-1-TC9	Indiana General
Miscellaneous			
Opto 1	1	H11A1 Opto-Isolator	G.E.
TH_1	1	3D304 Thermistor	Midwest Components, Inc.
F_1	1	2 A Fast Blow Fuse	Buss
TO-3 Heat Sink	2	LAT03B5CB	IERC
TO-220 Heat Sink	2	LAD66A4CB	IERC
TO-3 P.C. Sockets	4	LSG-3DG2-1	Augat
D_{11}, D_{12} Heat Sink	1	E240-001	IERC
Output Banana Jacks	5		
3-Wire Line Cord	1		
Fuse Block for F_1	1		
Transformer Tape		Type 10 Epoxy Film	3M
Copper Foil		Type 1194	3M

Circuit Board (Bottom Side)



Half Size

Circuit Board (Top Side)



Half Size

Application Note AN79-1

A 500 KHz Switching Inverter for 12 V Systems

This note describes the design of a 12 V to ±20 V inverter. The design is of the flyback type, made much more practical by the use of VMOS devices running at a high switching rate. It is an energy transfer circuit, not a voltage or current transfer circuit; the output power is maintained at a constant level for a given pulse width-modulator (PWM) operating point. If the load requires less current, the output voltage will soar. Conversely, if the output current demand increases, the output voltage will sag to maintain the constant output power (V x I). This contrasts sharply with conventional circuits that deliver a constant output voltage per PWM operating point. Maintaining constant power permits simplified circuitry with reduced magnetic and filter requirements.

The principles of operation may be described by the basic circuit shown in Figure 1, which includes the pulse width modulator (PWM) control circuit; the high frequency MOSPOWER FET Switch; the flyback circuit inductor (L), diode (D) and capacitor (C); and an error amplifier.

At the heart of this design is the PWM control circuit which provides the control pulse to the VMOS Power Switch in the flyback circuit. The output of the PWM is a pulse whose width is proportional to the input control voltage and whose repetition rate is determined by an external clock signal. To provide the control input to the PWM and to prevent the output voltage from soaring or sagging as the load changes the error amplifier and reference voltage complete the design. They act as the feedback loop in this control circuit much like that of a servo control system. Pertinent waveforms are given in Figure 2; 2a describes the conditions that exist at 50% (maximum) duty cycle and 2b describes those at a low duty cycle.

Operation is as follows:

1. Between t_0 and t_1 the VMOS is turned on and applies the supply voltage across L. The drain current is closely approximated as $I_L = t \times V_S/L$ and the final current I_L (peak) $= (t_1 - t_0)\, V_S/L$. The energy stored in L is $E_L = (t_1{}^2 - t_0{}^2)\, V_S{}^2/2L$.

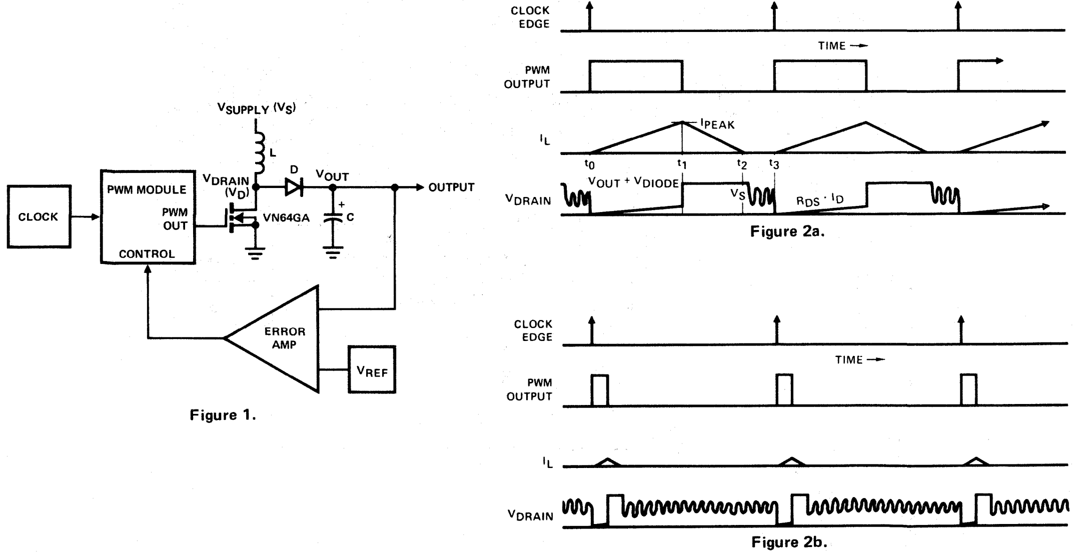


Figure 1.

Figure 2a.

Figure 2b.

2. At the instant of t_1 the VN64GA is turned off and its drain voltage increases to the voltage on C plus the forward voltage drop of D because of the inductor L. This works well when V_{OUT} is much larger than V_S and permits nearly all of the energy stored in L to be transferred to C with no large current or voltage spikes.

3. Between t_2 and t_3, no net DC current flows through L, and V_{DRAIN} tends toward V_{SUPPLY}, although a ringing will occur between L and the capacitance of the VMOS and D. The cycle is repeated at a frequency f_{CLOCK}, such that the power drawn from V_S is $(1/2\,(t_1 - t_0)^2\,V^2{}_S)/f_{CLOCK}$.

If we let the duty cycle $\delta = \frac{t_1 - t_0}{t_3 - t_0} = (t_1 - t_0)\,f_{CLOCK}$,

where $f_{CLOCK} \equiv \frac{1}{t_3 - t_0}$, then $P_{IN} = \frac{\delta\,V^2{}_S\,(t_1 - t_0)}{2}$.

If $\delta = 1/2$ max, then P_{IN} max $= V^2{}_S/8L\,f_{CLOCK}$.

The peak current through the VMOS will closely be $\frac{4\,P_{OUT}}{\eta V_S}$; and the value of inductor L will be $\eta V^2{}_S/$ $8\,f_{CLOCK}\,P_{OUT}$, where η is the overall power efficiency of the circuit.

The power losses in the circuit are, in order of importance:

A. $(I_D)^2\,R_{DS}$ loss in the VMOS switch

B. $I_{LOAD}\,V_F$ loss in the catch diode D

C. Transient charge losses in D due to a slow turn-on characteristic. This actually allows many volts of forward bias on D just at time T_1 while the diode is attempting to turn-on. Turn-off losses are not important in this circuit.

D. Loss in L due to hysteresis and saturation effects. The inductor is required to pass all of $I = 4P_{OUT}/\eta\,V_{SUPPLY}$, which usually results in magnetic saturation and losses. Fortunately, the higher frequencies allow fewer turns on L, reducing the number of turns and I_{SUPPLY} product, and the core material of L can be high-frequency ferrite, which is less prone to saturation (for a given inductance).

E. Simple $C_{STRAY}\,V^2{}_{OUT}\,f_{CLOCK}$ losses, where C_{STRAY} includes C_{DS} of the VMOS and C_D of the rectifier.

Figure 3 is the schematic of a simple 35 watt inverter designed to produce ±20 V regulated outputs from 12–16 volt inputs. U_1 is a simple Schmitt-trigger oscillator with a nominal 50% duty cycle. This duty cycle waveform buffered into Q_5 by Q_4 and U_2 through U_6 runs the system at full output power.

The duty cycle is reduced to stabilize the output voltage by the feedback amplifier Q_2 and its 18 V zener. Q_1 and its associated diodes switch Q_2's discharge current away from C during the discharge period of the transformers field, and allow it to shorten the period in which primary current is drawn through the transformer. Q_3 and its 21 V zener prevent the output from soaring (if a fault condition occurs in the feedback regulator) by simply clamping Q_5's gate drive.

L is wound on a ferrite core; I used a wideband toroid 1 1/2" in diameter with a cross-sectional area of about 1/10 in^2. The resistance of the winding should be held to less than 1/20 Ω; #22 wire is adequately large.

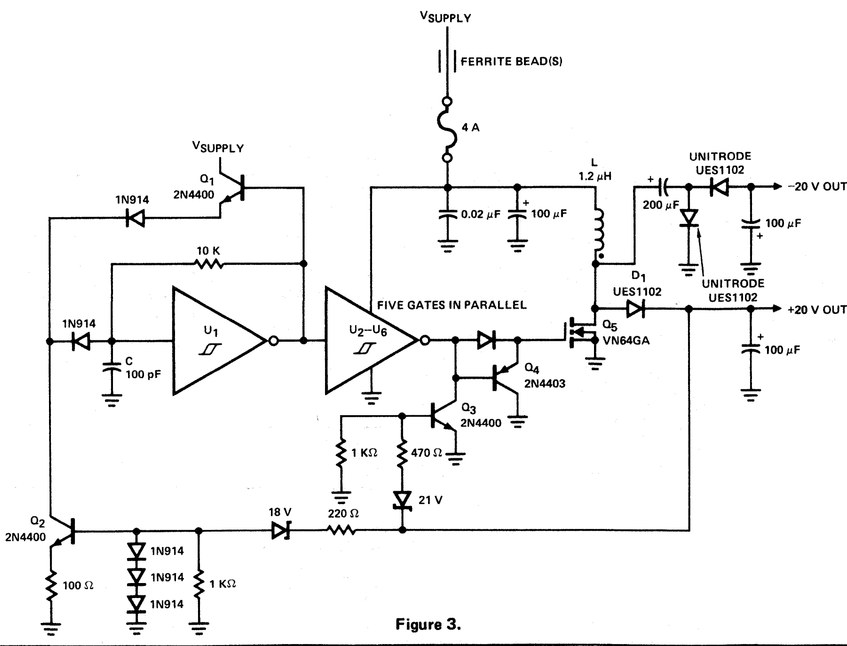


Figure 3.

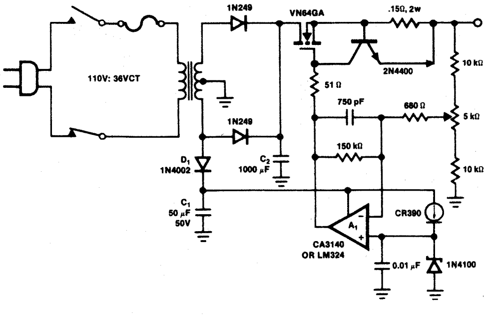
14 Volt, 4 Amp Battery Charger/Power Supply

Very low drive power makes MOSPOWER FETs more desirable than bipolar transistors in this simple, minimum-parts-count battery charger. A low-power operational amplifier is used to control the VN64GA. A power bipolar transistor in the same circuit would require over 100 mA of base current and a much more complicated drive circuit thus reducing overall efficiency and increasing circuit complexity.

Operational amplifier A_1 directly drives the VN64GA with the error signal to control the output voltage. Peak rectifier D_1, C_1 supplies error amplifier A_1 and the reference zener. This extra drive voltage is necessary because the VMOS gate voltage must exceed its source voltage by several volts for the VN64GA to pass full load current.

The output voltage is pulsating DC which is quite satisfactory for battery charging. To convert the system to a regulated DC supply, capacitor C_2 is increased and another electrolytic capacitor is added across the load. The response time is very fast, being determined by the op-amp.

The 2N4400 current limiter circuit prevents the output current from exceeding 4.5A. However, maintaining a shorted condition for more than a second will cause the VN64GA to exceed its temperature ratings. A generous heat sink, on the order of 1 °C/W, must be used.



400 Volt, 60W Push-Pull Power Supply

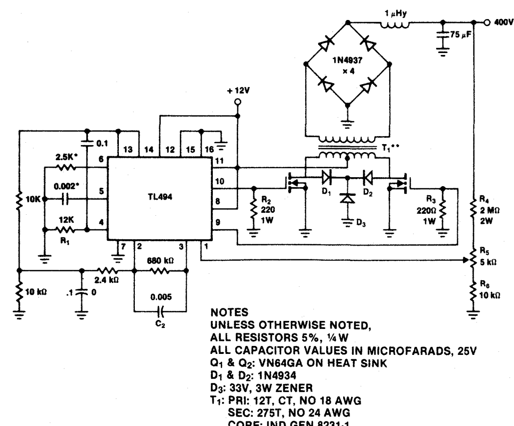
An increase in dc/dc-converter efficiency is achieved by using MOSPOWER® FETs in the power stage. Because the FET's drive requirements are low, a standard switching-regulator IC can provide both control and drive functions.

The design shown delivers a regulated 400V, 60W output. The TL494 switching regulator governs the operating frequency and regulates output voltage. R_1 and C_1 determine switching frequency, which is approximately 0.5RC—100 kHz for the values shown.

The TL494 directly drives the FET's gates with a voltage-controlled, pulse-width-modulated signal. Each FET requires only 10 mW; the remaining drive power is dissipated by the turn-off resistors, R_2 and R_3. Operating in a push-pull configuration, the FETs switch primary current on in about 150 ns and then off in 300 ns. These short switching times—about a tenth of equivalent bipolar devices—and the resulting high operating frequency permit using physically small reactive components.

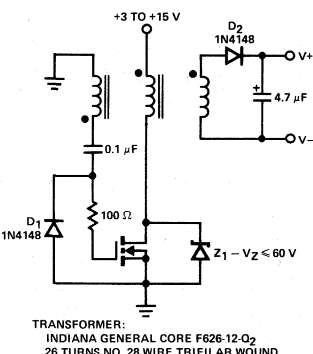
After full-wave rectification, the output waveform is filtered by a choke-input arrangement. The 1-µH, 75-µF filter accomplishes the job nicely at 100 kHz. A feedback scheme using R_4, R_5 and R_6 provides for output-voltage regulation adjustment, with loop compensation handled by C_2. Diodes D_1 and D_2 provide isolation and steering for the 33V zener transient clamp, D_3.

Output regulation is typically 1.25% from no-load to the full 60W design rating. Regulation is essentially determined by the TL494. Output noise and ripple consists mainly of positive and negative 0.8V spikes occurring when the output stage switches.



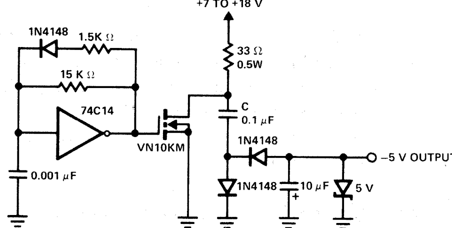
Self Oscillating Flyback Converter

A low-power converter suitable for deriving a higher voltage from a main system rail in an on-board application is shown below. It uses the core characteristics to determine frequency. With the transformer shown, operating frequency is 250 KHz. Diode D_1 prevents negative spikes from occurring at the VMOS gate, the 100 Ω resistor is a parasitic suppressor, and Z_1 serves as a dissipative voltage regulator for the output and also clips the drain voltage to a level below the rated VMOS breakdown voltage.



Positive Input/Negative Output Charge Pump

A charge pump is a simple means of generating a low-power voltage supply of opposite polarity from the main supply. The 74C14 IC is a self oscillating driver for the VMOS power switch. It produces a pulse width of 6.5 μs at a repetition frequency of 100 KC. When the VMOS device is off, capacitor C is charged to the positive supply. When the VMOS transistor switches on, C delivers a negative voltage through the series diode to the output. The zener serves as a dissipative regulator. Because the VMOS transistor switches fast, operation at high frequencies allows the capacitors in the system to be small.



Don't Trade Off Analog Switch Specs. VMOS—A Solution to High Speed, High Current, Low Resistance Analog Switches

INTRODUCTION

For analog switches, Vertical MOS (VMOS) transistors give you a nearly ideal combination of characteristics–without the tradeoffs required by the more conventional components. These devices are now available from two American suppliers: Siliconix and its licensee, Semtech.

Unlike the commonly used N-channel JFETs, VMOS chips that handle more than a few hundred milliamps are also small enough for economical production. Smaller chips lead to lower inherent capacitances. Moreover, the basic VMOS structure provides lower ON resistance.

Some analog switches use relays, bipolar transistors and even triacs. Although electromechanical relays offer the lowest ON resistance initially, their ON resistance will vary with current and degrade with use. Also, relays suffer from mechanical limitations.

Bipolar transistors require base-drive current that causes offset in the switched analog signal. Triacs are only suitable for switching raw power; for analog switching, they introduce too much offset and non-linearity although they easily handle high power.

VMOS Offers High Performance

VMOS devices aren't limited by any of these disadvantages. They can switch 10 W, linearly, over a wide dynamic range. In addition, VMOS input impedance is very high, and only input voltage (no current) turns the transistors OFF or ON. And since the drain-to-source channel is purely resistive while ON, you get low distortion.

VMOS transistors in analog switches offer several more advantages, including

- 1.8 Ω ON resistance, which results in low insertion loss in low-impedance systems
- 2.0 A DC current capability–paralleling three VMOS devices increases this capability to 6.0 A and unlike other devices, paralleled VMOS do not require power-wasting ballast resistors
- 3 A peak current, which makes VMOS super for driving capacitive lines and quickly charging and discharging capacitors in high speed A/D converters, sample and hold circuits, and integrators
- 60 dB isolation at 10 MHz and 500 nA DC leakage in the OFF state
- Enhancement-mode operation with a 0.8 to 2.0 V threshold, which gives VMOS direct compatibility with CMOS and TTL. And the logic gates aren't loaded by the VMOS.
- Linear ON resistance, which results in low total harmonic and intermodulation distortion

What's more, all these capabilities come in a TO-202AA package.

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Examine the output characteristics of a low resistance VMOS device like the Siliconix VN46AF. A look at the transfer characteristic in Figure 1A reveals that varying the gate-to-source voltage from 0 to +10 V switches the VN46AF from OFF to ON--with a 3 Ω ON resistance. From the curve you can see that the device turns OFF well before zero volts, which eases interfacing with logic.

In the VN46AF schematic in Figure 1B, note that the body and source are internally connected. Figure 1C and 1D, respectively, show simplified models of the VN46AF's OFF and ON states. Diode D_1 is the body-to-drain PN junction. When the VN46AF is OFF, its drain current vs drain-to-source voltage characteristics (Figure 1E) is essentially the curve for D_1.

The breakdown for D_1 is 40 V, and the diode exhibits forward conduction for drain-to-source potential as low as −0.6 V. This diode therefore constrains the analog voltage, which a simple switch (one VMOS transistor) can handle, to between −0.6 and +40 V.

When the VN46AF is ON, a 2 Ω resistance is in parallel with D_1. Maximum continuous current in either direction is 2.0 A, even though the diode is forward-biased for currents over 0.5 A.

One VMOS Device Makes an Analog Gate

VMOS characteristics are put to good use in the analog switch of Figure 1F. In the ON state, the gate of the VN46AF is positive with respect to the source. In the OFF state, the gate-to-source voltage is zero. The 2.0 A capability and the 3 Ω ON resistance of the VMOS transistor can be fully exploited in this circuit. The input signal, however, is restricted to positive voltages and must always be greater than the output voltage. Otherwise, OFF isolation is impaired.

Both ON and OFF switching takes 200 ns; charge feed-through during the ON-to-OFF transition is 80 pC with a 50 Ω load. Charge transfer is, of course, especially important in sample and hold systems. For example, 80 pC into 0.01 μF causes an offset of 8 mV.

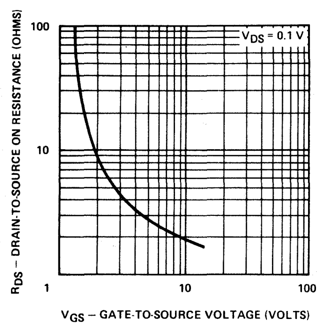
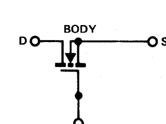
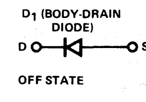


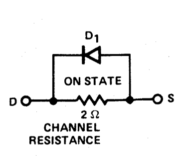
Figure 1A



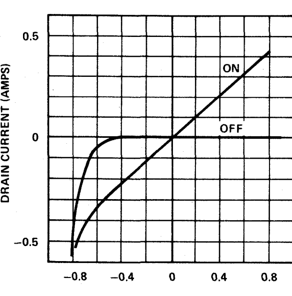
Schematic Symbol of VN46AF
Figure 1B



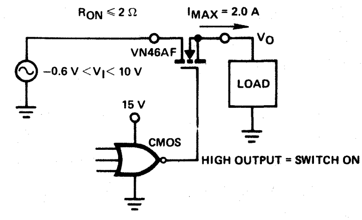
Equivalent OFF Condition (V_{GS} = 0)
Figure 1C



Equivalent ON Condition
(V_{GS} = 10 V)
Figure 1D



Small Signal Characteristics of VN46AF
Figure 1E



A Simple Unidirectional VMOS Analog Switch ($v_i \geqslant v_o$)
Figure 1F

The VN46AF switches from OFF to ON with a 3 Ω drain-to-source resistance, when its gate-to-source potential swings from 0 to +10 V. The device turns OFF at about 1 V(A). Some VMOS transistors (B) carry an on-board zener diode that protects the gate-to-source junction. A VMOS transistor is equivalent to two diodes in the OFF state (C), when the gate-to-source voltage is less than the threshold value. The equivalent diode, D_1 is shunted by 3 Ω when the VMOS device is ON (D), with the gate-to-source potential at +10 V. The small signal drain-to-source voltage vs current characteristic (E) is essentially determined by the body-to-drain diode. The input is restricted to positive voltages in the single-VMOS analog gate (F).

Figure 1

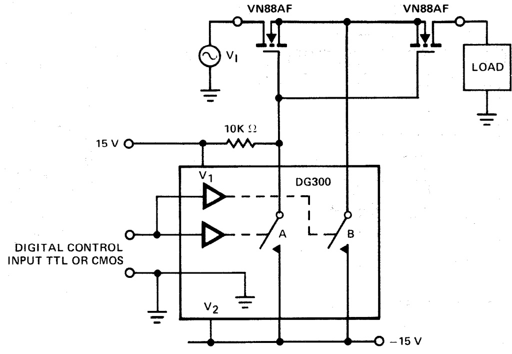
In Series, They Switch Both Polarities

To increase the switch's dynamic range, connect two VN88AF's in series (Figure 2A). In the ON state, both halves of the DG300 analog switch are open, so the gates of both VN88AF's are pulled to +15 V through the 10K Ω resistor. The ON resistance of this analog switch is twice as high as the drain-to-source resistance of a single VN88AF. The maximum current that this two-transistor switch can handle is the same as that for a single-transistor switch (2.0 A).

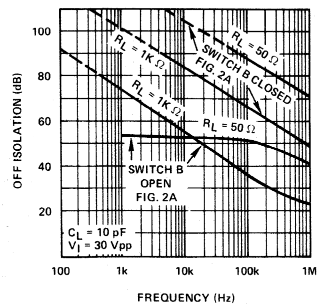
The switch is turned OFF by shorting the gates to the negative supply, thereby reducing the gate-to-source voltage to less than the threshold of 0.8 V. The second section of the DG300 adds 30 dB OFF isolation by shunting the signal-leakage path (through both sources) to the negative supply. OFF-isolation curves (Figure 2B) show that the DG300 raises the circuit's isolation and that decreasing the load resistance increases isolation.

Since the two transistors are back-to-back, one body-to-drain diode is always reverse-biased. This eliminates the OFF-state problem caused by forward-biasing the diode.

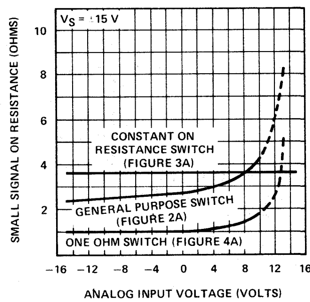
Since the bidirectional switch's gate drive is referenced to a fixed supply, its ON resistance varies with the input analog voltage (Figure 2C). This variation introduces distortion when you're driving low-impedance loads such as speakers or transmission lines. For constant ON resistance, use the circuit in Figure 3A.



A General Purpose Bidirectional Analog Switch
Figure 2A



OFF Isolation vs Frequency
Figure 2B



Small Signal ON Resistance vs Analog Input Voltage
Figure 2C

ON resistance is doubled in the two-VMOS switch (A), but inputs of both polarities are handled without losing isolation. The DG300 analog gate (B) raises the circuit's isolation by 30 dB. Decreasing load resistance also improves isolation. With the gate drive referenced to a fixed voltage (C), the ON resistance varies undesirably with the input, and generates distortion, especially with low impedance loads like speakers and transmission lines.

Figure 2

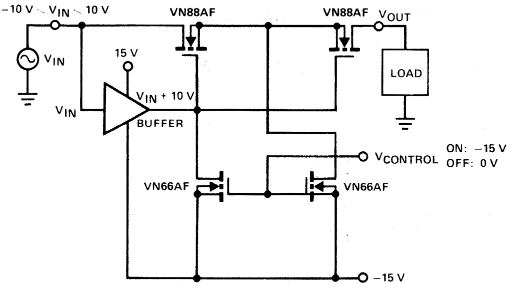
Bootstrapping Adds Linearity

In the ON state, a bootstrap voltage that tracks the input drives the gates of the VN88AF's. This bootstrapping keeps the VMOS's gate-to-source voltage constant and independent of the input signal. So, changes in the input-signal level do not modulate the ON resistance of the switch.

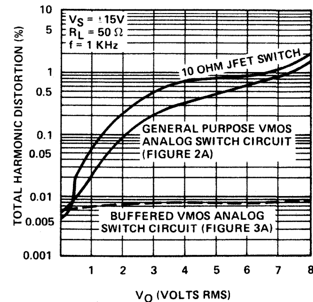
The buffer circuit reduces the computed total harmonic distortion from 1.5% to 0.005%, for 8 Vrms at 1 kHz into 50 Ω (Figure 3B). The popular 10 Ω DG186 JFET analog switch generates a higher total harmonic distortion of about 2%.

The two buffer circuits shown in Figures 3C and 3D isolate the input signal and employ a zener diode to provide a fixed gate-to-source voltage. The general-purpose buffer of Figure 3C has a flat frequency response of up to 300 kHz and accepts inputs ranging between ±15 V. The buffer of Figure 3D, VN66AK source follower, has its frequency response extended to 50 MHz and, when operated from ±30 V supplies, increases the signal range to ± 30 V.

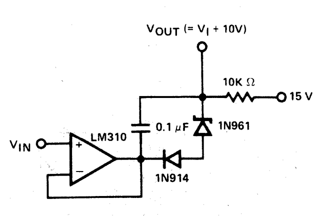
The VN66AK and VN88AF do not have on-board zener diodes like the VN66AF transistor. At the expense of the diode protection, the VN66AK and VN88AF gain lower capacitance from gate-to-source and reduced DC "see through" from driver to signal path. Bootstrapping the switch's gate circuits with a buffer permits the switch to operate with low distortion even as the signal amplitude comes close to the positive supply voltage.



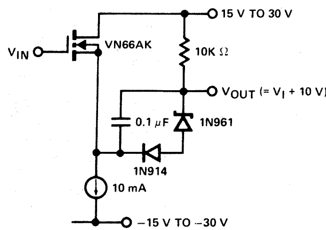
Low Distortion Constant ON Resistance Switch
Figure 3A



Distortion Improvement Using the Buffered Analog Switch
Figure 3B



General Purpose Buffer
Figure 3C



High Speed Buffer
Figure 3D

Bootstrapping the gate and input cuts distortion by holding the ON resistance constant (A). The buffered bootstrap circuit (A) distorts less than either a JFET or a nonbootstrapped VMOS analog switch (B). A general-purpose buffer (C) using the LM310 op amp is suitable for low speed switches, but when you need a fast analog switch, use the VN66AK buffer (D). In addition to speed, this buffer gives you increased isolation.

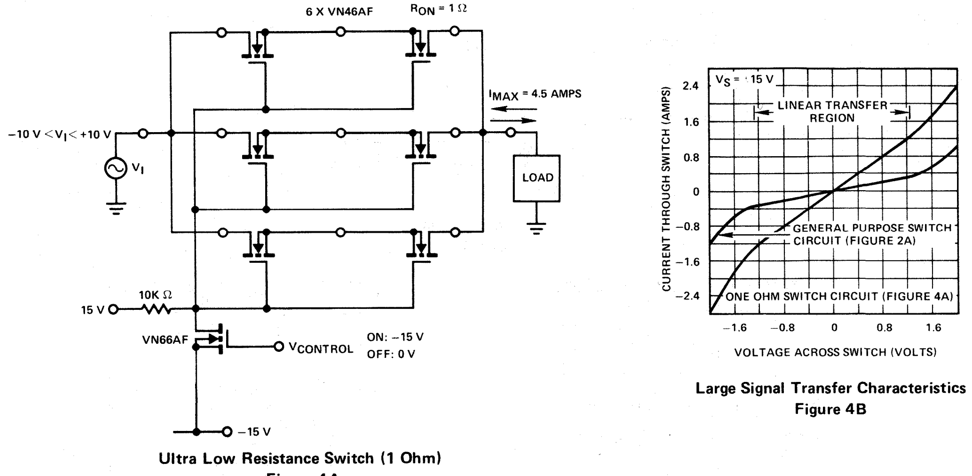
Figure 3

MOSPOWER FET Devices Parallel Without Padding

Paralleling devices lowers the total ON resistance. For example, three paralleled legs, each with two VN46AF's in series, make a 1 Ω switch (Figure 4A). Because VMOS devices are immune to current hogging, no ballast or balance resistors are needed. Negative tempcos, a VMOS feature, cause these devices to draw less current as they heat up. As a result, excess current is automatically shared by paralleled VMOS devices.

Paralleling three VN46AF's not only decreases ON resistance, but also increases the current capability to 6.0 A and extends the linear range of the large signal transfer characteristic from 0.3 to 1.2 A (Figure 4B).

The voltage range of the basic analog switch can also be increased. Simply use a higher breakdown VMOS unit (Figure 5). The VN98AK's have a 90 V breakdown, which allows up to ±40 V of voltage swing capability. However, these higher voltage devices do carry a penalty—the ON resistance is higher: 3.5 Ω vs 3.0 Ω for the VN46AF. Zener diode D_1 limits the gate-to-source potential to 30 V, and thereby prevents a possible gate-oxide rupture. Diode CR110 limits the current from the 50 V gate-bias supply.

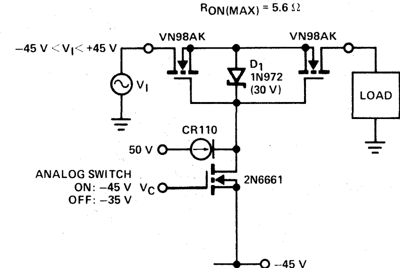


Ultra Low Resistance Switch (1 Ohm)
Figure 4A

Large Signal Transfer Characteristics
Figure 4B

No ballast or balance resistors are needed when VMOS devices are paralleled (A) because negative tempcos immunize them from current hogging. Paralleling extends the linear range from 0.3 to 1.2A (B) as it decreases the ON resistance of the analog switch to 1 Ω and increases its current-handling capability to 4.5 A.

Figure 4



90 V Peak to Peak Analog Switch

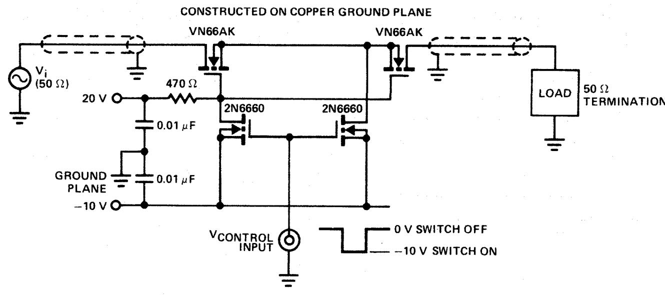
You pay for 90 V breakdown in the VN98AK with 3.0 Ω ON resistance, which allows swings of ±40 V. The zener diode limits the gate to-source potentials to 30 V.

Figure 5

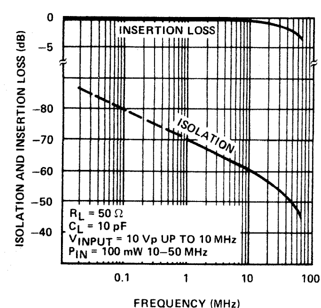
For the Ultimate in Switching Speed

The high power RF switch shown in Figure 6A performs very well up to 50 MHz—with turn-ON and turn-OFF times of 50 ns. At 10 MHz, isolation is 60 dB with a 20 V pk-pk input signal. Insertion loss is only 1 dB with a 50 Ω load (Figure 6B). The gain vs input power curve in Figure 6C shows that the RF analog switch using VN66AK's can put 1 W into a 50 Ω load at 14 MHz. The two-tone, third order, intermodulation product curves show a 42 dB intercept point with 1 dB of gain compression at 25 dBm input power.

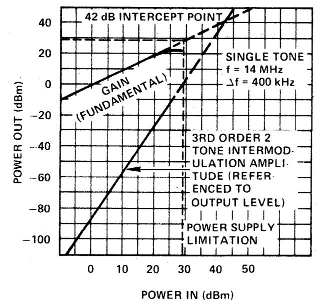
Turn-ON time of the switch (Figure 6D) is determined by the passive pull-up resistor combined with the capacitance at the gates of the VN66AK's. The negative turn-OFF transient is caused by charge-coupling to the output through the output capacitance of the VN66AK.



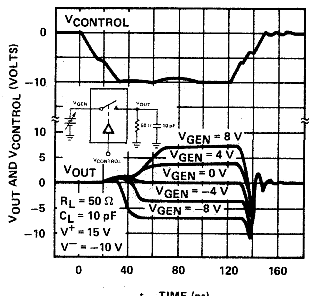
RF Analog Switch
Figure 6A



Insertion Loss and Isolation vs Frequency of RF Analog Switch
Figure 6B



Gain and Two Tone 3rd Order Intermodulation
Figure 6C



Switching Response of RF Switch into 50 Ohm Load
Figure 6D

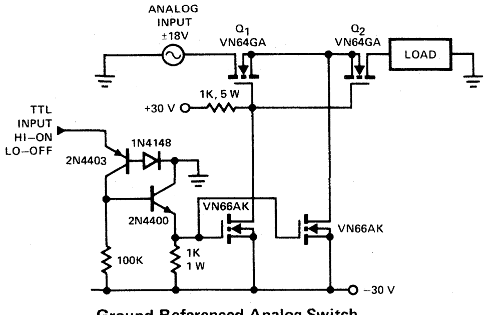
The VN66AK switches high power at RF (A). At 10 MHz, a 20 V pk-pk signal is attenuated by 60 dB and the insertion loss is only 1 dB into 50 Ω and 10 pF (B). Third-order intermodulation distortion is given by the 42 dB intercept point, and 1 dB gain compression occurs at 25 dBm input for 14 MHz (C). The negative turn-OFF transient (D) is caused by charge-coupling to the output through the output capacitance of the VN66AK.

Figure 6

High Current Analog Switches

For analog switches, MOSPOWER FETs provide an ideal combination of characteristics without the usual trade-offs inherent in more conventional components. Bipolar transistors require base current that causes offsets in the switched analog signal. Triacs also produce an offset and can only be used to switch AC or interrupted DC signals. MOSPOWER FETs provide none of these disadvantages. In the on-state, MOS looks resistive thus providing no offset voltage and very low distortion.

Either ground referenced or high-voltage isolated bidirectional analog switches can be configured with VMOS. Drive circuits are simple because VMOS drive power requirements are minimal. The very low on-resistance of the VN64GA makes it an ideal choice for analog switch circuits.



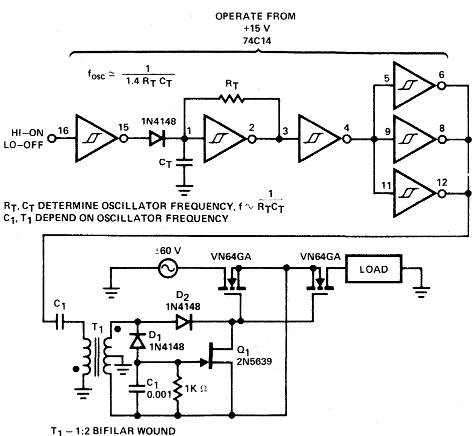
Ground Referenced Analog Switch

The circuit above shows a ground referenced, bidirectional switch with a signal range of ±18 volts for currents up to 12.5 amperes. Two VMOS devices are necessary to enable current control in both directions. This is not possible with a single device because of the drain-source diode which is inherent in the VMOS devices. Input signal range for this switch is limited by the maximum allowable gate-source enhancement voltage of ±30 volts. Since 12 volts enhancement is required for 12.5 amperes output, then ±18 volts is the maximum signal range. Higher voltage inputs begin to turn off the VN64GA at the positive signal peaks thus limiting the VMOS to pass less current. Turn-on is accomplished by driving the gates high (+30 V) and turn-off by driving the gates low (–30 V). Off isolation is enhanced by biasing the common source node at –30 volts. This has the effect of shunting to ground any signal that feeds through the VMOS drain-source capacitance.

Isolated gate drive is required to operate the analog switch over its full ±60 volt operating range. One way to accomplish this is to use a transformer isolated drive in a DC to DC converter as shown below. The transformer can supply high voltage isolation, thus allowing the analog switch to operate as a true isolated switch up to thousands of volts above ground.

The oscillator, buffer and control functions are all performed by a single hex CMOS Schmitt trigger. The oscillator is gated on or off from a CMOS compatible input signal controlling the input Schmitt trigger. The VN64GA's input capacitance acts as both filter and storage capacitor for the half-wave rectified oscillator control voltage. Turn-on time of the analog switch depends on the oscillator frequency and is typically 10 microseconds for a 1 MHz oscillator.

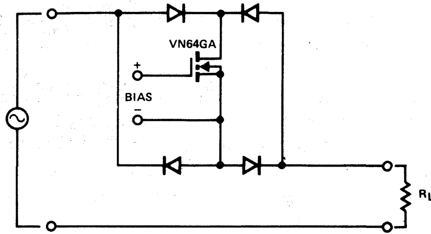
When the switch is on, JFET Q_1 is biased off by the negative supply D_1, C_1 and therefore has no effect on operation. When the oscillator is turned off, Q_1 loses its bias and turns on, thus shorting the VMOS gate to source for fast turn-off.



High Voltage Isolated Switch

A One-VMOS Analog Switch

Using four diodes in an array as shown allows using only one VMOS transistor for analog switching. Current flow is controlled keeping the source-base connection of the VMOS towards the load [the importance of this is stressed in AN77-2]. Be sure to use diodes capable of handling the load current and be sure to use a VMOS transistor whose breakdown voltage specification exceeds the peak analog voltage anticipated.



Operationally, by increasing the gate-to-source bias voltage the VMOS turns on. For applications other than either full on or full off, care must be taken not to exceed the dissipation of the VMOS transistor. A suitable heat sink cannot be overstressed in such applications.

Technical Article TA82-1

The Autobias Amplifier

A new topology for automatically biased audio amplifiers using power MOSFETs

ABSTRACT

An obstacle blocking wide acceptance of power MOSFETs in audio amplifiers is the lack of an automatic bias technique. A unique circuit topology senses and maintains quiescent current despite the half-wave pulses inherent in class AB operation. Performance of the circuit, consisting of little more than a differential amplifier driving a totem pole output, rivals that of more complex circuits.

INTRODUCTION

Vertical Power MOSFETs (VMOS) offer a number of significant improvements in the characteristics of interest for amplifiers as compared to their bipolar counterparts, namely:

1. **VMOS transistors are comparatively immune to second breakdown because no transverse current flow exists, as in a bipolar, to cause current concentrations. Therefore, no complex power limiting or protection circuitry is needed.**
2. **The temperature coefficient of transconductance is negative. Consequently, design of thermally stable circuits is easy and devices may be readily used in parallel for increased output current.**
3. **The transfer curve (I_D vs. V_{GS}) is linear over most of the operating current range of the transistor which produces a** low distortion output. Furthermore, the curvature which is present adheres approximately to a squarelaw, so that the resulting even-order products may be cancelled by a push-pull connection.
4. The capacitances are low which allows high frequency open-loop response. Also, FETs do not exhibit minority carrier storage time since conduction is solely by majority carriers. Consequently it is simple to build amplifiers which do not exhibit the various forms of transient distortions.

The chief problem in using VMOS is providing the proper biasing. The average gate voltage must be held a few volts positive with respect to the source, depending upon the current desired and the characteristics of the transistor, especially the threshold voltage. Unfortunately, threshold voltage not only shows a dependence upon temperature (approximately 6mV/°C), but is subject to lot-to-lot variations. Consequently, some kind of feedback scheme must be used to maintain the idle current despite variations on the order of 2 volts in the required gate voltage. The unresolved problem to date is how to sense the output idle current in the presence of the high current half-wave pulses which occur under class AB operation. The solution of this problem is the subject of this article.

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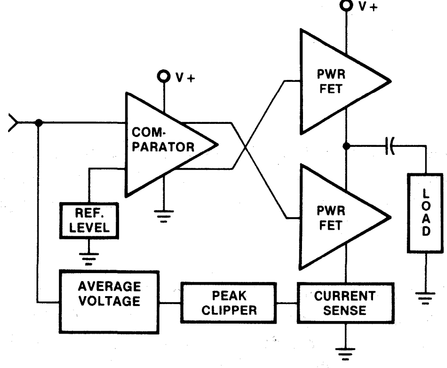
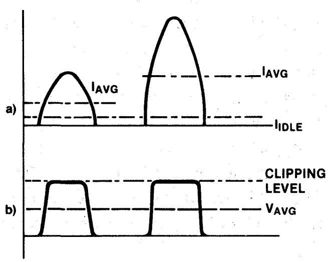
THE AUTO BIAS SCHEME

The method discovered which accomplishes biasing* is shown in Figure 1. In this scheme, the bias idle current is maintained by comparing the voltage obtained from the current sense resistor to a reference level. When the signal is large enough to cause cut-off of the current on negative half-cycles, thereby producing an asymmetrical waveform, the peak clipper and filter produce a voltage which is substantially the same as the zero signal level, regardless of the amplitude of the peak current. For proper operation, the dc level caused by the idle current must be set to one-half the level of the peak output from the clipper as shown in Figure 2. Note that the current waveform of Part A has an average level proportional to the peak current while the output from the clipper remains essentially constant as shown on B. Proof that this scheme really works will be given with the data obtained from the practical designs.



Automatically Biasing (Autobias) Scheme for Single Supply Class AB Amplifiers
Figure 1



Waveform of a) One Output Transistor Current and b) The Clipper Output. The Varying Average Level of the Current Wave Causes Negligible Shift in the Average Level of the Clipper.
Figure 2

GENERAL DESCRIPTION OF AMPLIFIER TOPOLOGY

The objective of this project was to produce a simple circuit which would fully utilize the advantages of MOSFETs and not require any adjustments. Consequently, a direct coupled scheme using complementary devices, so much in vogue with bipolar amplifiers, was rejected as being too complex, especially when a second differential amplifier to control the quiescent current would have to be added. In addition, p-channel FETs suffer from the severe disadvantage that holes are lower mobility carriers than electrons. The practical result is that to produce a p-channel FET with gain equivalent to a given n-channel FET, the die area must be about twice as large, causing a corresponding increase in capacitances and higher cost. The topology chosen is a direct implementation of the block diagram shown in Figure 1. As shown in Figure 3, the circuit using npn transistors and n-channel FETs consists of a differential amplifier driving a push-pull totem pole output configuration. The diff-amp controls the bias current of Q_4 which acts as a current source for Q_3. This arrangement necessitates a.c. coupling to the load even if a split supply were used because the voltage at the drain of Q_4 is affected by several component values.

Bias is accomplished by comparing the voltage drop across R_{21} to the voltage from the reference diode, D_1. To achieve accuracy in setting the bias, the dc resistance in the base circuits of Q_1 and Q_2 must be equal (i.e., R_{10} in parallel with $R_{11} = R_2 + R_{16} + R_{17}$ and the h_{FE} of Q_1 and Q_2 should be matched. Matching of V_{BE} is not important because of the drops across R_3 and R_4 and the base circuit resistance. Should the current in Q_4 tend to increase, the resulting drop across R_{21} coupled to Q_1 lowers its collector voltage (V_{C1}) which is coupled through R_6 to the gate of Q_4, thereby holding the current of Q_4 nearly constant.

Under large signal conditions, the high current peaks must be clipped and the waveform filtered. The best place to clip is right across R_{21}. Diode D_3 performs this function and also provides dynamic bypassing. In this location, power output is maximized, as the total voltage loss across the diode is only about a volt. Total harmonic distortion also is less with the diode in this position; apparently the decreasing diode incremental resistance with increasing current compensates for a nonlinearity in the VMOS. The diode introduces a generous number of low level high order harmonics, but a considerable reduction of the second and third harmonics occurs. R_{18} and R_{20} often can be chosen to achieve a minimum in the total harmonic distortion; their value determines the composition of harmonic content. R_{18}, R_{19} and D_2 balance both halves of the push-pull stage. At low signal levels, particularly when Q_3 and Q_4 are not well matched, R_{19} and R_{21} cause a reduction in even-order distortion products. The resistor R_{17} and diode D_4 form a second stage clipper which keeps the peak output quite constant regardless of the audio signal level across R_{21}. R_{16} and C_5 form a low pass filter to prevent the clipped waveform

*Patent pending.

from being mixed with the input audio which is also applied to the base of Q_1. Distortion increases considerably if C_5 is eliminated.

To provide maximum power output from a given supply, the dc level at the drain of Q_4 (V_{D4}) must be one-half of the power supply voltage (V_A) at full signal output. This level is controlled by the divider composed of R_{13}, R_8 and R_9. The level V_{D4} is thus determined by the fixed level placed on the gate of Q_3 minus the V_{GS} drop of Q_3, which usually is consistent within two volts from a given VMOS production line.

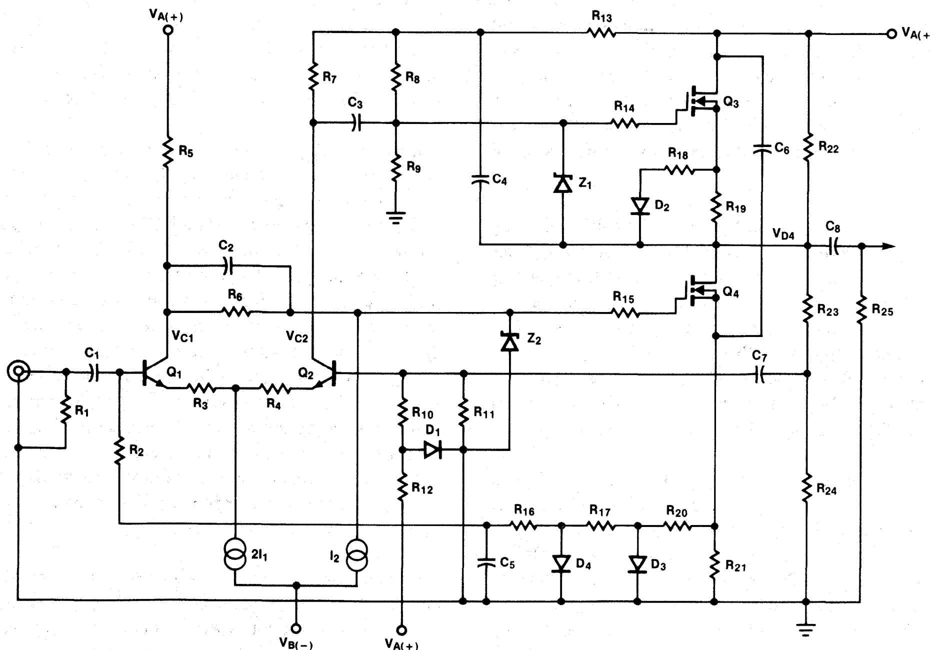
The differential amplifier acts as a voltage comparator to maintain the dc bias level and as a phase splitter to drive the VMOS output transistors. The interstage circuits are somewhat unusual. The load for Q_2 is R_7, but the signal from Q_2 must be referenced to the source of Q_3 since it is driven as a common source amplifier. This is accomplished by the bootstrap circuit R_{13} and C_4. To maximize R_7 for higher gain, R_{13} must be small, on the order of 1KΩ; this requires C_4 to be about 400 μF for satisfactory low frequency response.

Note that the divider composed of R_8 and R_9 is also bootstrapped by C_4 and R_{13} to provide benefits which are not generally obvious. The distortion is reduced slightly, but of more importance is the reduction of the turn-on current surge caused by charging the output coupling capacitor C_8. The time constant of R_{13} and C_4 determines the surge magnitude and duration.

The load resistors for Q_1 and Q_2 are R_5 and R_7, which should be matched for lowest distortion. The dc level at the collector of Q_1 is dropped by R_6 to the appropriate level at the Q_4 gate. Since current through R_6 is supplied by a low valued constant current source, negligible loss in dc gain occurs through the coupling network. However, capacitor C_2 is needed to prevent high frequency rolloff caused by the time constant composed of the input capacitance of the VMOS and R_6.

A feedback signal is developed by the R_{23}-R_{24} divider and applied to the base of Q_2 via C_7. Resistor R_{22} works with R_{23} and R_{24} to set the voltage V_{D4} to half of V_A during troubleshooting and these resistors also perform the function of a bleeder for the power supply filter capacitor. Resistor R_{25} insures that the output coupling electrolytic (C_8) has a charging current path should the amplifier be turned on with speakers disconnected. Feedback could be taken from a tap on R_{25}; this lowers distortion at low frequencies but overload recovery is poorer.

Since VMOS is not plagued by second breakdown, involved overload protection circuits are not required. However, gain does not decrease with operating current, so enormous output current could be developed into a short circuit load. To prevent this, the zener diodes Z_1 and Z_2 are used to prevent excessive gate drive. Although one diode per gate will limit the peak current, in some cases the circuit can cope better with large input signal overloads if two diodes are used in series. They should be chosen to allow equal positive and negative swings about the nominal idle gate voltage.



Basic Autobias Circuit
Figure 3

Since most VMOS devices have a cut-off frequency in the gigacycle range, parasitic RF oscillations can be troublesome. Most assemblies require an RF bypass C_6, on the order of 0.22 μF, physically connected as shown. In addition, R_{14} and R_{15} (100Ω or so) are included as parasitic suppressors. Ferrite beads could be used in place of the resistors. In either case, the suppressors should be mounted closely to the gate terminal. In addition, leads running to the gate terminal should be either shielded or used as a twisted pair with a ground lead.

DESIGN CRITERIA

In the simple circuit of Figure 3, primary tradeoffs occur between output slew rate, input impedance, matching requirements and bias point accuracy. For example, with a given pair of output transistors an increase of slew rate requires that the current in the diff-amp increases. The higher currents through the resistors in the base circuits of Q_1 and Q_2 produce larger voltage drops with a greater likelihood of an error in the output idle current unless the h_{FE} matching between Q_1 and Q_2 is tightened or the values of the resistors in the base circuit are proportionally reduced. If the resistors are reduced, then to preserve the low frequency response, capacitors, C_1, C_5 and C_7 must increase at an added cost which becomes significant if values over 1 μF are necessary, since it is desirable to avoid electrolytics.

The values of the components in the bias feedback loop from R_{21} to the base of Q_1 should be proportioned in a particular manner, since both bias and audio signals are present at the Q_1 base. A large signal which overloads the diff-amp disturbs the idle current setting. Best recovery was empirically determined to occur when the capacitor values for C_1, C_7 and C_5 are equal and R_2 is at least three times R_{16}. If C_5 is made proportionally larger, the point where low frequency distortion starts to increase can be made lower; however, the idle current recovery waveform begins to assume the character of a damped oscillation.

In order to prevent a significant portion of the dc level on C_5 from biasing the diode D_4, R_{16} should be at least twenty times R_{17}. R_{17} is chosen so that the clipped output voltage from D_3 sends a current through D_4 such that the peak level from D_4 equals twice the open circuit level at the base of Q_2. R_{17} should be large enough such that the peak level across D_4 is essentially constant regardless of the amount of current flowing through R_{21} and should produce the same current in D_4 as is flowing in D_1 when D_1 and D_4 are the same type diode.

Resistors R_3 and R_4 used in series with the emitters of Q_1 and Q_2 provide two benefits. The dc drops across them lessens the V_{BE} match required between Q_1 and Q_2. In addition, since the diff-amp will normally operate slightly out of balance, these resistors tend to balance the gain through both sides of the diff-amp. Choosing them to be about twice the junction incremental resistance (25 Ω/I_E(mA)) has yielded satisfactory results.

Because the load resistor for Q_2 is bootstrapped, the signal swing at the collector of Q_2 with respect to ground slightly exceeds the output peak-to-peak level which is close to the power rail voltage. Therefore, the quiescent level of the voltage V_{C2} must be above one half of the rail by at least 3 volts to avoid signal clipping or nonlinearity of the peak negative signal. Another 2 or 3 volts should be allowed for diff-amp unbalance. These requirements force the maximum value for $R_{13}+R_7$ to be $((V_A/2)-6)/I_1$, assuming that the current drawn by the R_8, R_9 divider is negligible. To maximize gain and prevent diff-amp current fluctuations from significantly influencing the voltage at the gate of Q_3, R_{13} should be small compared to R_7; however, the smaller R_{13} becomes, the larger C_4 must become in order to have adequate low frequency response and satisfactorily limit the turn-on current surge as C_8 charges.

R_5 must equal R_7 to keep the diff-amp in balance electrically. For thermal balance V_{C1} should equal V_{C2} by satisfying the equation $(I_1+I_2)R_5=I_1(R_7+R_{13})$. R_6 is chosen to place the proper gate voltage on Q_4 by consulting typical data for the particular VMOS being used.

The correct value for V_{G4} depends on the idle current required to minimize crossover distortion from the VMOS transistor. This is empirically determined and must be about 300 mA for the transistors used in the designs shown later. Using ordinary silicon diodes for the clippers yields a clipping level of 0.6 to 0.7 volts depending upon the diode characteristics. This dictates that the reference level on the base of Q_2 should be from .3 to .35 volts. If $R_{10}=R_{11}$ and D_1 and D_4 are the same type and operated at the same current, these requirements are met and a 1Ω resistor for R_{21} will set the idle level between 300 and 350 mA. To preserve the balance of the push-pull output, R_{19} must equal R_{21} and correspondingly, $R_{18}=R_{20}$ and $D_2=D_3$.

The value for R_{20} and R_{18} is empirically determined. If R_{20} is greater than twenty times R_{21}, its effect on distortion and power output is negligible; the output spectrum will be relatively free of high order harmonics but maximum power output will not be achieved. As R_{20} approaches the value of R_{21}, the "dynamic bypass" action becomes noticeable, power output increases and a marked reduction in 2nd and 3rd harmonics occurs. This results in a decrease of total harmonic distortion, but the output spectrum will have minute amounts of high order harmonics. The optimum value depends upon the VMOS characteristics as well as that of the bypass diode. A search for the optimum point is best done by operating the amplifier open loop, i.e. R_{24} shorted, and monitoring the output with a spectrum analyzer. The most acceptable spectrum is usually obtained with an R_{20} value slightly on the high side of that which yields the lowest THD.

The remaining network to be designed is that of the divider R_8 and R_9. It sets the output level V_{D4}. For symmetrical clipping, which yields maximum power output, the voltage at the gate must equal one-half the supply voltage at maximum power

output plus the nominal gate to source drop of the VMOS transistor and the drop across the source circuit network. The resistances can be in the megohm range, as the VMOS gate is essentially an open circuit. The value of C_3 is chosen to have negligible phase shift in the frequency range of interest. Overly large values for C_2 and C_3, however, improve overload behavior when the zener diodes conduct due to excessively large low frequency signals.

PRACTICAL APPLICATIONS

During the development of the autobias scheme, two practical amplifiers were designed. The first is a 25 watt version intended for home high-fidelity use, and the second is a 50 watt design of lesser power bandwidth intended for public address use.

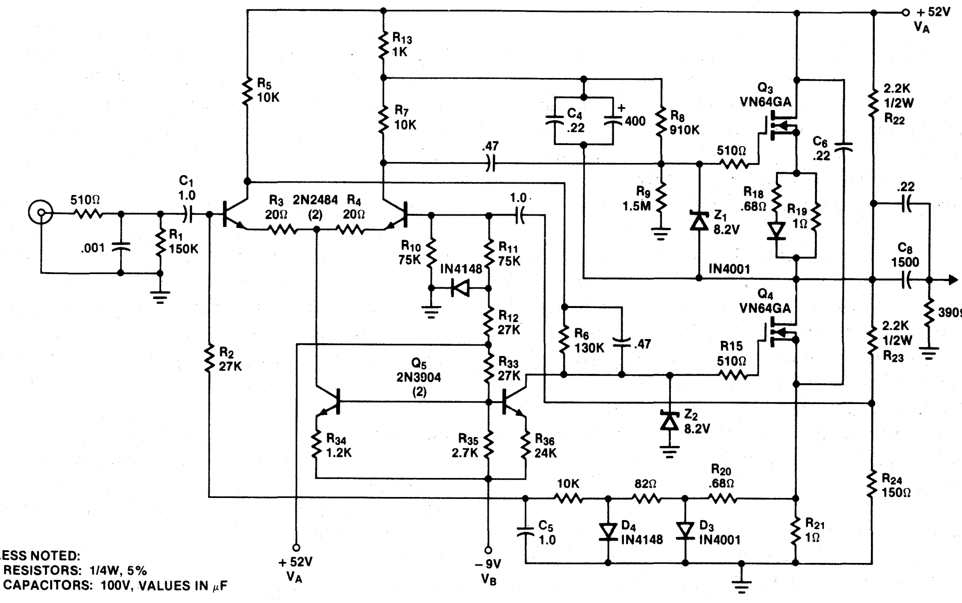
A 25 WATT DESIGN

Figure 4 shows a practical 25 watt amplifier. Transistors are used for the current sources shown in Figure 3. Base drive for these transistors is derived from the main power supply V_A, so that their collector current is proportional to the rail voltage. This feature holds the voltages on the diff-amp collectors close to $V_A/2$. The sensitivity of I_Q to V_A is about 3.4 mA/volt when V_B is held constant; the sensitivity of I_Q to V_B is -15 mA/volt when V_A is held constant. In a practical amplifier with a non-regulated supply, variations in power output will cause fluctuations in V_A, but will not affect V_B; therefore, having I_Q increase slightly with power output as discussed later will tend to compensate for the 3.4 mA/volt I_Q/V_A sensitivity. In the case of line voltage variations, since V_A is about five times V_B, the sensitivities tend to cancel, leaving a net sensitivity of about 2 mA/volt.

The circuit arrangement causes ripple cancellation to take place. Ripple from V_A is applied via R_5 and R_6 to the gate of Q_4. An out of phase ripple component is also applied to the gate via the current source Q_6. By properly proportioning the filter components of the supplies V_A and V_B, output ripple can be reduced to a level acceptable for most applications without the use of unduly large capacitors or an extra filter section connected between R_5 and V_A. The bootstrap capacitor (C_4) effectively filters the ripple from the gate of Q_3. The filter for V_A should be at least 5000 μF.

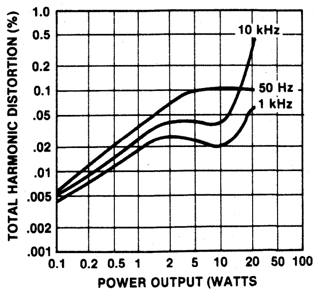
The sensitivity of the VMOS quiescent current, I_Q, to threshold voltage of the VMOS ($V_{GS(TH)}$) depends upon the loop gain of the bias stabilization portion of the circuit. With the components used in Figure 4, the sensitivity is about 16 mA/volt, which is felt to be satisfactory to accommodate the typical 2 volt tolerance of a VMOS production line.

It is not possible to measure the change in idle current level as the power output from the amplifier is varied using the usual sine wave test signal because the idle level is obscured by the output current. However, waveforms similar to the ones shown on Figure 5 can be fed into the amplifier; by viewing the voltage across R_{21} during the time of the zero level step, the idle level is visible. It is found that a fairly precise setting of the voltage across R_{21} is necessary if the idle level is to remain invariant with power output changes.

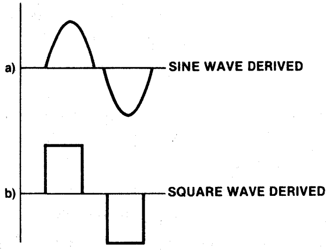


Practical 25 Watt Autobias
Figure 4

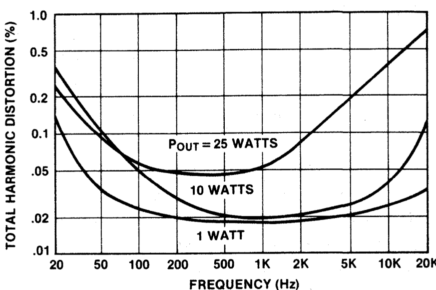
An increase of idle level with power output is a result of the average voltage output from the clipper and filter decreasing with signal level. The decrease results in the diff-amp raising the gate voltage to compensate for this apparent decrease in idle level. A small amount of this behavior is desirable in that it compensates for the decrease in idle level experienced as the supply voltage, V_A, drops due to increased audio power output. Should the clipper output increase with power output, the circuit will reduce the idle current level. This situation yields improved power efficiency, but the output may show evidence of cross over distortion at the higher power levels. For optimum performance, it is therefore necessary that the clipping level be maintained at slightly below twice the zero signal idle voltage from the clipper, regardless of the power output from the amplifier. The two stage clipper used is necessary to reasonably achieve this goal.



Distortion vs Power Output for 25 Watt Amplifier
Figure 6



Test Waveforms Used to Observe Idle Level Under Large Signal Conditions
Figure 5



Distortion vs Frequency for 25 Watt Amplifier
Figure 7

Identical tests were run on an amplifier at ambient temperatures of 25 °C and 45 °C. The current at all power levels dropped about 22 mA at 45 °C, a predictable result because the reference diode, D_1, has a temperature coeficient of 2 mV/ °C, which is divided in two by the resistors R_{10} and R_{11}. Distortion as a function of power output remained essentially unchanged at the test frequencies of 75 Hz, 1 kHz, and 5 kHz.

Figure 6 shows total harmonic distortion at selected frequencies as a function of power output and Figure 7 shows distortion at 1.0, 10 and 25 watts as a function of frequency. In the important mid-range, THD is under 0.1%. The increase in THD at high frequencies is caused by the extra drive required of the diff-amp to handle the VMOS input capacitance, while the increase at low frequencies is caused somewhat by the coupling capacitors, primarily the output capacitor (C_8), but mostly is attributed to the bootstrap capacitor (C_4), and the bias filter capacitor (C_5).

The usually published frequency response at 1 watt power output is not shown as it conveys little information. Response is down 1/2 dB at 19 Hz and 100 kHz when driven from a 1 KΩ source with the input filter removed.

The power efficiency calculates at 53% at the 25 watt output level. The power dissipation is essentially independent of frequency and varies little with power output. It is about 17 watts at idle and increases to about 22 watts at output levels from 10 to 25 watts.

Most assemblies show no evidence of slew rate distortion until at least 30 kHz when a slight crossover glitch appears on the waveform at a level of 15 watts or more. The glitch is level sensitive due to imperfect bias tracking as a function of power output. Bias tracking also becomes worse as the frequency increases, probably because of stored charge problems in the rectifier diodes used for D_2 and D_3. This tracking error would normally not be encountered on speech or musical signals.

Choice of suitable transistors for the diff-amp is limited. Good results have been obtained by using matched pairs of type 2N2484. The gain typically is about 400 at 2 mA and although the 60 volt V_{CEO} rating seems marginal, no problems have been expeiienced.

The output devices are Siliconix type VN64GA, which typically have a transconductance of 3 mhos, an $r_{ds(on)}$ of 0.3

ohms, and an input capacitance of 700 pF. These characteristics are needed in order to have sufficient gain in the current bias loop, good power efficiency, and wide open loop bandwidth.

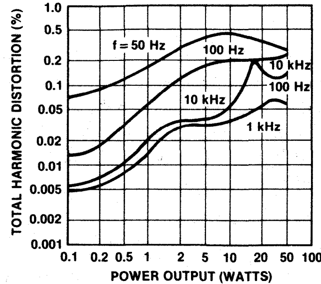
Some listening tests have been run using a variety of associated equipment. Most listeners notice improved reproduction of high frequency transients and have difficulty in detecting overloads and clipping unless excessive.

A 50 WATT DESIGN

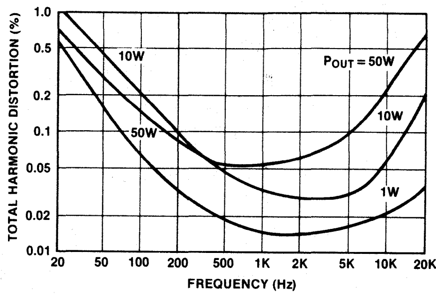
An amplifier designed to produce 50W into 8Ω is shown on Figure 8. For this application low distortion is only required over a range from 50 Hz to 10 kHz. It was adapted to use an available power supply which produces +78V and −52V under no load and nominal line conditions.

Figure 9 shows total harmonic distortion at selected frequencies as a function of power output and Figure 10 shows distortion at 1, 10, and 50 watts as a function of frequency. In the important mid range, THD is under 0.1%.

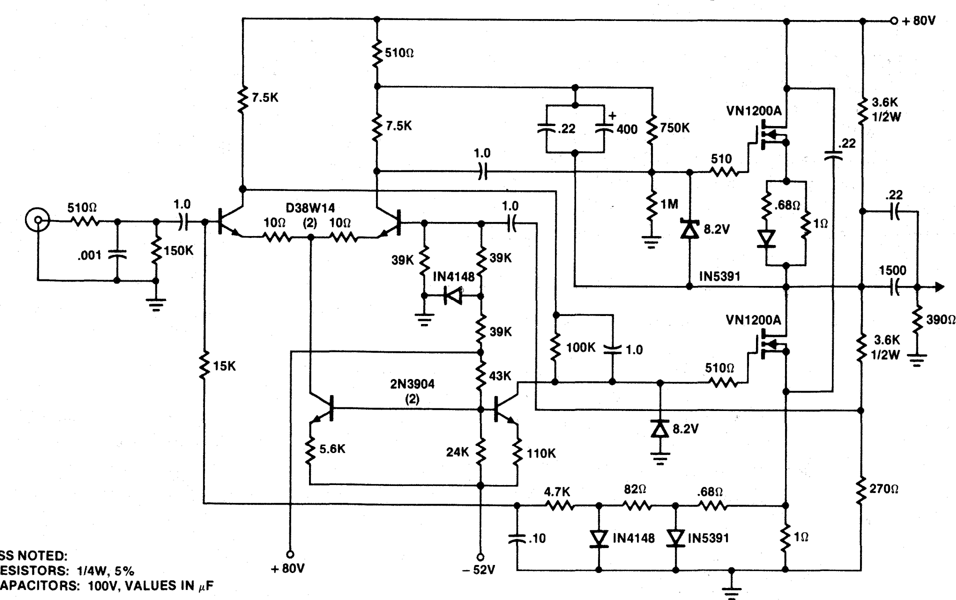
The narrower power bandwidth of the 50 watt amplifier as compared to the 25 watt amplifier is a direct result of the higher input capacitance of the higher power output devices. To avoid serious high frequency distortion the diff-amp current was increased from 2 mA to 4 mA; the higher current necessitated a 2:1 reduction in base circuit resistance in order to avoid an excessively tight match on the current gain of the diff-amp pair with the result that the bypassing action of C5, kept at 1 μF, is less effective at low frequencies. The narrower power bandwidth of the 50 watt amplifier does not reflect a significant difference in the frequency response at 1 watt as compared to the 25 watt design.



Distortion vs Power Output for 50 Watt Amplifier
Figure 9



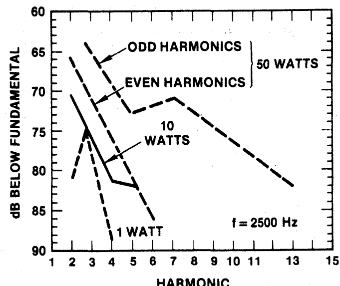
Distortion vs Frequency for 50 Watt Amplifier
Figure 10



Practical 50 Watt Autobias
Figure 8

Although not shown, data at 5 watts output is similar to that at 10 watts. The low frequency distortion is higher at these levels than at 50 watts because of the imperfect filtering action of C_5. Because of the clipper circuit, the voltage on C_5 is a larger percentage of the input signal as the output drops from the 50 watt level.

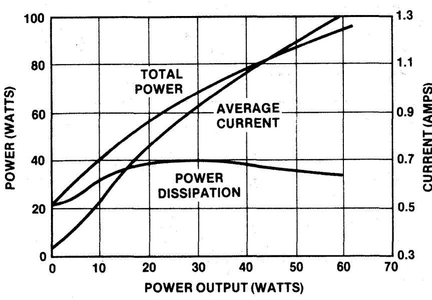
The harmonic distortion spectrum is shown on Figure 11. The dynamic range of the instrument used is 90 dB. Note that the third harmonic is prominent at all power levels. The even harmonics quickly disappear, but at the 50 watt level, odd harmonics up to the 13th were detectable. Probably none of these harmonics is discernable by ear.



Locus of Harmonic Spectrum
Figure 11

Power data is shown on Figure 12. The power efficiency calculates at 63% at the 50 watt output level. The power dissipation is essentially independent of frequency. The heat sink must handle about 40 watts of power.

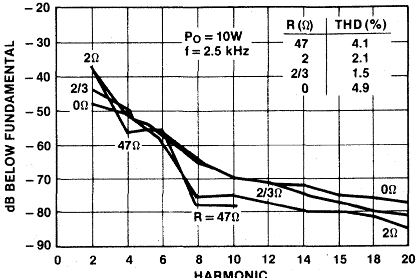
Finding suitable driver transistors for the diff-amp was not easy. The best transistor discovered to date is a D38W14 manufactured by General Electric. The transistor has $BV_{CEO} > 100V$, which allows ample voltage margin, and $h_{FE} > 400$ which places base current $< 10\ \mu A$ at 4 mA of collector current. Consequently, base current matching to within 1 μA is not too difficult and this match will produce a maximum error of 20 mV in the diff-amp which translates into a 20 mA error in the VMOS idle current.



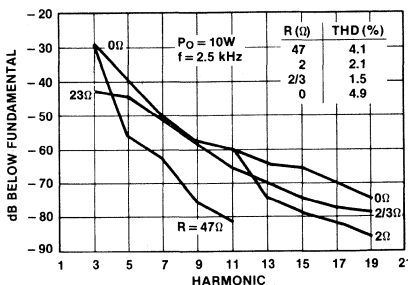
Power Requirements
Figure 12

The VMOS output transistors are VN1200As under development by Siliconix. They have 120V breakdown ratings, an "on" resistance under 0.2 ohms, transconductance of 5 Siemens, and an input capacitance of 1200 pF. This excellent combination of characteristics plays a major part in achieving the excellent results displayed by the simple autobias circuit.

Finally, Figures 13 and 14 illustrate the tradeoffs in open loop harmonic content as the diode series resistance is varied in the dynamic bypassing scheme. With R = 47Ω, the bypassing effect is negligible, and no harmonics past the 11th are discernable. As R is reduced, high order harmonics are introduced which increase in level. However, harmonics below the 6th minimize at various values of R. In the final amplifier design, 2/3Ω was chosen as it minimized the large 3rd harmonic resulting in lowest overall total harmonic distortion. By better matching of the push-pull configuration, it should be possible to reduce the even harmonics below the levels shown.



Open Loop Output Spectrum Even Harmonics
Figure 13



Open Loop Output Spectrum Odd Harmonics
Figure 14

CONCLUSIONS

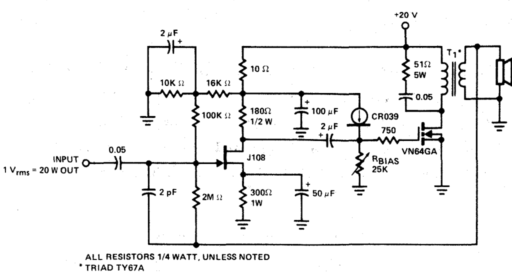
The circuit scheme presented illustrates that using VMOS transistors as power output devices produces an amplifier of extraordinary performance considering the circuit simplicity. It offers the following advantages over bipolar amplifier counterparts:

1. Only one driver stage
2. Simple overload protection
3. Stable bias point
4. Power efficiency independent of frequency.

20 Watt, Class A Audio Amplifier

Linear transconductance characteristics and low drive power requirements make VMOS ideal in low-distortion audio amplifiers. VMOS transconductance becomes linear at higher operating currents. This is in direct contrast to bipolar transistors which exhibit gain that changes significantly with changes in collector current.

The Class A amplifier shown delivers 20 watts into an eight ohm load using a single VN64GA driving a transformer coupled output stage. This circuit is similar to the audio output stage used in many inexpensive radios and phonographs. Distortion is less than 5 percent at 10 watts using very little feedback (3%) with the VN64GA biased at 3 amperes.

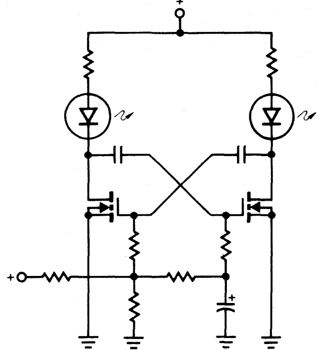


ALL RESISTORS 1/4 WATT, UNLESS NOTED
* TRIAD TY67A

Astable Flip-Flop with Starter

A pair of non-zenered VMOS transistors, a pair of LEDs and a simple RC circuit makes an easy sequential flasher with almost unlimited sequencing time – from momentary to several seconds.

The infinite input resistance of the VMOS' gate allows for very long sequencing times that are impossible when using bipolars. One precaution, though, don't wire your circuit using phenolic or printed circuit boards when you're looking for slow sequencing (they exhibit too much leakage!).

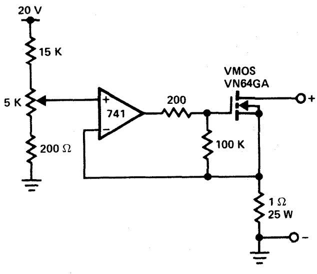


High Compliance Current Load

An op-amp, a VMOS power transistor and a high wattage resistor are all that it takes to make a superb constant current load with outstanding regulation.

Varying the load voltage from near zero to near breakdown the voltage variation across the 1 ohm load was unmeasurably low!

When implementing this circuit if your current range is moderate but your load voltage range is wide be sure to use a good heat sink and watch for excessive temperature rise.



Laser Diode Pulsers

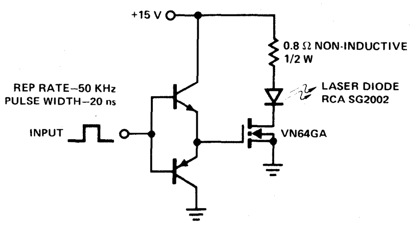
The VN64GA can switch 10 amperes in 10 to 20 ns when driven by a low impedance source. This extremely fast switching speed is excellent for driving high-current laser diodes and to modulate these diodes at very high frequencies. A typical 2 watt peak power laser diode requires a maximum 200 ns, 10 ampere pulse at a 0.1% maximum duty cycle.

The Laser Diode Pulser is a simple drive circuit capable of driving the laser diode with 10 ampere, 20 ns pulses. For a 0.1% duty cycle, the repetition rate will be 50 KHz. A complementary emitter-follower is used as a driver. Switching speed is determined by the f_T of the bipolar transistors used and the impedance of the drive source.

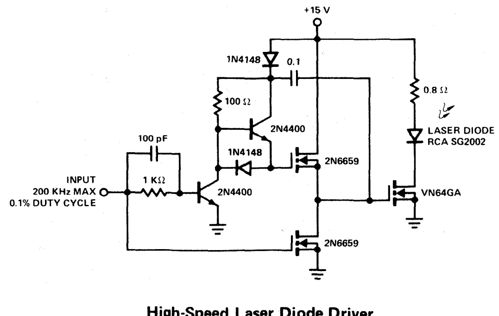
A faster driver circuit is shown in High-Speed Laser Diode Driver. It can supply higher peak gate current to switch the VN64GA very quickly. This circuit uses a VMOS totem-pole stage to drive the high power switch.

The upper VMOS is driven by a bootstrap circuit[1]. Typical switching times for this circuit are about 10 ns for both turn-on and turn-off.

[1] Siliconix Application Note AN79-4, "Driving VMOS Power FETs."



Laser Diode Pulser



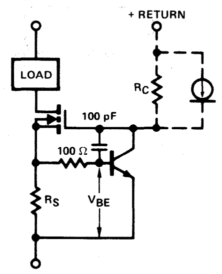
High-Speed Laser Diode Driver

Current Regulators

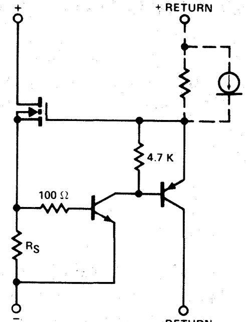
Current regulators find wide use as high impedance loads and current sources for differential amplifiers, zener diode references, and capacitors in timing circuits. FETs are attractive for use in current regulators because of their high output impedance and relative insensitivity to temperature variations. Use of VMOS devices permits higher current outputs to be achieved than possible with the more widely used junction FETs; however, some provision must be made to forward gate bias the VMOS transistor. The various circuits discussed show techniques of achieving current sources of different degrees of accuracy at the expense of increasing circuit complexity.

The simple current source shown below uses the base-emitter diode of a bipolar transistor as a reference voltage. The feedback action of the connection is such that the bipolar collector voltage – which is the VMOS gate voltage, forces the VMOS device to draw a current of approximately 0.65 volt/R_S. The collector resistor of the npn simply provides a bias for linear operation of the bipolar. This circuit is good from 30 mA to the maximum current rating of the VMOS transistor. The voltage rating of the circuit is that of the VMOS transistor. If the minus terminal of the circuit is to be grounded, the (+) return can be connected to a positive supply, rather than the load. This connection improves the current accuracy by diverting away the variable current flowing in the collector resistor, further improves the output impedance by preventing base-emitter voltage variation due to a variable collector current, and reduces the knee voltage required to obtain the required output current. Use of a current diode of the J500 family in place of the collector resistor provides superior performance, particularly when the return must be connected to the load.

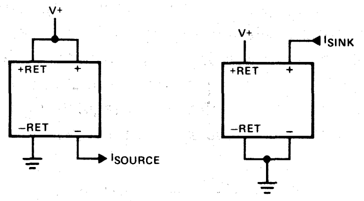
An improved current source results by adding a pnp transistor to increase loop gain and thereby improve the regulation of the collector current of the npn device. Both (+) and (–) returns are available for connection to a fixed supply in order to improve the accuracy of the output current. Techniques of using the returns for positive or negative current sources as well as a floating source are shown below the circuit diagram.

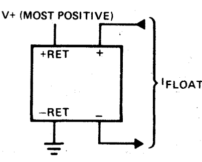


Simple Current Source



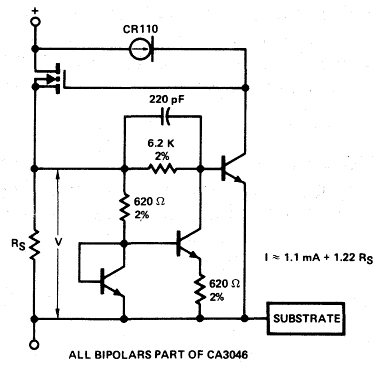
Improved Current Source





Connection of the Returns of the Improved Current Source for More Accurate Output Currents

The circuit below uses a band gap reference instead of a base-emitter junction for better temperature stability. It performs well as a two-terminal regulator without the need of returns.



Accurate and Temperature Stable Current Source

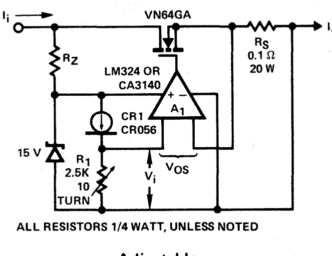
Current Regulators (Cont'd)

The circuit shown below is fully adjustable from less than 10 milliamperes to 12.5 amperes by R_1. Output current depends on R_S and the op-amp input voltage (V_i) by the relationship:

$$I_o \simeq \frac{V_i}{R_S}$$

Accuracy of this circuit depends mainly on the op-amp's input-offset voltage and on the stability of R_S. Digital current control is feasible if the designer employs a D/A converter to supply reference voltage V_i.

The circuit is configured as a two terminal regulator and must operate from a minimum of about 15 volts, to assure that adequate gate voltage is available for the VN64GA. By returning CR_1 and the A_1 power terminal to a separate 15 volt power supply, the circuit can regulate up to 12.5 amperes from a source voltage as low as 6 volts.

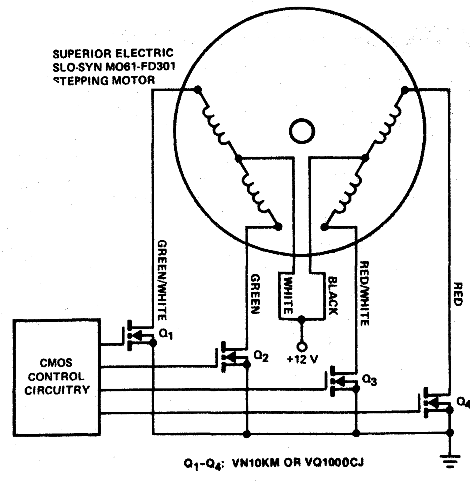


Adjustable

Stepping Motor Driver

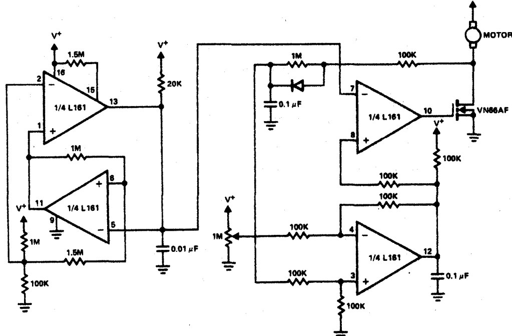
Stepping motors find wide use in disk drives and machine control. VMOS transistors are ideal motor drivers because of their freedom from second breakdown. The circuit shows how simple a motor drive becomes when using VMOS transistors. Note that snubbing networks are not used because load line shaping is not necessary with VMOS and the inductance of the motor is fairly low so that the inductive spike is small.

The VMOS gates are tied directly to the outputs of the CMOS control circuitry. The logic is arranged to sequence the motor in accordance with the needs of the application.



Constant Speed Motor Controller

DC motors enjoy wide usage in applications varying from electric trains to electric drills. In many applications a constant speed characteristic is desirable. This circuit uses VMOS and a single IC to achieve this speed control. One feature of this circuit is that no tachometer is required for monitoring the speed. Speed is determined by sampling the reverse EMF generated by the motor. Motor speed is controlled by pulse width modulation. Be sure only to use this circuit for DC supply rails because VMOS devices can only block voltage in one direction. If you want to operate from an AC supply, refer to the analog switch section of the handbook for AC switching techniques.



Voltage-to-Frequency Converter with Digital Line Driver

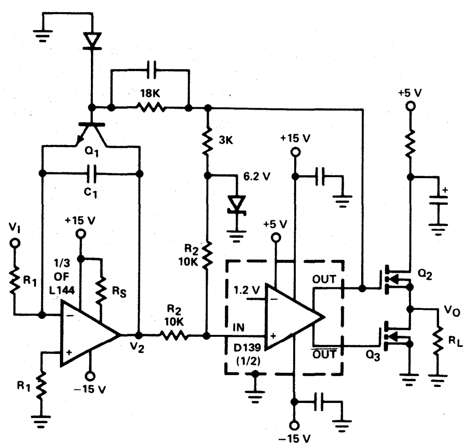
In industrial instrumentation systems, it is sometimes advantageous to amplify and digitize the transducer outputs at the physical location of the transducers. The data can then be digitally transmitted to a central computer location or terminal. A precision amplifier with digitally-controlled gain is excellent for amplifying the transducer signals up to the ±10 V level. A voltage-to-frequency converter (VFC) can then be used to convert the amplifier output voltage to a pulse train of variable frequency. A VFC provides an output frequency proportional to the average value of the input voltage over some specified range. The output pulse train can be transmitted over a single twisted pair for long distances without degradation of the data. In addition, the signal commons can be readily isolated if desired by coupling the output pulse train through an electro-optical coupler or pulse transformer.

Low-cost integrated VFC circuits are adequate for some applications, but are generally limited in output drive capability. Some also require numerous external components. The VFC circuit shown can provide good accuracy and can drive very long cables or low-impedance loads.

A two-channel FET switch driver, the Siliconix D169, is used as a comparator. The D169 comparison threshold is internally 1.2 V with V_R connected to ground and the complementary outputs both swing ±14 V when connected as shown. The ±14 V complementary output drives two VMOS transistors connected in a totem-pole configuration. The VMOS ON-resistance will be approximately 2 to 3 ohms with ±14 V of gate drive, so the output voltage V_O will swing between +5 V and zero even with a low-impedance load.

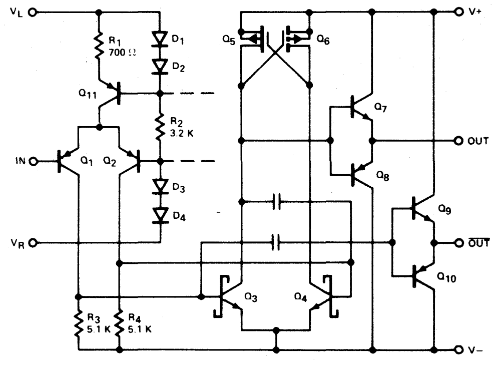
To visualize the circuit operation, assume that the integrator output V_2 is ramping positive in response to a negative input V_1. This circuit configuration requires that the input voltage be negative. The D169 output (OUT) is negative and transistor Q_1 is OFF. Since OUT is approximately −14 V, the 6.2 V zener will be conducting and the input to the comparator will be determined by the R_2 voltage divider. The voltage at IN, the D169 input, will be half of the integrator output V_2 minus half of the 6.2 V zener voltage.

When the integrator voltage ramps positive up to +8.6 V, the voltage at the D169 input will be +1.2 V and the comparator will trip. The OUT pin will suddenly go positive and thereby gate Q_1 ON which will reset the integrator. With the OUT pin positive, the zener-diode will conduct as a forward biased diode and the voltage applied to the input of the D169 comparator (IN pin) will be half of V_2 plus half of the diode drop (0.6 V). When the integrator output drops down to approximately zero during the reset cycle, the comparator will again trip and OUT will again go negative. Since the saturation voltage of Q_2 is much less than 1.8 V, we can be sure that the integrator will always ramp down sufficiently to trip the comparator. After resetting, the integrator will again ramp positive at



NOTE: ALL RESISTORS ARE IN OHMS UNLESS OTHERWISE NOTED.
$f_o = V_1 / R_1C_1\Delta V \quad -10 < V_I < 0$

Voltage-to-Frequency Converter

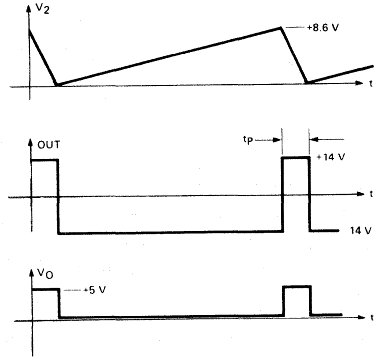


Logic	OUT	$\overline{OUT}$
0	V−	V+
1	V+	V−

D169 Switch Driver

Voltage-to-Frequency Converter with Digital Line Driver (Cont'd)

a rate set by the input voltage V_1. With OUT at −14 V, the zener-diode will again conduct as a zener and apply −6.2 V through R_2 to the D169 input. The VFC waveforms are shown for one cycle. The width of the positive 5 V output pulse is determined by the integrator reset time, which will be constant. The pulse repetition rate is directly proportional to the negative input voltage; higher input voltage causes the integrator to ramp positive faster and to thereby increase the pulse repetition rate.



VFC Waveforms

For a DC input of $-V_1$ and integrator output change ΔV, the output frequency will be determined by the integration time interval Δt. From $i = CdV/dt$, we have

$$\frac{V_1}{R_1} = C_1 \frac{\Delta V}{\Delta t}$$

Neglecting the short reset time, output frequency will be $1/\Delta t$ which is equal to $V_1/R_1C_1\Delta V$. The nonlinearity error caused by finite reset time, tp, is approximately $tp/\Delta t$ multiplied by f_0.

This basic VFC design can be easily tailored to specific design requirements by judicious choice of integrator op amp and component values. For example, using 1/3 of a Siliconix L144 triple op amp with a 120 K current-setting resistor provides a low current drain circuit capable of about 1.3 μsec reset time. A capacitor C_1 of 0.001 μF was used in one application along with an R_1 of 100 K. This made the full-scale frequency for a −10 V input equal to:

$$f_{MAX} = \frac{10\text{ V}}{100\text{ K} \times 0.001\ \mu\text{F} \times 8.6\text{ V}}$$

$$= 11{,}628\text{ Hz}$$

The other component values are not critical; an 18 K resistor to the base of Q_1 will be adequate and 3 K to the 6.2 V zener with R_2 of 10 K. For very wide dynamic range, a DG211 quad switch can be used to switch in different values of input resistor R_1.

The output can be taken directly from the complementary outputs of the D169 comparator/driver or from the totem-pole VMOS transistors. The VN35AK power transistors can readily drive a 50 ohm load with 5 V, one microsecond pulses.

Although this circuit requires two IC packages rather than one, it has many advanatages in flexibility. It can be designed for high-frequency operation, minimal power drain, or maximum output pulse power.

Siliconix

Technical Article TA82-2

MOSPOWER Semiconductor

AN HISTORICAL PERSPECTIVE

Edwin S. Oxner

Since MOSFETs were first introduced in 1975, no less than 17 suppliers now offer their own versions of MOSFET technology. The already dazzling array of power MOSFETs commercially available is complicated further as technological advances constantly produce new devices with improved performance. As a result, device specifiers can be overwhelmed when faced with the growing assortment of tradenames such as MOSPOWER, SIPMOS, HEXFET and so on.

Underlying this apparent state of confusion, however, is an orderly progression of technological events leading to the present marketplace profile. This article, the first of a three-part series, retraces the milestones leading to the ubiquitous MOSFET, and characterizes present technologies by noting their similarities and differences.

The Beginning

The forebearer of power FETs is not a MOSFET but a junction field-effect transistor (JFET). The development of the fundamental JFET that began with Julius Lilienfeld in the late 1920s and gained added momentum when William Shockley published his paper, "Unipolar 'Field Effect' Transistor," in 1952. However, despite the efforts of many researchers, this JFET disclosed by Lilienfeld and defined by Shockley, could not handle more than a few hundred milliamperes at modest standoff voltages.

The secret of greater power capability eluded researchers until the early 1950s, when several researchers, apparently working independently of each other, published the solution. Among these investigators were Nishizawa and Wegener.

The Problem: Two contradictory problems had remained insolvable for years. The first was the so-called "high-frequency" problem. In early JFETs, as device geometry increased in size to support increased current, parasitic capacitances increased faster and, consequently, the gain-bandwidth product decayed.

The second problem was channel resistance: It simply was too high. Planar, or laminar JFETs exhibited too much degeneration, transconductance was too low and parasitic capacitances too high. Paralleling device cells only aggravated the already poor figure of merit.

The Solution: Where Nishizawa buried his solution in a Japanese patent, Wegener publicized his findings in a 1959 paper entitled, "The Cylindrical Field-Effect Transistor." The two solutions were similar. Wegener postulated that current saturation in a cylindrical cross-section JFET (Figure 1), occurs at a lower pinch-off voltage than was possible for a planar or laminar JFET of equal transverse dimensions and equal saturation current (Figure 2).

The significance of this discovery was obvious. As pinch-off voltage drops, channel resistance likewise decreases. The result was less degeneration for higher transconductance, and smaller geometry for higher current and lower parasitic capacitances. The cylindrical cross section had thus solved both problems.

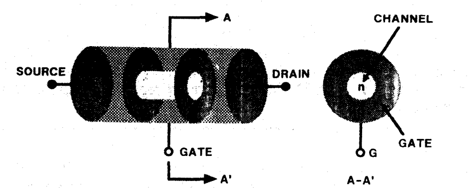


FIGURE 1. Cylindrical FET Concept was published in 1959.

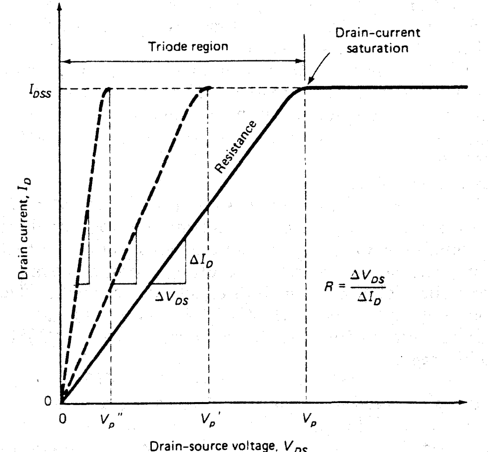


FIGURE 2. Curves depict the effect of channel resistance as pinch-off voltage is decreased, keeping I_{DSS} constant.

Early Power JFETs

Several researchers were already using the centripetal or cylindrical JFET concept in experimental devices when Wegener published his paper. Among these devices was Stanislas Teszner's Tecnitron (Figure 3) which was patented around 1956. However, the Tecnitron had limited power capability.

Soon after Wegener's paper was presented, Teszner published another paper in 1964 that described the Gridistor (Figure 4), a device that appeared to have solved the

Figure 1, 2, 4-9 reproduced with written permission from Power FETS and Their Applications, © 1982, Prentice-Hall, Inc.

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MOSFETs twenty years ago produced maximum resolutions of only about 5 microns. Consequently, planar construction using photolithographic masking required massive geometries to handle the current required for power applications.

FIGURE 7. The SIT (Static Induction Transistor) has a cross section similar to the MUCH-FET, and offers remarkable power handling capabilities.

The high parasitic capacitances associated with these large structures reduced MOSFET gain-bandwidth and speed. Other penalties of the large geometries were high channel resistance, excessive losses, poor thermal dissipation, high costs and poor yields.

However, in 1969, the Japanese Electrotechnical Laboratory unveiled their planar and V-groove double-diffused MOSFETs — both with underside drain contacts and with an insulated gate replacing the p-n junction. No longer dependent upon the limited dimensional accuracy of the photolithographic process, the power problem of MOSFETs had been solved.

Modern MOSFETs

The key to the problem was channel length. MOSFET channel length is inversely proportional to forward transconductance and proportional to on-resistance. Furthermore, the small geometry resulting from achieving a short channel also has lower parasitic capacitances. The double-diffused MOS (DMOS) FET was one of the earliest successful efforts in short-channel MOSFET technology.

The name "DMOS" for n-channel MOSFETs comes from the sequential manner in which the p-doped (body) diffusion is followed by a highly doped n+ source diffusion. The short channel results from careful control and placement of the second (n+) diffusion. The DMOS process has undergone continual refinement so that it is currently one of the major power FET technologies. There are two principle variations of vertical MOSFET structures.

Vertical DMOSFET

When early high-voltage DMOS devices with lateral structures became unduly large, their advantages were soon offset by the traditional drawbacks of large geometries. Consequently, suppliers resorted to vertical structures to restore chip size to the point where costs could match those of bipolar devices with similar ratings. All high-voltage, high-power DMOSFETs are now constructed with the source and gate located on the top of the chip and the drain on the underside, as shown in Figure 8.

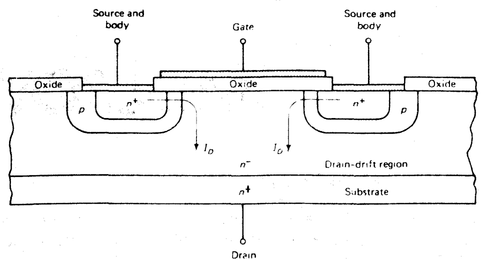


FIGURE 8. Power DMOSFETs employ this construction, and are now gaining wide use as they offer fail-safe operation in the enhancement mode (i.e. automatic shut-off after loss of gate drive).

VDMOS power FETs can withstand extremely high voltages with some device ratings approaching the kilovolt range. Operationally, there is little difference between the vertical structure and its planar or lateral equivalent. But VDMOS devices have a higher breakdown voltage, and smaller chip size results in higher yield.

V-Groove MOSFET

The other short-channel power FET can only be constructed as a vertical structure, Figure 9. Operating exactly as the DMOS device, a positive gate potential inverts the p-channel, resulting in an uninterrupted, low-resistance current flow between source and drain.

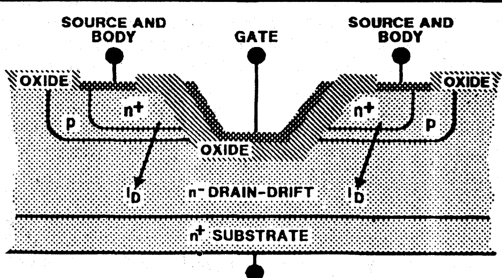


FIGURE 9. V-Groove Power MOSFET, also a short-channel device, operates exactly as a DMOSFET. This technology is generally limited to low voltage (less than 60 volts).

For the most part, silicon gate has replaced metal-gate technology in both DMOS and VMOS devices. However, metal gate is still used in high-frequency applications where the series resistance of silicon gate would be prohibitive.

Complementary power FETs (FETs of opposite polarity) operate in like fashion, except all voltage polarities are reversed. A p-channel MOSFET turns on with a negative voltage applied to the gate. There is growing interest in p-channel, enhancement-mode MOSFETs with short channels. However, since the mobility of p-doped silicon is considerably less than that of n-doped silicon, a true complement is impossible.

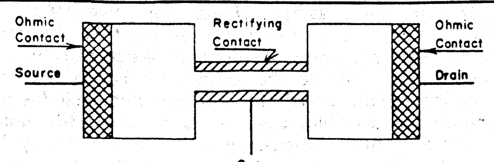


FIGURE 3. Tecnitron, shown in this simplistic cross-sectional view, was patented in 1956.

power problem. This development was closely followed by the appearance of Ranier Zuleeg's multi-channel field-effect transistor (MUCH-FET, Figure 5) in 1966.

The simplified cross section of a Gridistor (Figure 4) shows a grid of p-type cylinders (gate) imbedded in n-type material. This imbedded gate structure was characteristic of all the early power devices which, accordingly, were called junction FETs (JFETs) because the gate electrode is a p-n junction. Because the structure is similar to a basic npn bipolar transistor, either bipolar or FET action is obtained by manipulating gate bias voltage. Applying a negative potential to the grid operates the device as a FET. With a positive gate potential the structure takes on the characteristics of a bipolar transistor (Figure 6).

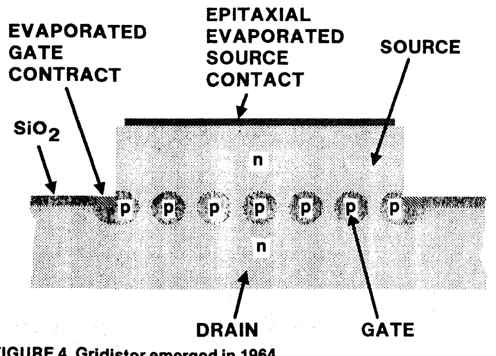


FIGURE 4. Gridistor emerged in 1964.

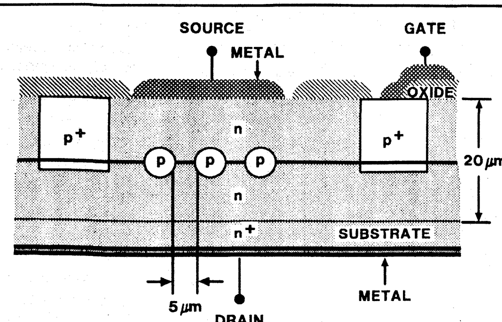


FIGURE 5. The MUCH-FET, a multi-channel field-effect transistor, was described in detail in 1966.

Unlike the planar or laminar JFET, Gridistor channel length is limited only by the diffusion process and is

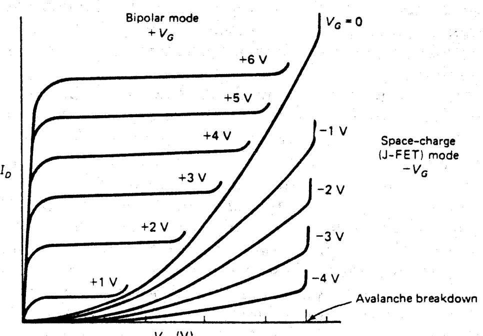


FIGURE 6. Output characteristics with negative and positive gate bias.

therefore, much shorter. Consequently, the channel does not pinch off as drain voltage increases, and drain current continues to increase as a function of drain-source voltage. This action results in output characteristics resembling those of a vacuum-tube triode.

The early Gridistor had two faults. Maximum forward transconductance was limited to about 200 μmhos for a single channel (regardless of size), and single-cell devices had limited power dissipation.

These drawbacks were overcome by Zuleeg's MUCH-FET, which was basically a multicell Gridistor with high forward transconductance, high thermal dissipation and high current-handling capability by virtue of the parallel-connected cells. The MUCH-FET was designed specifically for high-frequency, high-power operation. Early devices achieved 2 W at 100 MHz.

However, as with the Gridistor and other depletion-mode JFETs, the MUCH-FET required two power supplies: one for the drain-source voltage and the other for bias. Bias must be of opposite polarity from that of the drain-source potential to ensure that the FET can be turned off. Nevertheless, the MUCH-FET made a significant contribution to the technology in that it was the first device to be fabricated vertically, as is practically all other power FETs presently on the market.

While the Gridistor and MUCH-FET were being developed, the Japanese were quietly perfecting an analog field-effect transistor called SIT (static induction transistor). This device (Figure 7) has a cross section similar to that of a MUCH-FET, and has remarkable power-handling capabilities at high frequencies.

Like the MUCH-FET, the SIT has a very short channel and exhibits a nonsaturating drain current similar to that of a vacuum tube or space-charge-limited triode. However, the device can also withstand high drain-gate voltages. Among other benefits arising from this characteristic, lower parasitic drain-gate capacitance allows operation at higher frequencies. Consequently, the depletion-mode SIT has been used successfully in applications ranging from high-fidelity audio amplifiers to high-frequency power amplifiers.

Thus, power FET technology appeared to be the exclusive domain of JFETs as the decade of the 1960s drew to a close. Technical problems had frustrated earlier attempts at fabricating power MOSFETs. For example, photolithographic techniques for building

(Continued on following page)

Generally, a match is based upon on-resistance and transconductance, but at the cost of unbalanced capacitance. Consequently, a p-channel power FET in CMOS applications needs a heavier drive than its n-channel counterpart.

Most commercially available power MOSFETs fall into one of two categories — VMOS and DMOS. Within each category, cell construction is the same and performance characteristics are very similar. The emergence of different trade names (e.g., MOSPOWER from Siliconix; SIPMOS from Siemens; HEXFET from International Rectifier) reflect differences in surface geometries, which don't appreciably affect power MOSFET performance. Accordingly, the power system designer specifying power MOSFETs should not be confused by different trade names. Instead, he should focus his effort on evaluating actual power MOSFET performance against the manufacturer's published specifications.

As newer trade names proliferate within the family of power MOSFETs, they are expected to follow the short-channel concept. Barring some unforeseen and dramatic technological breakthrough, understanding the structure and operation of a basic cell means understanding them all.

INDUSTRIAL APPLICATIONS

Industry is increasingly relying upon power MOSFETs for more efficient conversion of raw electrical power to forms more suitable for energizing electrically driven products. This article, the second of a three-part series, examines the role of MOSFETs in two principal industrial applications: switching power suppies and electric motor controllers. In this discussion, efficiency is not only the ratio of power output to power input, but it also relates to switching speed, ease of applications, and system size, cost and simplicity.

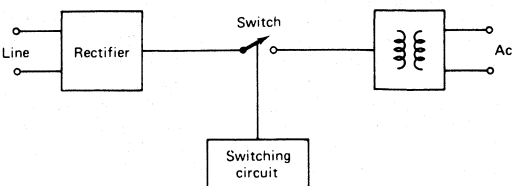


FIGURE 1. Block diagram of a basic inverter circuit

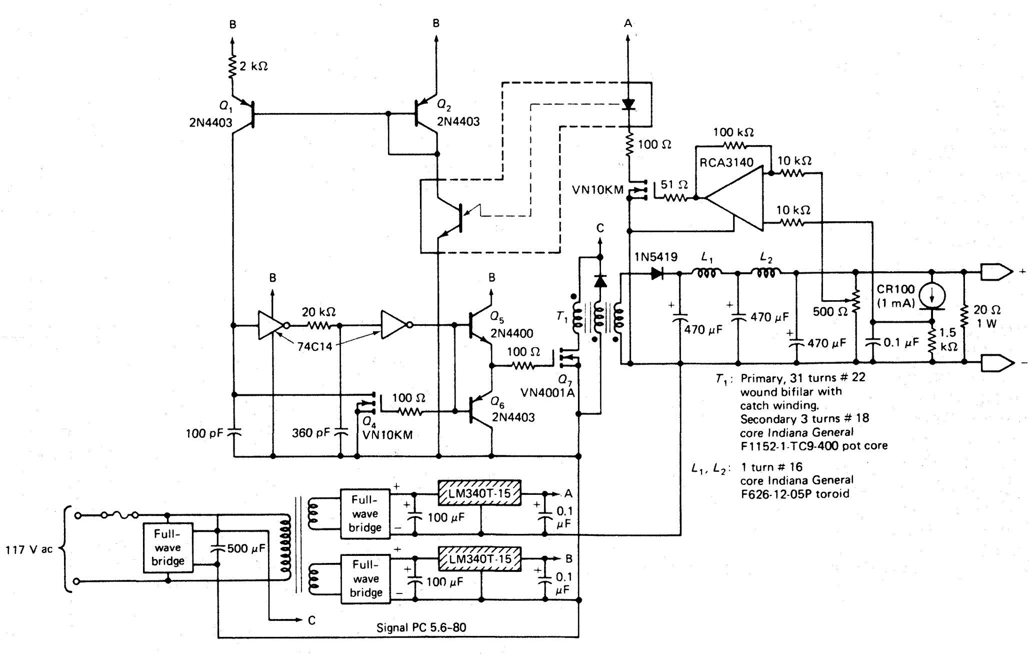


FIGURE 2. Flyback regulator circuit for supplying 5V, 10A microprocessor power.

Switching Power Supplies

A basic inverter is little more than a DC to AC energy converter consisting of an input rectifier followed by the switching circuit and output transformer, Figure 1. The high-voltage capability of power FETs allows considerable design flexibility when applied to the switching circuit of an inverter. One commonly used approach that has low parts count is the flyback switching power supply, often economical for low-power applications.

The circuit shown in Figure 2 can be used to supply 5V at 10A for microprocessor operating power. The use of off-the-shelf ICs for all critical functions greatly simplifies design and construction. For example, an operational amplifier (RCA3140) compares the output voltage against a reference and controls the light output of an optocoupler which sets the current level. This current, in turn, establishes the operating frequency of the 74C14 Schmitt hex inverters that drive the gate of the power FET. An emitter-coupled drive lowers the drive impedance and reduces switching time.

Pulse-Width Modulation: One of the most efficient ways to drive power FETs is to use pulse-width modulation (PWM). Here, the drive frequency is fixed, but pulse on and off times are variable. The result is a sinusoidal waveform whose shape depends on the number of pulses in a cycle and their spacing. Half-bridge and full-bridge circuits are capable of delivering power limited only by the current-handling capability of the switching transistors.

If transistors are connected in parallel to increase output current, they must be switched off in unison to avoid excess switching losses. Partly because of the positive temperature coefficient of MOS transistors, the threshold voltages of paralleled power devices need to be matched only to within 10%. However, ferrite beads or 30 to 50-ohm carbon resistors should be inserted in series with each gate lead to prevent unwanted parasitic oscillations. Also two paralleled devices should share the same heat sink.

Half-bridge and full-bridge switchers use power FETs stacked in a totem-pole configuration so that the MOSFETs do not have to withstand full operating voltage. One method for driving a half-bridge MOSFET total pole is shown in Figure 3a, where a single input controls the action of the two output transistors. Another method uses an isolation transformer to drive one transistor of the pair, Figure 3b. For high-frequency operation the isolation transformer driving the MOSFET gate can be a small pulse transformer driven by complementary emitter-coupled bipolar transistors.

A full-bridge totem-pole circuit is shown in Figure 3c. In this circuit the transistors are switched on and off to produce alternating current flow through the cross-leg containing the main transformer. The pulse transformers can be simply constructed using trifilar wire wound on ferrite bobbins. This circuit should be ale to switch at frequencies exceeding 200kHz.

An example of a dimple half-bridge switcher is shown in Figure 4. This circuit includes a pair of 400V power MOSFETs in a totem-pole arrangement and triggered from a commercially available integrated circuit for

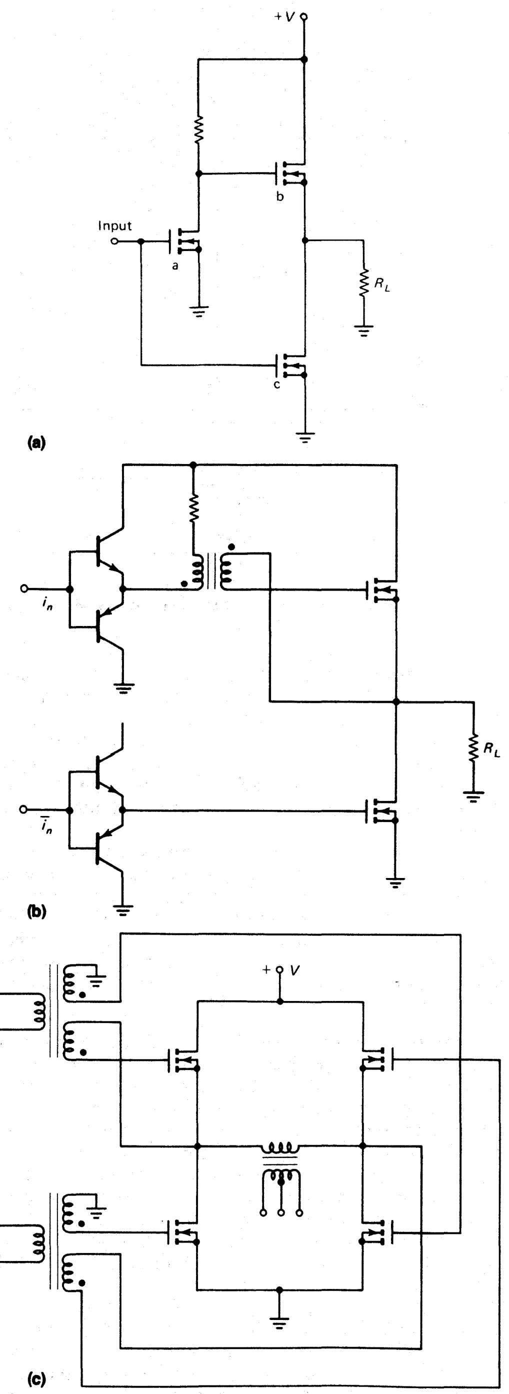


FIGURE 3. Power MOSFETs in half-bridge totem-pole, a and b, and full bridge totem-pole arrangements, c

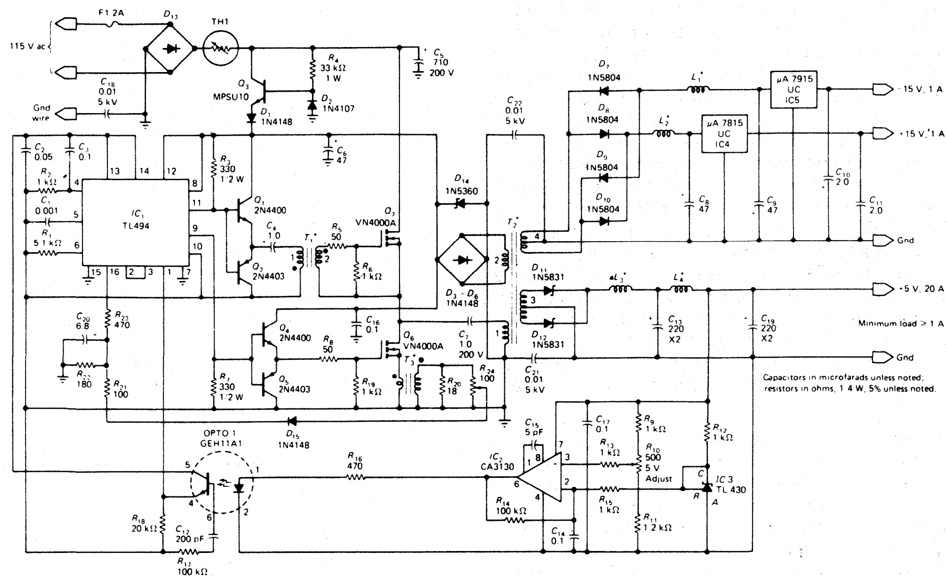


FIGURE 4. Half-bridge switching power supply using 400V power MOSFETs to deliver 150W at 100kHz

operating frquencies of 100kHz and higher. Pulse transformer T_3 and diode D_{15} provide automatic shutdown if drain current through the totem-pole power MOSFETs rise to a level exceeding the setpoint established by potentionmeter R_{24}. Thermistor TH_1 following the input rectifier bridge provides a soft-start feature, and IC_4 and IC_5 are voltage regulators for low to moderate output power.*

Power MOSFETs used in totem-pole switchers can have lower breakdown voltage ratings since each transistor is subjected to only half the total voltage. On-resistance should be equal to or less than 1 ohm. Using parallel transistors to boost output power, of course, further reduces effective on-resistance. Decreased on-resistance means lower power loss ($I^2R_{DS(on)}$) and, consequently, lower temperature rise of the MOSFETs.

Contrary to general belief, catastrophic failure can also result from thermal runaway. True, MOSFET on-resistance increases with increase in temperature and tends to limit current. However, if drain current is set or controlled by an external force or load (or a short circuit), I^2R losses increase as the device heats up. The result appears no different from thermal runaway. Consequently, a critical part of switcher design is guarding against thermal runaway by first determining device junction temperature and then sizing the heat sink to ensure that the junction temperature is not exceeded under normal operating conditions.

The thermal design of a switching power supply involves procedures which are beyond the scope of this article. However, several thermal-dissipation and heat-sink problems can be solved graphically by using curves normally found in MOSFET data sheets. Therefore, make sure the vendor's data sheet contains a plot of normalized $r_{DS(on)}$ versus junction-temperature (T_J). Also, make sure that the thermal resistance between the heat sink and ambient is available from the heat-sink supplier.

Another point is worth noting with regard to heat sinks. Insulating a MOSFET from a heat sink adds stray output capacitance in parallel with the common-source output capacitance (C_{oss}) of the device. For example, a mica or thin plastic insulating washer for a TO-3 package adds nearly 200pF and a 0.062-in. beryllium-oxide washer, 25pF. The result can be increased turn-off time.

The other two critical areas of high-speed switcher design are the circuit board and the main power transformer fed by the power MOSFETs. It is recommended to use a high-quality material for the circuit board. Short-lead, point-to-point wiring is mandatory, and ground connections are critical. Plated, through holes should be used, and pulse-carrying leads running an appreciable distance should have reasonable separation. Transformer

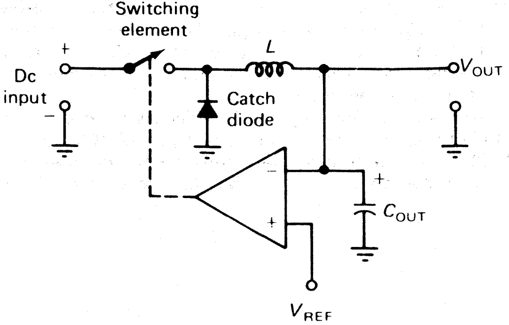


FIGURE 5. Simplified circuit of a basic regulator

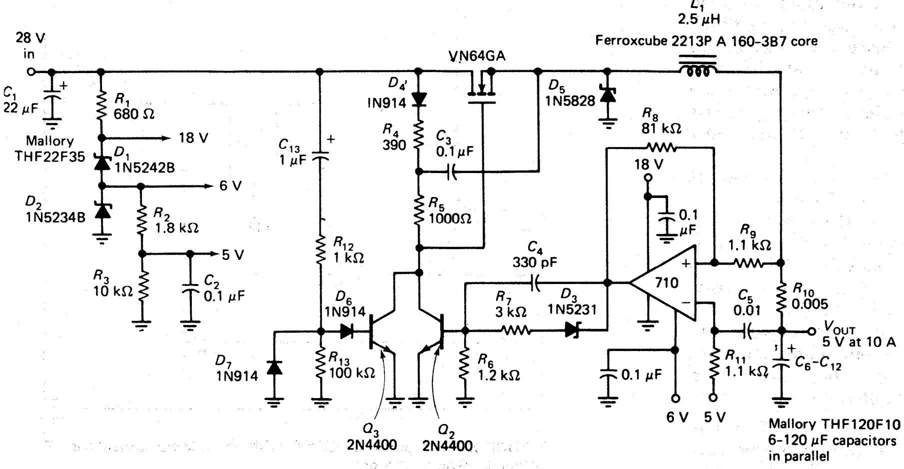


FIGURE 6. Switching regulator operating at 200kHz

design is even more critical and should be based on practices described in available technical literature.

Regulators

Regulators differ from switchers in that they provide highly regulated direct current from a poorly regulated or poorly filtered DC source. In this application the power MOSFET is usually a series regulating element. A basic regulator operates by comparing the output voltage with a reference and generating an error signal to control the series-pass regulator transistor, either directly or by PWM, Figure 5. When using power FETs as series regulators it is advisable to use an overcurrent shut down to protect the power FET from excessive I^2R losses.

If the switching element is closed, direct current flows from the source through the load and catch diode.

A voltage regulator includes a circuit connected across the output to close the switch upon sensing a voltage drop. The degree of regulation (ripple) due to the recurring voltage drop depends on the sensitivity and slew rate of the feedback network.

Adding a few refinements to the basic regulator of Figure 5 provides a regulated DC with less than 100mV of ripple for microprocessor applications, Figure 6. Necessary operating voltages are taken from the bleeder resistor network connected across the unregulated 28V supply. A soft startup feature clamps the series VMOS switch off until the supply has stabilized. The output of the LM710 comparator, which is actually an oscillator running at 200kHz, is fed through a level-shifting circuit to the base of bipolar transistor Q_2. This transistor is part of a bootstrap circuit necessary to turn the power MOSFET full on in totem-pole MOSFET arrays.

Current Regulator: The principal advantages of using a power MOSFET as a constant-current regulator stem from its very high output impedance, which provides exceptionally stable current over wide voltage fluctuations, and its minimal sensitivity to temperature variation.

Unlike in switcher applications where power MOSFETs operate in their triode mode (low $r_{DS(on)}$), devices used as current regulators operate in the saturation region or high $r_{DS(on)}$. Consequently, adequate heat-sinking is critical for avoiding excessive temperature rise.

The basic circuit of Figure 7a is a current sink. The operational amplifier compares the voltage across the low-ohmic, high-wattage resistor with a reference voltage, which can be supplied by a potentiometer, a zener diode or a D/A converter. Accuracy is a function of sense resistor stability, amplifier offset and reference voltage stability. This circuit is especially useful as a constant-current load and, with the addition of a D/A converter to supply the reference voltage, can be designed for digital current control.

The circuit in Figure 7b can be used as either a current sink or a two-terminal regulator. The latter connection regulates current levels from a few milliamperes to the maximum current allowed by the power MOSFET used.

Motor Control

Power MOSFETs are expected to make deeper penetration into the field of electric motor control as power-handling capability continues to increase. Traditionally,

Because of high motor starting current, the MOSFET should have a low $r_{DS(on)}$ to avoid high device losses and excessive temperature rise and to minimize effective V_{SAT}. Also, if the motor stalls, a low $r_{DS(on)}$ is less likely to cause thermal runaway.

Possibly one of the easiest power MOSFET applications in motor control is for brushless stepping motors, Figure 9, particularly since the MOSFETs can interface directly with computer logic. Additionally, the inherent parasitic source-drain p-n diode eliminates the need for free-wheeling diodes and snubber networks.

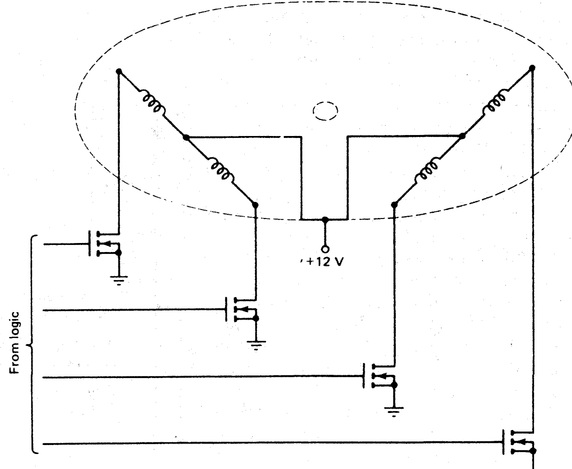


FIGURE 9. Using power MOSFETs with direct logic control for driving a stepping motor

AC Motor Control: The typical AC induction motor controller is basically an inverter that changes DC power into a variable frequency, usually by pulse-width modulation. This technique is commonly used because it produces a low harmonic waveform and maintains a constant voltage-to-frequency ratio, which avoids field-winding saturation and possible motor damage.

PWM control of an AC induction motor is obtained by properly sequencing a pair of power MOSFETs arranged in a totem-pole configuration, Figure 10. The amplitude of the resultant sine wave is proportional to the width and phase of the pulses. The number of pulses per half cycle can be fixed with only the width varying, or the number of pulses can increase with pulse period with pulse width varying for voltage control. In practice, variations of these two basic approaches are found in a variety of industrial applications.

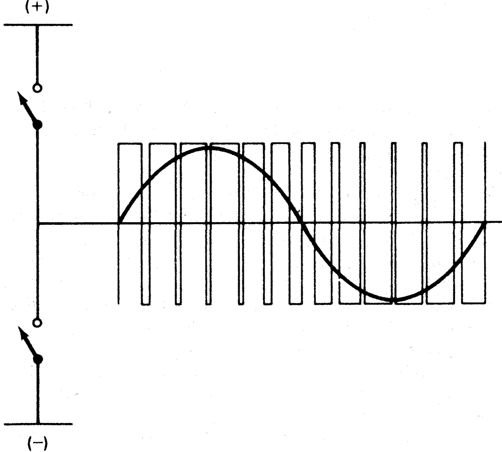


FIGURE 10. Pulse-width modulation generated by a totem-pole switch pair

The heart of any PWM controller is the generator that synthesizes the sine wave. Figure 11 shows the use of an op amp, such as a 741 or LM356, as the basic building block. The control signals are a sawtooth waveform fed to the inverting (−) input and a DC voltage fed to the noninverting (+) input. The resultant output is a series of pulses whose frequency depends on the frequency of the sawtooth input and whose pulse width depends on the level of the DC input voltage.

Application Tips

Successful power MOSFET application requires operating the device within the safe operating area (SOA) defined by a plot of drain current versus source-drain voltage. In order to comply with this constraint, which is provided on the device's data sheet, a MOSFET driving certain types of loads requires protective measures.

Inductive Loads: When a power MOSFET driving an inductive load is turned off, the collapsing magnetic field around the inductor induces a counter EMF that could exceed the breakdown voltage of the MOSFET. One way to avoid this effect is to shunt the inductive load with a resistor and a fast diode, Figure 12. To ensure fast response to the transient-voltage spike, the use of a gold-doped diode is recommended.

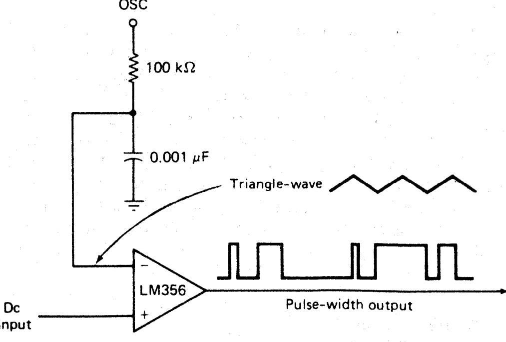


FIGURE 11. PWM waveform generator for driving the power MOSFET gate

thyristors have dominated these applications because of their ruggedness and low cost— particularly for DC motor control. DC motor speed is controlled by controlling armature voltage, and torque is controlled by controlling armature current.

One member of the thyristor family, the silicon controlled rectifier (SCR), has several merits for this application. First, current and voltage are controlled simply by adjusting the firing angle of the device. Second, an SCR acts as a rectifier, which is an advantage when operating a DC motor from an AC power source. Finally, SCRs can withstand high surge currents and very high voltages.

On the other hand, SCRs require commutating circuits to turn them on and off when operating off a DC power source. Another basic problem results from high-speed switching of high current and voltage. Exceeding the dV/dt and di/dt ratings of an SCR could result in false triggering and device overheating.

In AC motors, speed is dependent on the frequency of the AC power source rather than voltage. Moreover, torque is relatively constant until the motor stalls. AC motors are often preferred over DC motors because they are smaller, less costly and are more reliable. However, their application range has been restricted by the lack of cost-effective speed controllers. Because most AC motors are designed to operate on sine-wave inputs, the harmonic-filled waveforms generated by SCRs would cause serious motor overheating.

These SCR shortcomings leave several avenues open to the power MOSFET in DC and AC motor control. Heavy industrial DC motors of several hundred horsepower are certainly beyond the power-handling capability of present MOSFET technology. However, power MOSFETs are an attractive alternative for controlling small DC motors. An equal if not greater opportunity exists in AC motor controllers where power MOSFETs can be used to synthesize relatively smooth sine waves for cool motor operation. And in some controller applications, power MOSFETs are the only practical solution.

DC Motor Control: Power MOSFETs are unquestionably better than SCRs for controlling DC motors from direct-current lines. An example of this application is the control of DC motors in automotive electrical systems, Figure 8. This circuit is part of a microprocessor-based DC motor controller using a D/A converter to provide a speed-setting reference voltage. The L161 quad op amp performs several functions. Op-amp comparators a and b generate a triangular waveform for the input of op amp comparator c, which biases the MOSFET gate.

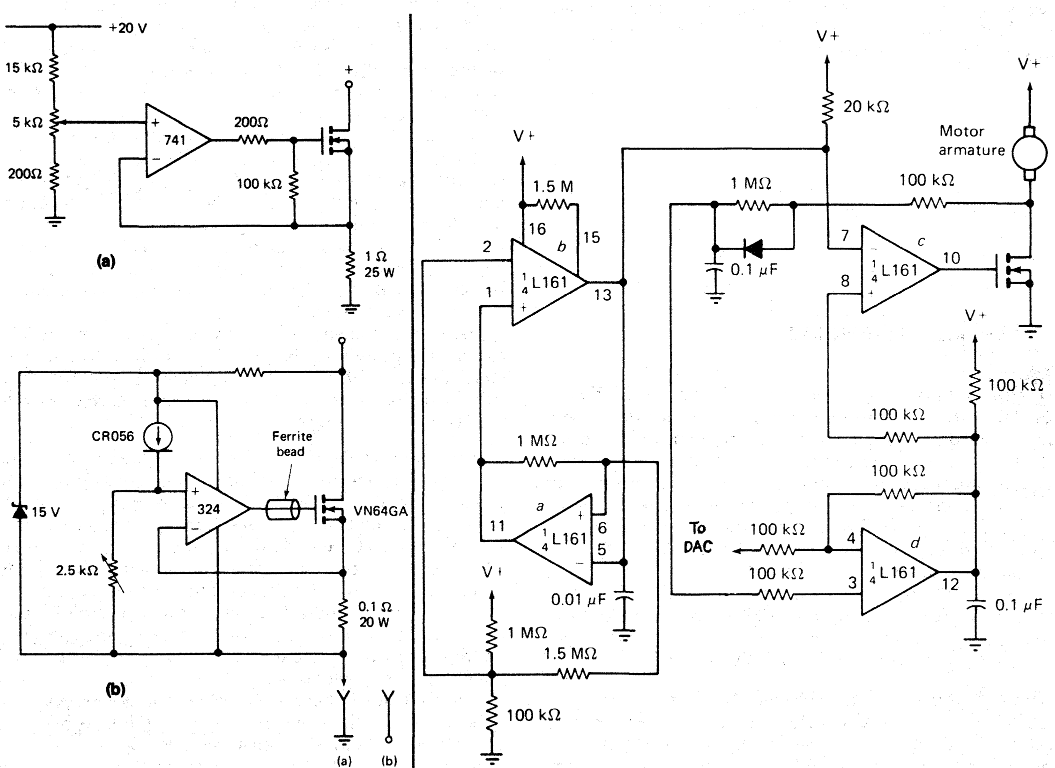


FIGURE 7. Power MOSFET in a basic current sink circuit, a, and a two-terminal regulator with a sink option, b.

FIGURE 8. Power MOSFET in a constant-speed DC motor controller

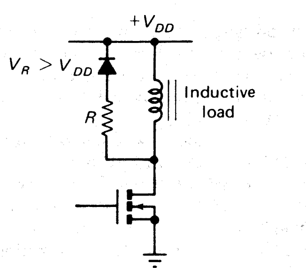


FIGURE 12. Free-wheeling diode for diverting inductive transients from a power MOSFET

Another effective protective method— especially suited when working "off line" either directly or with isolation or step-down transformers— is placing a zener diode across the MOSFET. This device has picosecond response time and also protects against line-voltage transients which can be twice the line voltage.

Capacitive and Lamp Loads: An uncharged capacitor appears as a short circuit when voltage is first applied to it. The result is high inrush current through the MOSFET. A similar condition is presented by incandescent lamp loads whose "cold" resistance is only a fraction of that when the lamp is hot. In these cases gate voltage must be high enough to ensure the MOSFET operates in its ohmic region. At the same time, this voltage must not be ramped up slowly. Otherwise, high $r_{DS(on)}$ at low gate voltage might lead to thermal runaway.

NEW APPLICATION FRONTIERS

N-channel, enhancement-mode power MOSFETs with low threshold-voltages interface easily with logic-level drive circuits. As a result, these power-switching devices are used increasingly with digital-logic circuits controlling substantial amounts of electrical power. But dramatic increases in speed, power-handling and thermal capabilities promised for next-generation power MOSFETs will also thrust them into application areas traditionally served by other power-switching devices.

This article, the final of a three-part series, discusses techniques for driving power MOSFETs with digital logic circuits and examines new application possibilities awaiting imminent advances in MOSFET technology.

Driving Power MOSFETs With Logic Elements

DTL, RTL, TTL and CMOS circuits can drive power MOSFETs directly, provided their high and low-state output voltages and current-handling capability are compatible with power MOSFET input requirements. Similarly, power MOSFET characteristics must be chosen so that the device responds correctly to the on/off commands of the driving circuit.

For example, MOSFETs used with DTL, RTL or TTL devices must turn fully off at a gate voltage of 0.8V or less and turn on with a gate voltage above about 2.4V. How far the MOSFET turns on depends on available gate-drive voltage, and switching speed depends on how much drive current is available to charge device input capacitance quickly.

There are several options for meeting these requirements in each of the three modes of power MOSFET operation: common-source, source-follower and totem-pole.

Common-Source MOSFET Drive: Figure 1 illustrates why the common-source configuration is the easiest to drive. Gate drive voltage V_{GS} is the full output voltage of the direct-coupled, high-voltage CMOS logic element which can operate with ±15V supplies. This device can provide hard turn-on for most available power MOSFETs. The only problem arises if fast switching is required— particularly in MOSFETs with high threshold voltage for transient noise immunity. These power MOSFETs can have an input capacitance C_{iss} as much as 3000 pF, which demands a drive current substantially higher than that provided by a 74C00 CMOS gate, for example.

One solution is to use paralleled gates to boost drive current. Regardless of the number of gates used, they must be operated as close as possible to the ±15V rails for maximum current-handling capability. The other option is to use an emitter-follower drive circuit.

In Figure 2, for example, MOSFET drive current is the output current of the CMOS gate multiplied by the beta of the bipolar transistors. Switching speed is limited only by the speed of the CMOS driver or the f_t of the bipolar transistors. Moreover, there is no turn-off delay since emitter-followers never saturate.

Driving a logic-compatible, power MOSFET with RTL, DTL and TTL circuits requires different techniques. Low supply voltage (typically +5V) coupled with at least two internal diode voltage drops of these logic circuits restrict their high-state output voltage to about +3.7V or less, which is considerably lower than CMOS logic levels. Figure 3 shows how to make these logic families both supply and sink the substantial current required to switch power MOSFETs quickly.

The circuit shown is basically an open-collector TTL circuit with pull-up accomplished by using a totem-pole, emitter-coupled driver. The high-beta npn bipolar transistor and diode provide a fast charge and discharge cycle to maximize switching speed.

Source-Follower MOSFET Drive: The challenge in driving a source-follower power MOSFET is in keeping the gate at least 10V above the source voltage, regardless of its magnitude. The task is simple if another voltage source is available that exceeds drain voltage by about 10V. Alternatively, such a voltage can be provided by a bootstrap circuit, Figure 4. This circuit is effective only for repetitive drive operation and now for steady-state applications. Once capacitor C loses its charge, gate voltage drops and the capacitor does not recharge until the circuit is first shut down.

Diode D1 should have a high reverse leakage resistance to help maintain the charge on C1 as long as possible. The capacitance should be at least ten times C_{iss}.

Another way to drive a grounded load from a logic circuit is to use a p-channel, enhancement-mode MOSFET driven from CMOS, Figure 5. Here, the MOSFET source terminal is tied to the positive voltage rail and the CMOS, in effect, operates in reverse. In other words, a low logic

output turn on the power device and vice versa.

Power MOSFETs interface with most microprocessors without any major problems. The devices can be driven through the processor input/output ports and interface directly to any CMOS processor if logic levels are high enough to allow the device to produce useful current.

Logic-compatible power MOSFETs become susceptible to false triggering as increasing temperature lowers threshold voltage. Consequently, temperature control is a critical factor in applying these devices.

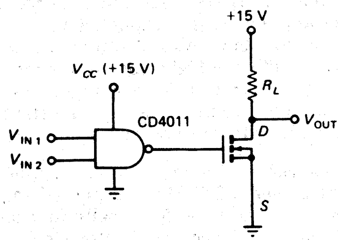


FIGURE 1. Driving a logic-compatible power MOSFET with a CMOS gate

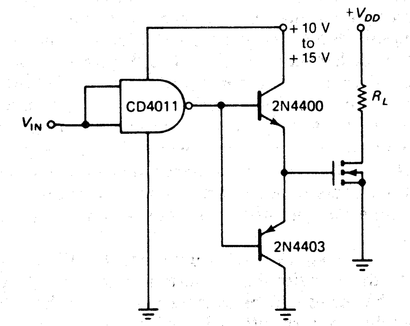


FIGURE 2. Using an emitter-follower to increase power FET speed and boost current source and sink capability

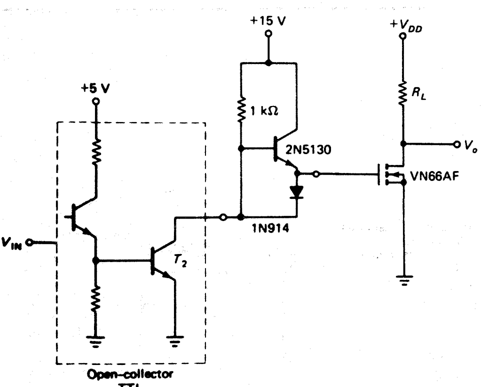


FIGURE 3. Increasing switching speed by charging MOSFET C_{in} with the almost unlimited current source of an external torem-pole circuit

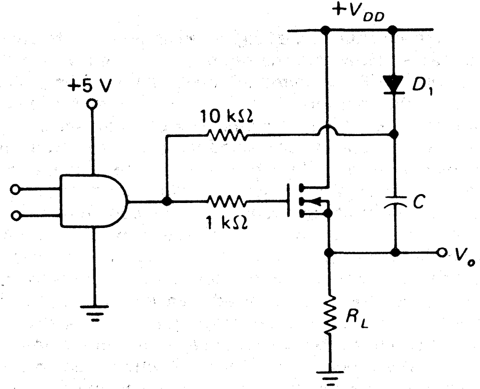


FIGURE 4. Using a bootstrap circuit to drive a source-follower from conventional TTL

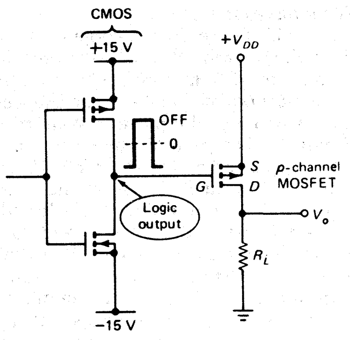


FIGURE 5. Eliminating the need for bootstrapping by using high-voltage CMOS to drive a p-channel power MOSFET source-follower

Frontiers of Application

As future MOSFET voltage and current ratings increase, resultant higher threshold voltages improve immunity to noise and false triggering. However, the penalty for improved noise immunity is decreased compatibility with most logic families other than high-voltage CMOS. Never-the less, although devices with higher electrical ratings may not be the easiest to combine with logic circuits, they promise unique advantages to a variety of new applications.

Synchronous Rectifiers: Among these new application possibilities, most excitement in the industry centers about the synchronous rectifier, which might find application in switch-mode power supplies (SMPS). An SMPS is often preferred over a linear power supply because high-frequency switching allows the use of smaller, lighter and lower-cost components that produce space-saving designs.

For example, filter choke coils and capacitors can be microhenries and picofarads in size instead of henries and microfarads. Additionally, high-frequency operation results in lower inductor core loss and allows a power supply to react faster to error signals. This latter benefit is especially attractive for powering microprocessors, which present a fast-changing load to a power source.

These advantages are heightened as operating frequency increases. However, the operating frequency of a conventional SMPS is limited to about 100kHz. The problem is with the minority storage time of both the bipolar transistor switching elementes as well as the intrinsic p-n diodes of power semiconductors. As frequency increases in a full-wave rectifier, this storage time becomes a significant part of total conduction time. Consequently, at high frequencies the conduction period of the diodes in each leg of the power transformer secondary winding overlap during a fraction of each cycle.

This "crowbar" condition, during which the secondary winding is effectively shorted, can lead to transformer overheating and eventual destruction — even with added circuit complications that reduce diode storage time.

Schottky diodes can switch effectively up into the microwave frequency region without causing this condition. Unfortunately, however, typical Schottky diodes have voltage ratings of only 40V; 60V devices are rare, and 80V ratings even more so.

Power MOSFETs are on the verge of a technological breakthrough that will allow a SMPS rectifier circuit to operate at up to 500kHz frequencies. In a synchronous rectifier, a portion of each side of the center-tapped secondary winding of the power transformer biases the FETs, Figure 6. The parasitic bipolar diode connected across the source and drain has a typical storage time of about 200ns and would encounter the same problems high-frequency as a discrete diode — if allowed to conduct.

To prevent this from occurring, the MOSFET must be able to pass useful current levels at a drain-to-source voltage drop less than forward turn-on voltage, $V_{f(diode)}$, of the intrinsic diode. The secret is in minimizing $r_{DS(on)}$ so that $E = IR < V_{f(diode)}$. This means that $r_{DS(on)}$ must be on the order of 0.02-0.04 ohms, which industry expects to achieve within a year. Also, it is expected that packages will be more massive than the presently used TO-3 design whose stray capacitance and pin resistance are too high.

Imminent reductions in $r_{DS(on)}$ promise significant improvement not only in device speed, but in power and thermal capabilities as well. For example, maximum drain current $I_{D(max)}$ is a function of maximum power dissipation $P_{DISS(max)}$ and $r_{DS(on)}$, expressed as

$$I_{D(max)} = \frac{P_{DISS(max)} \text{ @ ambient}}{r_{DS(on)} \text{ @ } T_j}$$

where T_j is maximum operating junction temperature of the device. Present power dissipation of power MOSFETs is limited to about 175W. But new package designs of next-generation devices are expected to be rated at a $P_{DISS(max)}$ of about 300W. Coupled with the decreases in $r_{DS(on)}$, devices with the higher power ratings should be able to deliver around 17A to a load. In fact, 50A MOSFETs are foreseeable in the not to distant future as 500W power dissipation ratings become feasible.

Energy Conversion: One of the largest applications for high-current power MOSFETs is expected to be in the energy conversion industry. Solar cells, for example, can generate 1V at 60A. Driven by a pulse-width modulator, power FETs can convert this energy into practical AC voltage, current and frequency. And if DC is required, the addition of a synchronous rectifier converts the switcher output to the required DC voltage and current.

Windmill energy conversion is a similar application potential for high-current MOSFETs, Figure 7. A windmill is used to drive a DC generator that charges a battery or powers some other load. Either way, the load acts as a brake that prevents generator damage from high-voltage caused by excessive windmill speed. Thus, if the generator is charging a battery, the battery must be disconnected when fully charged since it no longer constitutes a load. At the same time, another load must replace the charged battery.

It is conceivable that high-current MOSFETs will perform these switching functions. Additionally, the charged batteries can be switched into switcher circuits and synchronous rectifiers in the same manner as the solar cells for conversion to any required form of electrical power.

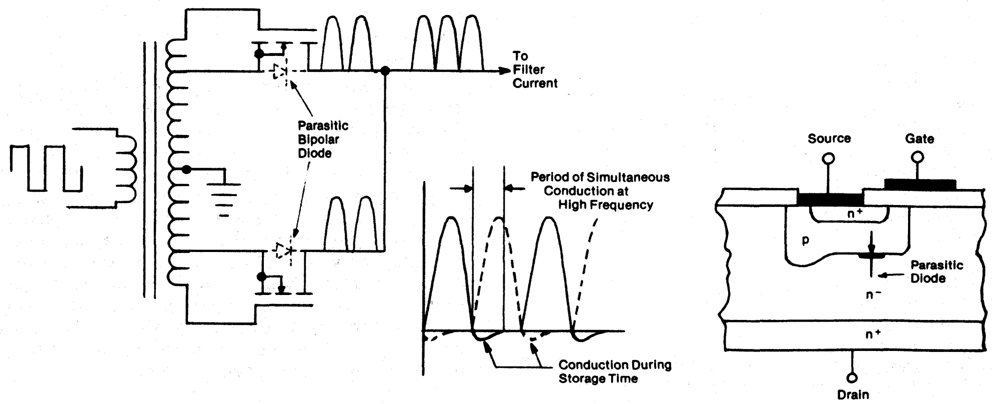
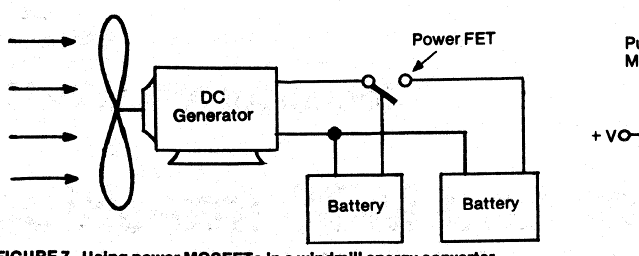


FIGURE 6. How storage time of the MOSFET parasitic diode limits maximum operating frequency



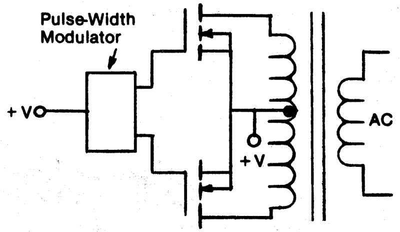


FIGURE 7. Using power MOSFETs in a windmill energy converter

Transportation: This capability of switching battery power may also benefit the electric vehicle industry. Most electrically powered vehicles use DC motors even though they are larger, heavier, less reliable and more expensive than AC motors. Moreover, DC motors have less than ideal speed-torque characteristics for motor vehicle operation, Figure 8. Despite these drawbacks, DC motors are preferred because their controllers are simpler and less cumbersome than those required by battery-powered AC motors.

Much of the circuit complication of an AC motor controller comes from the drive circuits of the bipolar power-switching devices, which traditionally have greater current-handling capability than MOSFETs. However, new power FETs with lower $r_{DS(on)}$ and higher P_{DISS} and current ratings will simplify AC motor controllers because MOSFET drive circuits are simpler. Thus, electric vehicles may at last be able to exploit the advantages of using an AC motor.

In a similar fashion, electrically powered mass transit systems such as the Bay Area Rapid Transit (BART) of the San Francisco—Oakland region could conceivably benefit from a change to AC motors. Each car in a multicar train is driven by its own DC motor. Consequently, a highly complex controller is needed to synchronize the speed of the DC motors. If the motors were AC, speed would automatically be synchronized by the frequency of the AC controller. Using power MOSFETs, the controller would synthesize AC waveforms with pulse-width modulation techniques.

The same reasoning applies to multimotor applications where speed relationships between many motors must be accurately maintained as in, for example, the conveyor drive system of an automated manufacturing complex.

Finally, MOSFETs are now eligible for applications previously beyond their temperature capabilities. Recently introduced devices have a 200°C junction-temperature rating, which matches that of bipolar power transistors. This means that power MOSFETs can now be used in ambient temperatures 33% hotter than before, Figure 9.

As a result, these devices are now ready for application in heat-generating appliances such as dishwashers and washer/dryers. Automotive applications, where temperatures reach 150°C under the hood and 110°C under the dashboard, are another application potential. Even higher temperatures are encountered by the power supplies of deep-well instrumentation which must withstand 200°C at depths of 20,000 feet. Here, the MOSFETs can be derated to deliver useful power levels.

Most of these new applications for power MOSFETs are on the threshold of reality. The 200°C T_j ratings are already available. And, from all indications, it is only a matter of time before devices can switch at a frequency of 500kHz, withstand drain-source potentials up to 850V, deliver 100W and 17A to a load and dissipate 300W. the principal beneficiaries of these dramatic performance improvements are expected to be the power-conversion industry, followed closely by the automotive, appliance and instrumentation industries. However, greater design freedoms afforded by new-generation power MOSFETs quite likely will foster even more, as yet unconceived applications.

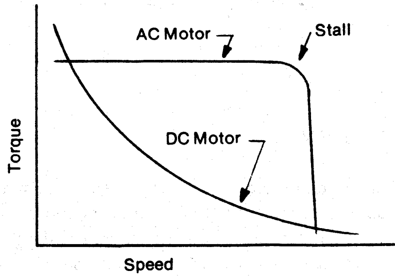


FIGURE 8. AC and DC motor speed-torque characteristics

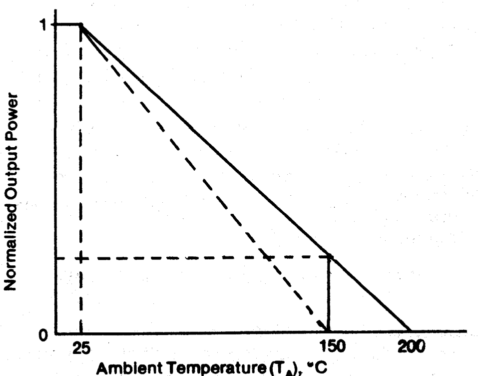


FIGURE 9. The advantage of higher T_j ratings. A power MOSFET with a T_j rating of 200°C can deliver useful power levels while operating in an ambient temperature 33% higher than that allowable for 150°C devices.

Siliconix

Technical Article TA82-3

Bipolar and MOS Transistors: Emerging Partners for the 1980s

Richard Blanchard, Ph.D.

INTRODUCTION

The designer of electronic systems requiring high current, high voltage components has witnessed a significant improvement in the availability of devices for this function. The development and introduction of power MOS transistors has significantly impacted the direction of power device technology. Future developments in this area are expected to have a similar effect as higher power, more versatile devices are introduced. This paper begins by tracing the development of power MOS transistors. The structure and performance of power MOS and bipolar transistors are then compared. The relative strengths of each device type are matched with applications. New solutions to specific systems problems are emphasized. As part of this comparison, an emerging class of devices—those manufactured by combining power MOS and bipolar transistors—is discussed. Finally, future directions of both MOS and bipolar transistor technology are discussed.

EVALUATION OF POWER MOS TRANSISTORS

The high current, high voltage power MOS transistors that are commercially available today are the result of nearly a decade of development effort. The evolution that led to these devices began with the N-channel MOSFET of Figure 1. Several key parameters determine the performance of this MOS transistor. These are:

L = The channel length (see Figure 1).

Z = The width of the channel (see Figure 1).

μ_e = The electron mobility in the channel region.

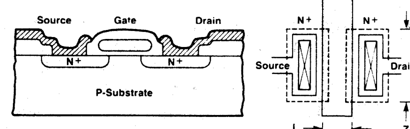
V_{GS} = The gate-to-source voltage.

V_T = The device threshold (turn-on) voltage.

C_o = The capacitance per unit area of the gate oxide.

I_D = The current through the transistor.

Figure 1. Structure of a Silicon Gate FET.



A current, I_D, flows through the transistor proportional to the gate-to-source voltage, V_{GS} flows through the transistor:

$$I_D = \frac{\mu_e C_o Z}{2L} (V_{GS} - V_T)^2 \quad (1)$$

for the transistor in saturation.

Using the definition

$$\beta_o = \frac{Z}{L} \mu_e C_o \quad (2)$$

the change in source-to-drain voltage for a given change in the gate-to-source voltage is:

$$g_m = \beta_o(V_{GS} - V_T) = \frac{1}{R_{DS(ON)}} \quad (3)$$

$$I_D = \frac{g_m}{2} (V_{GS} - V_T) \quad (4)$$

where $R_{DS(ON)}$ is the device on-resistance in the linear region. The voltage-current relationship of a conventional MOS transistor is shown in Figure 2. Examination of equations (2) and (4) provides information on the limits of conventional MOSFET technology.

The channel length, L, is determined by fabrication tolerances varying from 1-2μm for extremely short channel, low voltage devices to 15-25μm for higher voltage, long channel devices. The tolerance in the value of L is set by the ability to accurately reproduce the source-to-drain distance.

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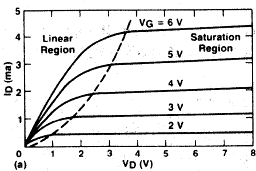
Figure 2. The Voltage-Current Relationship of a Conventional MOS Transistor Showing the Square Law Relationship.

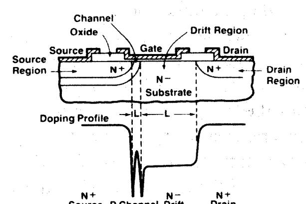


The reverse biased body-to-drain junction depletes further into the body region than the drain region because the drain region is more heavily doped than the body. The depletion of this junction into the body as a result of large source-to-drain voltages necessitates large values of L to obtain high breakdown voltages. An MOS structure that eliminates many of the voltage and on-resistance limitations of conventional MOS transistors is manufactured with double-diffused or DMOS technology.[1]

Double-diffused MOS structures utilize the difference in the diffusion of sequentially introduced impurities from a common edge or boundary to define the channel length. The channel length is analogous to the base width of a conventional double-diffused bipolar transistor. Control of both the channel length and the peak dopant concentration in the body are obtained as in double-diffused bipolar technology by the amount of dopant introduced at each step and the associated diffusion cycle. The channel length and dopant profile for a lateral DMOS or LDMOS transistor are shown in Figure 3. A DMOS transistor differs from a conventional MOS transistor in two significant ways:

1. The channel length, L, is determined by the difference between two sequential diffusions moving in the same direction from a common point of origin. L can be reproducibly controlled to values in the $1 \mu m$ to $2 \mu m$ range.
2. The body region is more heavily doped than the N-drain region. The body-to-drain junction depletes further into the drain region than into the body region when a reverse bias is placed across it. This difference allows significantly higher voltage to be placed across the body-to-drain junction without markedly affecting the electrical channel length of the transistor.

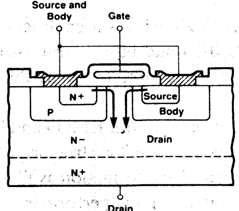
Figure 3. The Structure and Dopant Profile of a Lateral DMOS Field Effect Transistor.



These two differences result in MOS transistors with both a short channel length and the ability to withstand high drain-to-source voltages because of the separation of the active or channel region of the device from the region of the device that sustains the drain-to-source voltage. This structure is exactly analagous to that used in double-diffused bipolar transistors for many years. In these devices, a narrow, moderately doped based region controls device electrical characteristics. A highly doped N-collector region is used to support applied potentials.

A variation of the lateral DMOS structure is used for the manufacture of high current, high voltage MOS transistors. The vertical DMOS transistor[2] shown in Figure 4 is similar to the lateral DMOS transistor, except that the N+ drain region is on the backside of the device and current flow is largely vertical.

Figure 4. Structure of a VDMOS Power Transistor.



DMOS transistors exhibit some differences in the relationship between drain current and gate-to-source voltage. The simplest equation describing conventional MOS devices was previously given in equation (1):

$$I_D = \frac{\mu_e C_o Z}{2L} (V_{GS} - V_T)^2 \qquad (1)$$

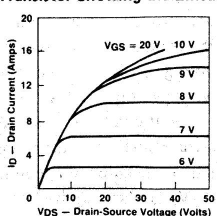
This equation indicates a square low relationship between the transistor current and the gate-to-source voltage. Such a dependence is observed in long channel MOS transistors under moderate gate voltages. In devices with short channel lengths such as DMOS transistors, the carrier velocity in the channel region saturates under even moderate drain-to-source voltages as a result of the interaction between the carriers. When velocity saturation occurs, equation (1) is no longer valid, and the drain current is linearly related to the gate-to-source voltage by the equation:

$$I_D = C_o Z V_{SAT} (V_{GS} - V_T) \qquad (5)$$

where V_{SAT} is the saturation velocity of electron in silicon.

The voltage-current relationship of a DMOS transistor is shown in Figure 5.

Figure 5. The Voltage-Current Relationship of a DMOS Transistor Showing the Linear Relationship.



COMPARISON OF DMOS AND BIPOLAR TRANSISTORS

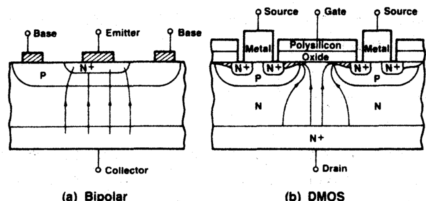
Transistors, whether bipolar or DMOS, may be used as linear devices or as switches. This paper focuses on the use of transistors as switches. The ideal switch has the following characteristics:

1. Infinite input impedance.
2. Zero switching time.
3. Zero on-resistance.
4. Infinite off resistance.
5. The ability to withstand infinite voltages.
6. Infinitely rugged.
7. Zero cost.

It is unlikely that such a device will be developed in the near future, but both DMOS and bipolar transistors have device characteristics that come close to matching this list.

The fabrication sequence for both DMOS and bipolar transistors produces devices with similar structures. This similarity can be seen in Figure 6. The information available from Figure 6 may be used for comparing the performance of DMOS and bipolar transistors.

Figure 6. Cross-Section of a Bipolar and a DMOS Transistor.

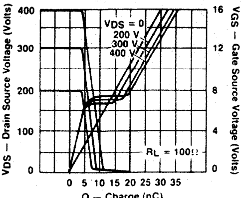


Drive Requirements

The ideal switch has an infinite input impedance and requires no power to change state. A bipolar transistor with a current gain of 10 to 100 requires a finite drive current, but a relatively low drive voltage. The base current must often be supplied from a power supply separate from the voltage on the load. For applications requiring high current, considerable power may be dissipated in the base drive circuitry. Cascaded transistor configurations are often used to reduce the base drive requirements.

In a DMOS transistor, the oxide layer that separates the gate from the channel region gives it an input impendance of 10^9 to 10^{11} ohms as compared to 10^3 to 10^5 ohms for a bipolar transistor. A DMOS transistor requires little current to maintain a constant voltage on its gate, but current is required to change the gate voltage. Figure 7 shows the amount of charge required to change the voltage in a 400V/3A VN4001 MOSPOWER transistor. Sufficient drive current must be sourced or sunk to change the gate voltage in the desired time. A higher voltage (~10V) is also required to fully turn on a power MOS transistor. The combination of high gate voltage and non-zero gate charge and discharge currents can often be met more easily than providing the drive to the base of a bipolar transistor, but these drive requirements must still be met.

Figure 7. The Gate Turn-On Charge Characteristics of a 400V/3A VN4000 MOSPOWER Transistor.



Switching Time

The switching speed of a device is directly related to time delays in the structure and the presence of capacitances that must be charged and discharged. The distance carriers must travel from the emitter to the collector region in a bipolar transistor is comparable to the source-to-drain distance in the DMOS structure. Accordingly, any time delays associated with carriers traversing these regions are comparable. Bipolar transistors operate through the flow of carriers from the emitter to the collector region through the base region. In the base region, these carriers are in the "minority." Turning on a bipolar transistor requires only that the capacitances associated with the junction be charged. The minority carrier distribution or "stored charge" required to sustain current flow results in a "storage time" when the bipolar transistor is switched from "on" to "off." This storage time may be on the order of microseconds.

The carrier flow from the source to the drain in a power MOS transistor occurs in an inverted region of the body adjacent to the gate. The current flow from source to drain is by majority carriers, hence no storage time effects are found in their devices. The switching time is determined by the gate capacitance and the current available from the drive circuitry.

Voltage Drop in the "On" State

Power MOS transistors have been portrayed as being capable of fast switching speeds, but having a relatively large forward drop in the "on" state. A comparison of the MOS and bipolar transistors of Figure 6 produces the results of Figure 8. This figure assumes that the same thickness and resistivity collector regions are used and that the devices have the same area. The same resistance value is present in the collector of the bipolar transistor and the drain of the DMOS transistor. However, the ability to bias the bipolar transistor into "quasisaturation" gives the bipolar transistor a significant advantage in voltage drop for a given current. As discussed earlier, this decreased voltage drop is not without its costs. The carriers present when the bipolar transistor in in quasisaturation result in a storage time. This storage time affects the device efficiency as a function of frequency. The power resulting from both switching and

resistive losses have been investigated for the devices of Figure 8. Figure 9 compares the total power loss in the two types of transistors[3] as a function of frequency. As expected, the bipolar transistor has less total power loss at low frequencies while the power MOS transistor is superior at high frequencies.

Figure 8. Collector and Drain Characteristics for the Bipolar and MOSFET at Low Voltages. [3]

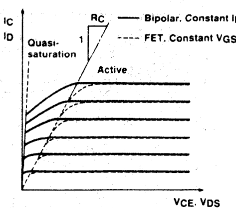
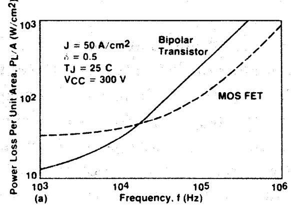


Figure 9. Total Power Loss vs. Frequency for MOS and Bipolar Transistors at 25°C. [3]



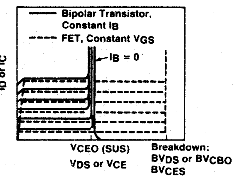
Device "Off" Resistance

Similar techniques are used in the manufacture of both power MOS and bipolar transistors. The silicon substrates used in device manufacture are capable of producing transistors with suitably low leakage currents at room temperature. However, at elevated temperatures, the leakage current increases due to the thermal generation of carriers. This unwanted junction "leakage" sets one limit on the maximum transistor operating temperature. Bipolar transistors are typically rated at 150°C. Leakage currents do not impact the operation of power MOS devices as significantly. A power MOS transistor with a rated junction operating temperature of 200°C has recently become available. There is no reason that this temperature rating cannot be achieved on all hermetic power MOS devices.

Transistor Breakdown Voltage

No electronics component is capable of withstanding an infinite voltage. The higher the voltage a device will withstand, the higher the voltage drop at a given current. It is most efficient to use a transistor with a voltage rating matched to the application. Investigation of the high voltage limits of bipolar and power MOS transistors shows that for the same material parameters in the collector and drain regions, there is a significant difference between the maximum voltage that the device can sustain under all operating conditions. This difference is shown in Figure 10. The bipolar transistor collector region thickness and resistivity must both be increased if the sustaining voltage of the bipolar transistor is to equal the breakdown voltage of the power MOS transistor. This change in the collector material reduces the voltage drop advantage that a bipolar transistor has over a power MOS transistor.

Figure 10. The Maximum Operating Voltage of a Bipolar and an MOS Transistor Fabricated in the Same Starting Material. [4]



At this time, bipolar transistors are available with voltage ratings higher than MOS transistors. This greater availability is the result of at least four factors:

1. Bipolar transistors have been under development for a longer period of time, so the techniques needed to obtain high voltages have been used more frequently.
2. A market for high voltage bipolar transistors has been developed over the years.
3. The large increase in MOS transistor on-resistance with breakdown voltage results in poorer relative performance when compared to bipolar transistors as the breakdown voltage increases.
4. The junctions used in the manufacture of MOS transistors are often shallower than those of a bipolar transistor. The surface geometry of a power MOS transistor places a restriction on the junction depth if efficient surface utilization is to be realized. High breakdown voltages are more easily obtained with greater junction depth.

With these constraints, it is unlikely that power MOS transistors with ratings in excess of 1200V will be commercially attractive.

Ruggedness

When comparing these two device types in terms of ruggedness, the power MOS transister is superior. Bipolar transistors have a positive temperature coefficient with current while MOS transistors have a negative temperature coefficient. As seen in Figure 11, a bipolar transistor has substantially higher voltage blocking capabilities at low currents, but a power MOSFET is rugged at high currents. The negative temperature coefficient of the MOSFET reduces the current through localized regions, allowing the transistor to sustain a considerably higher current over the entire chip. The power dissipation characteristics of the package, whether it houses a bipolar or an MOS transistor is also of great importance. The difference in safe operating area between packaged bipolar and power MOS transistors is shown in Figure 12.

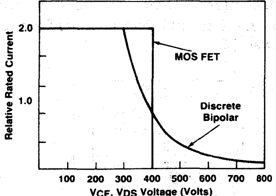


Figure 11. The Safe Operating Area Limits of Power MOS and Bipolar Transistor Chips. [5]

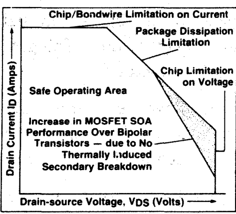
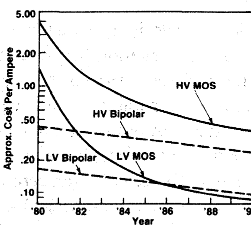


Figure 12. The Safe Operating Area of Assembled Power MOS and Bipolar Transistors.

Economics

A comparison of the process steps used in the manufacture of the two types of transistors reveals that both the process complexity and the number of critical process steps is greater for an MOS transistor. It follows that for the same die size, MOS transistors can, at best, approach the costs of bipolar transistors. The performance of each device per unit area and expenses associated with packaging and testing are two additional factors that impact cost. Based on the performance advantages that bipolar transistors have at higher voltages, they should remain less costly in this range. This conclusion is verified by the cost projections contained in Figure 13.

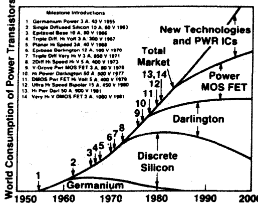
Figure 13. Cost Projections for Bipolar and MOS Power Transistors. [5]



POWER TRANSISTOR APPLICATIONS

The use of bipolar power transistors is continuing to expand as power conditioning efficiency becomes more important. The application of bipolar transistors is well documented, so their use will not be addressed here. Power MOS transistors are well under a decade old, however, and their use is continually expanding. Figure 14 shows the world consumption of power transistors from 1950 to 2000. The growth in the use of power MOS transistors, new technologies, and power ICs is particularly impressive. The remainder of this paper focuses on the application of power MOS transistors alone or in conjunction with bipolar transistors.

Figure 14. The Life Cycle of Low-Frequency Power Transistors. [5]



Power MOS Transistors

The applications most suited for power MOS transistors are those that utilize one of their advantages over bipolar transistors. A quick comparison of relative performance is given in Table 1. Using this table, one sees that applications needing high frequency capability and ruggedness are natural for power MOS transistors. The switch mode power supply has been identified as one such product. Much work has been done to use power MOS transistors as the main switching elements in these power supplies. Two additional power supply applications for MOS power transistors have recently emerged.

Table 1
A Comparison of Power MOS and Bipolar Electrical Characteristics

Parameter	MOS Performance	Bipolar Performance
Input Impedance	High (10^9-10^{11} ohms)	Intermediate (10^3-10^5 ohms)
Current Gain	High (10^5-10^8)	Intermediate (10^1-10^2)
Switching Frequency	High (100-500 kHz)	Intermediate (20-80 kHz)
On Resistance	High	Low
Off Resistance	High	High
Voltage Capability	Intermediate (500 V)	High (1200 V)
Ruggedness	Excellent	Good
Cost	High	Intermediate
Maximum Operating Temperature	High (200 C)	Intermediate (150 C)

Synchronous Bridge Rectifier

In power supplies and in other applications requiring full wave rectification, the diode bridge shown in Figure 15 is often used. The diodes in the bridge are not ideal, and there is a voltage drop of approximately 0.6V across the diode when it is conducting. There are also recovery- and steady-state currents in the reverse direction. The differences between the ideal and the actual current waveforms are shown in Figure 16. An alternate approach to rectification is shown in Figure 17. Using this circuit, the voltage drop across the bridge is significantly reduced. This reduction in voltage drop is apparent in Figure 18, where the output of a conventional diode bridge rectifier circuit and the power MOS synchronous bridge are compared to the input signal. Unfortunately, this circuit is limited to

applications with less than 30V peak to peak because of the breakdown voltage of the gate dielectric of the MOSFET. A second advantage of the power MOS synchronous bridge rectifier results from the reverse recovery current of the diode. The recovery time associated with this current reduces the efficiency of the bridge as the operating frequency increases. The efficiency of a conventional bridge using fast recovery diodes is considerably less than that of the power MOS synchronous bridge. This difference in efficiency is shown in Figure 19, where the response of each bridge to a 400KHz squarewave is shown.

Figure 15. A Conventional Diode Bridge Rectifier.

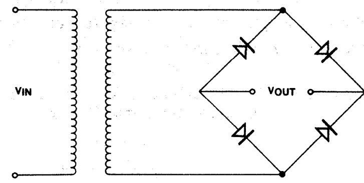


Figure 16. The Differences Between Ideal and Actual Current Waveforms of a Diode.

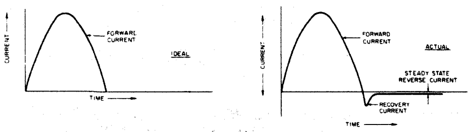


Figure 17. A Synchronous Bridge Rectifier Using MOSPOWER Transistors.

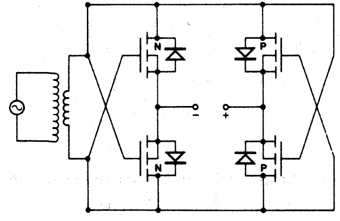
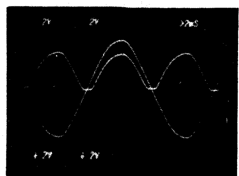
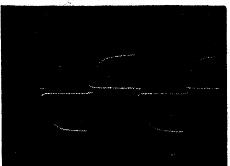


Figure 18. Input and Output Signals of Bridge Rectifiers.

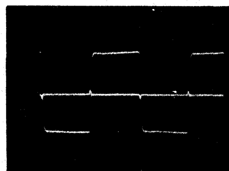


a. Conventional diode bridge. b. MOSPOWER synchronous bridge.

Figure 19. A Comparison of the Efficiency of a Conventional Diode Bridge Rectifier and a MOSPOWER Synchronous Bridge Rectifier with a 400 KHz Square Wave Input (.5 μs/div; 5V/div.).



a. Conventional bridge.



b. MOSPOWER bridge.

Synchronous Power MOS Rectifier

The second power supply application for power MOS transistors is replacing Schottky diodes as shown in Figure 20. A power MOS transistor is capable of carrying current in both directions. However, the body-drain diode limits the forward voltage across the junction, as seen in Figure 21. Figure 22 depicts the two current flow paths in a power MOS transistor used as a synchronous rectifier. The resistive characteristic of the power MOS transistor produces a sufficiently low voltage drop as long as its on-resistance is properly chosen. The device on-resistance depends strictly on area and breakdown voltage. Figure 23 shows the product of the device area and the on-resistance as a function of breakdown voltage for a variety of commercially available devices. Their performance is compared with the theoretical minimum for a silicon power MOS transistor. At low voltages, an order of magnitude improvement is possible in device performance per unit area. Assuming a 50V, 100A device is needed with a total voltage drop of 0.5V, it can be theoretically realized in a 2mm × 2mm (80 mils × 80 mils) chip if technology can come within a factor of two of the silicon limit.

Figure 20. Use of a MOSPOWER Transistor to Replace a Schottky Diode.

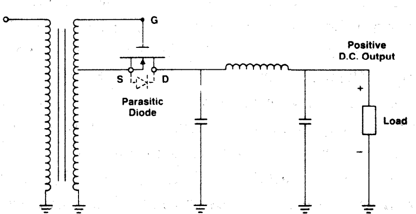


Figure 21. The Forward and Reverse Characteristics of a MOSPOWER Transistor.

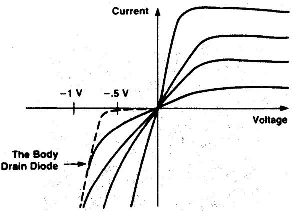


Figure 22. The Carrier Paths in a MOSPOWER Transistor Used as a Synchronous Rectifier.

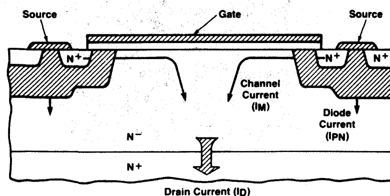
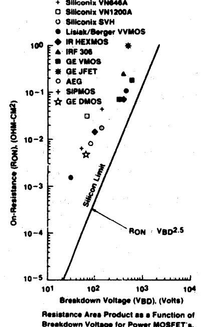


Figure 23. Device On-Resistance Area Product as a Function of Breakdown Voltage for Power MOS Transistor. [6]



Composite MOS/Bipolar Devices

The comparison of transistor characteristics shown in Table 1 has led to the proposal of combining bipolar and MOS transistors to take advantage of the best characteristics of each type. Three device configurations warranting consideration are the cascade, the cascode, and the parallel combinations.

Cascade Configurations

The Darlington configuration with one bipolar transistor driving another can be modified to take advantage of the characteristics of an MOS transistor. Substitution of an MOS transistor for the input transistor as shown in Figure 24 produces a composite device with the advantages of both transistor types. The high input impedance of the MOS transistor reduces the circuit drive requirements. In addition, all of the current through both the MOS transistor and the bipolar transistor flows through the load. This configuration retains the current handling capability and the low voltage drop of the bipolar transistor, but without the slow switching times. The MOS transistors across the base-collector junction of the bipolar transistor keep the bipolar out of full saturation. The majority carrier characteristics of the MOSFET allow the bipolar transistor to switch rapidly in this configuration. Trade-offs in the base-emitter resistor value and the on-resistance of the MOS transistor result in the combined device performance variations shown in Figure 25. This figure shows the trade-off between voltage drop and switching speed as a function of base-emitter resistor value and the $R_{DS(ON)}$ of the MOSFET. The ruggedness of this configuration is determined by the characteristics of the bipolar transistor. This configuration may be implemented by the circuit designer using discrete devices. This approach allows optimization of important performance parameters. If sufficiently large numbers of devices are required, they can be easily obtained using hybrid technology. It is also possible to fully integrate the cascade configuration as shown in Figure 26.

Figure 24. The MOS-Bipolar Cascade Configuration with a Base-Emitter Bypass Resistor.

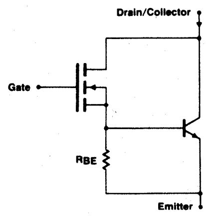


Figure 25. Performance of the MOS-Bipolar Cascade Configuration as a Function of Base-Emitter and MOS Transistor Resistance.

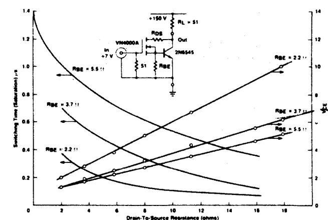
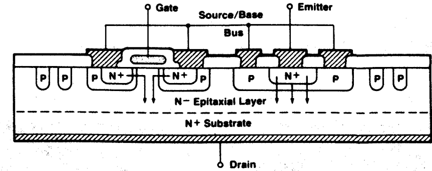


Figure 26. Cross-Section of a Monolithic Cascade MOS-Bipolar Structure. [7]

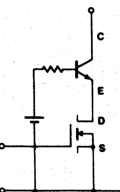


Cascode Configuration

The MOS–bipolar cascode configuration of Figure 27 produces a combined device with the collector base-breakdown voltage of the bipolar transistor and the fast switching characteristics of the MOS transistor. Since the MOS transistor only sees the base-emitter breakdown voltage, a high current, low on-resistance device may be used. The voltage drop is determined by

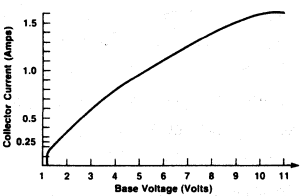
the saturation voltage of the bipolar transistor and the on-resistance of the MOSFET. This configuration also has the safe operating area of the common base bipolar transistor.

Figure 27. The MOS-Bipolar Cascode Configuration.



The cascode configuration may also be realized using discrete components, though it is not easily integrated. Proper selections of component values and the base bias voltage result in switching characteristics optimized for the applications. Figure 28 shows the impact of varying the base bias voltage on the collector current. As the collector current begins to saturate, the turn-off time of the circuit increases, limiting the maximum switching frequency.

Figure 28. Collector Current vs. Base Voltage for the Cascode Configuration.



Parallel Configuration

The use of an MOS transistor in parallel with a bipolar transistor as shown in Figure 29 has advantages that are not readily apparent. By properly sequencing the drive signal to the gate and the base, the ruggedness and fast switching speed of the MOS transistor may be combined with the low voltage drop of the bipolar transistor. The MOSFET is first turned on, allowing the load current to flow while absorbing any turn-on transient. The bipolar transistor is then turned on and the voltage across the parallel structure drops to its $V_{CE(SAT)}$. To turn the parallel combination off, the bipolar transistor base drive is first removed and the load current flows through the MOSFET. After the current through the bipolar transistor reaches zero, the MOS transistor is turned off, absorbing the associated transient. This series of events is shown in Figure 30, where the bipolar transistor input and the combined voltage drop across the parallel combination is shown. Figure 31 shows the bipolar and MOS current waveform during this drive sequence.

Figure 29. The MOS-Bipolar Transistor Parallel Configuration.

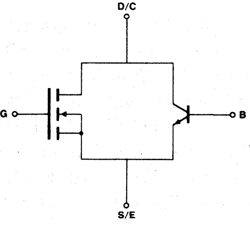


Figure 30. The Bipolar Transistor Input and the Combined Voltage Drop of the Parallel Configuration (10V/div., 5 μsec/div., R_L = 50 Ω).

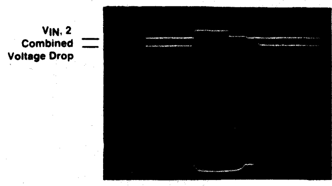
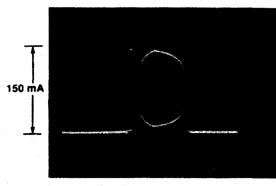
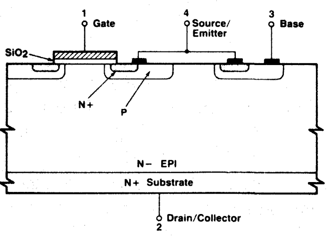


Figure 31. The Bipolar and MOS Transistor Current Waveform (5 μsec/div.).



The parallel combination of a bipolar and an MOS transistor may be optimized using discrete devices, but, as with the cascode configuration, it is possible to integrate this structure. A cross-section showing one monolithic implementation is shown in Figure 32.

Figure 32. Monolithic Implementation of the Parallel MOS-Bipolar Transistor Configuration. [8]

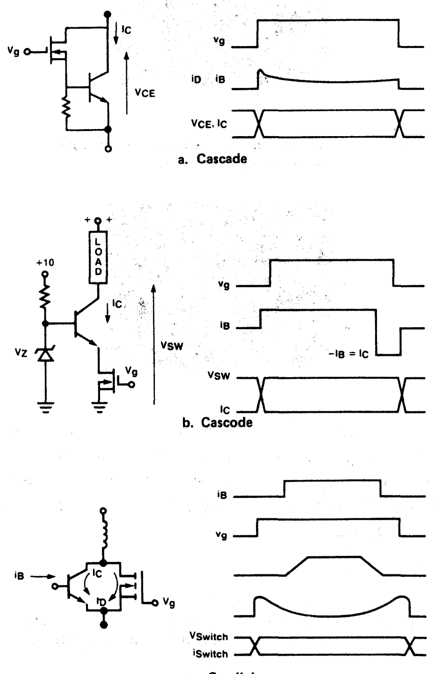


SUMMARY

The brief, but dynamic, history of power MOS transistors has been presented in this paper. Power MOS transistors have become accepted by "circuit design" engineers because of their performance advantages over bipolar transistors in certain applications. A comparison of MOS and bipolar transistors has been made. The strengths and weaknesses of each device type has been related to device structure. On the basis of this comparison, new applications for power MOS transistors in power supplies were presented.

The comparison of the relative advantages of bipolar and MOS transistors suggested combining the device types to gain the advantages of each. The performance of the cascade, cascode, and the parallel configuration has been discussed. These performances are summarized in Figure 33.

Figure 33. The Switching Waveforms of Combination Devices. [9]



a. Cascade

b. Cascode

c. Parallel

The development of new power semiconductor devices and power integrated circuits has not been discussed in this paper. Both of these areas promise to significantly impact the direction of power handling and conditioning technology. As new devices and integrated circuits become available to the design engineer, advancements in this area will continue.

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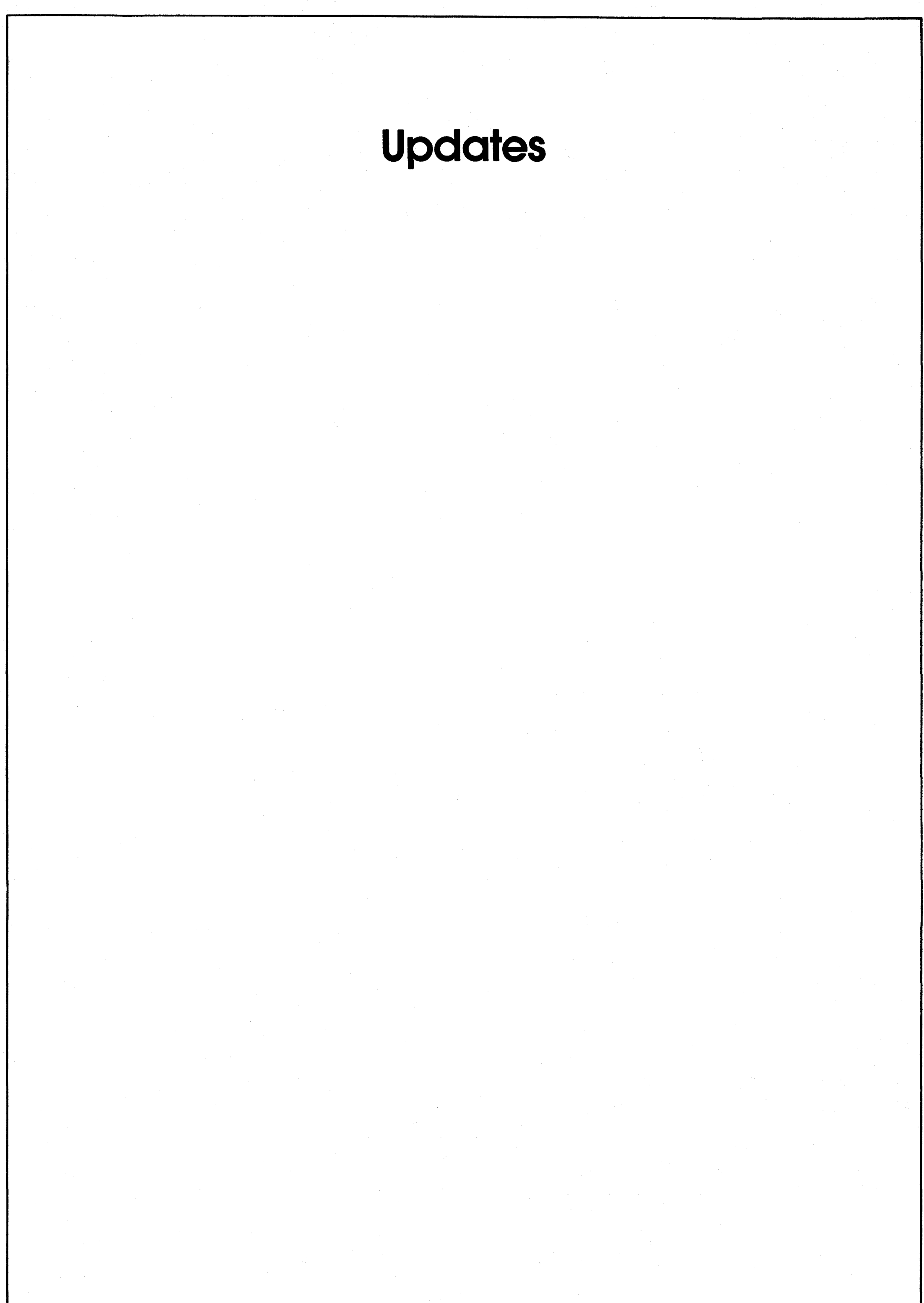

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Introduction

Siliconix is committed to your future system designs. As a multinational semiconductor manufacturer, we offer some of the industry's broadest product lines. No one gives you more analog switch ICs and MOSPOWER to choose from. Our multiple technologies include DMOS, VMOS, CMOS, PMOS, PMOS/bipolar and bipolar. And we are constantly advancing semi-custom state-of-the-art technology.

SMALL SIGNAL FETs

Siliconix is an industry leader in the manufacture of Small Signal FETs, offering a broad line of Junction Field Effect Transistors, MOS Field Effect Transistors, and DMOS Field Effect Transistors. Each line of transistors offers high-performance characteristics for such applications as low-noise, low-frequency amplifiers, low-drive DC amplifiers, high-frequency amplifiers on oscillators (to 1 GHz), ultra-low operating gate currents (to 10^{-13} Amp), and high-speed analog switching (under 1 ns).

Junction FETs are also used in N-channel monolithic and discrete pairs for a wide variety of use as high-performance amplifiers.

Siliconix offers a wide variety of package combinations, ranging from hermetic packaging to plastic packaging. Also offered are products in chip form to address hybrid requirements.

MOSPOWER

MOSPOWER identifies the "up front" technology that places Siliconix among the leaders in power device development for the 1980's, and has helped make Siliconix *the Discovery Company*.

MOSPOWER is a generic name coined by Siliconix to identify not only Siliconix's expanding family of medium and high power MOSFETs, but *all* power MOSFETs. The name also covers the many technologies used in the manufacture of these power MOSFETs which have been identified by various trade names. Vertical DMOS (double-diffused MOS); metal-gate V-groove MOS for high-frequency; lateral DMOS technology for arrays — all are covered by this generic name: MOSPOWER.

RF POWER

MOSPOWER shadow-mask vertical technology is used to manufacture the only true power MOS transistors. The technology enables their use as RF broadband amplifiers in the 2MHz to 200MHz region, providing output powers from 2 to 120 watts. Devices are available for 12.5V or 28V operation and in a variety of packages to suit different needs. They offer the advantages of high stage gain, low baseband noise and immunity to burn-out due to mismatch. The latest addition is the 35V single-side-band 2–30MHz series.

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Siliconix JFET, MOSPOWER and Integrated Circuit (IC) technologies have been utilized to produce an extensive family of Analog Switch ICs. They are used in many high-reliability military and aerospace applications such as Mercury, Gemini, Apollo and Skylab manned space programs. The family of analog switch ICs includes monolithic multi-channel switches with integral drivers. Also high performance JFET switches packaged with IC drivers offering very low ON-resistance, fast switching, excellent frequency response (DG180 series); low spike feed-through, low leakage and high OFF-isolation (DG281); low cost, single or dual supply operation (DG308, DG211); low consumption CMOS switches (DG300 series) and multiplexers with up to 16 channels (DG506A). The recent addition to the range of analog switch ICs is the Plus-40 enhanced DG5040 series with guaranteed safe operation up to 44V, and DG243CJ, the dual make-before-break equivalent of the DG5043CJ.

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Siliconix is an industry leader in telecommunications circuits, A/D conversion and micropower linears. The Company's LSI or linear ICs are incorporated in products ranging from sophisticated instrumentation to consumer smoke detectors. Advanced processing capabilities used in the manufacture of such ICs range from high and low voltage CMOS to bipolar-PMOS. High reliability processing procedures combined with volume production capabilities complement state-of-the-art products.

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Siliconix is a high-technology manufacturer of complex, highly specialized integrated circuits for the telecommunications industry. The current product lines use the CMOS process to satisfy the low power requirements of the telecom industry. Our Loop Disconnect Dialer Circuits offer subscribers push-button dialing privileges even with exchange systems presently tied to the rotary dial pulse timing.

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Siliconix's capability in providing high-reliability devices to meet stringent military or aerospace applications is amply demonstrated by the Company's qualifications as a supplier for important European projects that include Ariane, Concorde, European Airbus, the Alpha Jet and Tornado Aircraft, also Apollo, Viking and Voyager space projects.

Siliconix has a number of standard Hi-Rel screening options that can be applied to standard products. These options include screening to BS9000 for analog switches and CECC standards for FETs, also MIL-STD-750 for discrete FETs. In addition, Siliconix offers certain JEDEC-registered FETs with JAN, JANTX and JANTXV processing, as well as an increasing number of QPL-listed analog switches. Special additional inspections and controls can be met and Siliconix can supply SEM-qualified products to meet individual customer requirements.

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SMALL SIGNAL FET Product Information

Siliconix products are divided into three basic categories:

Standard Products, Modified Standard Products, Custom Products

- **Standard Products** — All the part numbers described in this catalog are standard products. A summary list of the prefixes used is shown below in the Device Identification Table. Ordering any of the standard products is easily done by referring to the data sheet part number. For example, a 2N4391 is simply ordered by that number: "2N4391." It will also appear in that form on the price lists, published separately.

- **Examples of Modified Standard Products are:**

Electrical Specials — Devices with either tightened, relaxed and/or special electrical specifications selected from a standard product.

Mechanical Specials — Devices with standard or modified electrical specifications mounted in non-standard packages or modified (lead formed) standard packages. Modifications and/or additions to standard marking are also considered mechanical specials.

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In all of the above cases (with the exception of JAN, JANTX, or JANTXV parts), a special part number is assigned which defines the part either by reference to customer's print(s) or by associated special requirements. Each special product is proprietary to the customer, and is *not* made available to other customers.

- **Custom Products** — Are designed to meet customer requirements not realizable by selection from standard parts; usually, these products require special engineering development. The proprietary relationship described above also applies to custom products.

Inquiries for *SPECIAL DEVICES* may be directed to the nearest field sales office or to:

FET Marketing Department, Siliconix incorporated, 2201 Laurelwood Road, Santa Clara, California 95054, Telephone: (408) 988-8000.

FETs/Part Number Prefixes and Suffixes

Prefix	XXX	XXXX
CR	Si Standard N-Channel Current Regulator	Si Standard N-Channel Current Regulator
CRR		
DPAD	Si Standard Dual JFET Diode	
DM		Special DMOS
DN		Special N-Channel Dual FET (Also Standard Offering)
FN	Special N-Channel JFET	Special N-Channel JFET (Also Standard Offering)
J	Si Standard TO-92 Cased FET	Special TO-92 Cased FET (Also Standard Offering)
JPAD	Si Standard TO-92 Cased JFET Diode	
M	Si Standard MOSFET	
MEM	Si Standard MOSFET	
MU	Special MOSFET (Also Standard Offering)	
PAD	Si Standard JFET Diode	
PF	Special P-Channel JFET (Also Standard Offering)	
PN		Si Standard TO-92 Cased FET
SD	Si Standard DMOS	
SU	Special P-Channel JFET (Also Standard Offering)	
U	Si Standard FET	Si Standard FET
VCR	Si Standard N- and P-Channel Voltage Controlled Resistors	
VMP	VMOS Power FET N-Channel	
VN		VMOS Power FET N-Channel
2N		JEDEC-Registered Device
3N	JEDEC-Registered Device	
Suffix		
-18	Std TO-92 Package with Center Lead Formed Toward Flat of TO-92 Package	

The above prefix list does not include some second source products supplied by Siliconix. Refer to FET Cross Reference and Index or current price list for availability of these devices.

SMALL SIGNAL FET Product Selector Guide

Application	Detail Application	Important FET Parameters Required	Major Tradeoffs	Unimportant FET Parameters	Preferred Parts
AMPLIFIER	Audio	Low noise (e_n), g_{fs}/g_{os}	Voltage amplification factor μ $= g_{fs}/g_{os}$ $= \Delta V_{DS}/\Delta V_{GS}$ @ I_D = const	$R_{DS(on)}$ $V_{DS(on)}$ $I_{D(off)}$ Switching Times	J111-3 PN4091-3 2N4094-3 2N4856-61 2N4339-40 2N4867-69 J230-32 J202-4 J308-10 U308-10
	Buffer	Low I_G, high g_{fs}			
	Differential	Good matching V_{GS}, g_{fs}, I_{DSS}, I_G			
	High Input Impedance	Very low I_G (e.g., MOSFET)			
	High Frequency	High g_{fs}/C_{iss} ratio, NF, RF parameters			
	FET Input Op Amp	Good matching V_{GS}, g_{fs}, I_{DSS}, I_G			
	Low Distortion	High $V_{GS(off)}$ compared to signal amplitude			
	Low Supply Voltage	Low $V_{GS(off)}$			
	Low Noise	Low e_n, i_n, low 1/f noise, low NF			
	Preamplifier	Operate near I_{DZO}, high g_{fs}/I_D ratio			
	Video	High g_{fs}/C_{iss} ratio, NF			
SWITCHES	Analog Gates	Fast switching time	$R_{DS(on)}$ vs. Capacitance	g_{fs} g_{os} I_{DSS} max	2N4091-3 2N4391-3 PN4091-3 PN4391-3 J108-10 J105-7 U290-1 2N5432-4
	Choppers	$r_{DS}/I_{D(off)}$ switching efficiency			
	Commutators	Low C_{rss}			
	Digital	Fast switching time			
	Integrator Reset	Very low $R_{DS(on)}$, High I_{DSS}			
	Sample and Hold	Low C_{rss}			
CONSTANT CURRENT SOURCE	Current Limiting Reference Current Source Biasing	Low g_{oss}, low $V_{GS(off)}$, high BV_{GSS}	I_{DSS} vs. BV_{GSS}	g_{fs}, $R_{DS(on)}$, $I_{D(off)}$, $V_{DS(on)}$ switching times, RF parameters, capacitance	CRR Series J501-11 J552 Any J-FET
VOLTAGE CONTROLLED RESISTORS	Gain Control Amplitude Stability Attenuators	High $V_{GS(off)}$ for wide dynamic range and low distortion		g_{fs}, BV_{GSS}, I_{DSS}	VCR Series Any J-FET
MIXERS	VHF	RF parameters, NF, high g_{fs}/C_{iss} ratio, low C_{rss}		$r_{DS(on)}$ $V_{DS(on)}$ $I_{D(off)}$	U430-1 U440-1-3-4 2N5911-12 U308-10 J308-10
	UHF Double Balanced	Matching characteristics			
OSCILLATORS	Class A	Good g_{fs} at operating frequency	g_{fs} vs. Capacitance		2N4416 PN4416 U308-10 J308-10
	Class C	Low C_{iss} for VHF operation			

SMALL SIGNAL FET Application Selection Preferences

Additional Information

POPULAR PRODUCT TYPES	2N4117-9, 2N4117A-19A, PN4117-20, A	2N4338-41, J201-4, J304-5	2N4416, PN4416	2N3821-2, 2N4221-2, 2N5457-9	2N4867-9 A, J230-2	U308-10, J308-10	J300, J210-2	J105-7, U290-1	2N5432-4, J108-10	2N4856-61, 2N4391-3, J111-13, PN4391-3	3N163, 4, MFE823	U421-U428
PROCESS DESIGNATION	**NT**	**NP**	**NH**	**NRL**	**NS**	**NZA**	**NZF**	**NVA**	**NIP**	**NC**	**MRA**	**NNT**
Low Current Amplifier	P	S		S	S						P	P
Low Freq Amplifier ≤ 100 Hz		S		S	S						P	
High Freq Amplifier > 100 MHz			P			P	P					
HF ≥ 400 MHz Prime						P	S					
General Purpose Amplifier		P	P	P						P		
Low Noise Amp (10 Hz e_n)		P	S	S	S				S	P		
Low Noise Amp > 50 MHz			P	S		P	P					
High Frequency Mixer			P			P	P					
Dual Diff Pair												P
AGC Amplifier			P	P			P					
Electrometer Preamp	P											P
Microvolt Amplifier	P											P
Low Leakage Diode	P	S										
Low Leakage Dual Diode												P
Smoke Detector Input	P										P	
Battery Operated Amp < 1.5V	P	P										P
Diff/Single Ended Inp. Stag.												P
High Slew Rate Diff Amp												
Active Filter		S	P	P								
Oscillator		S	P	P		P	P					
Voltage Controlled Resistor		S	P	P						P		
Hybrid Chips	P	P	P	P						P		P
Analog/Digital Switch			S					P	P	P	S	
Multiplexing			P	S				S	S	P		
Choppers								P	P	P		
Reed Relay Replacement								P	P			
Sub pA Dual Diff Pair												P
Sample Hold			P	S						P		S
Buffer Interface to CMOS												
Matched Switch												
Current Limiter										P		
Current Source	S	S		LV								LV
High Voltage Protection Diode												

P = PRIME CHOICE
S = SECONDARY (ALTERNATIVE) CHOICE
LV = LIMITED VALUE

SMALL SIGNAL FET Application Selection Preferences
(Cont'd)

2N5196-9, 2N5515-24, 2N5545-7, 2N39548, U231-5	U401-6	2N5911-12, U440-1 U443-4	2N5902-9	2N5564-6, DN5564-6	2N5515-24, 2N6483-5	2N5018-21, 2N5114-6 J174-7	2N2609, 2N2844	2N3382, 4, 6	2N2608, VCR5P	J500-J511	CRR0240-CRR0560 J553-7, J9100	CRR0800-CRR1250 CR068-CR150	CRR1450-CRR4300 CR160-CR470	SD210-SD215DE	JR135V-JR240V
NQP	NNR	NZFD	NTD	NCD	NSD	PS	PD	PE	PC	NCL	NKL	NKM	NKO	DMCB	VRMA
P	P		S		S		P	LV	LV						
P	P				S	S	S								
		P												P	
														P	
						P	P	LV	LV					S	
P	P			P	S										
		P		P											
P	P	P	S	S	S										
S	S		S												
P	P		S												
S			S												
P	P	P		P											
		P		P											
							S								
							S								
	P					P	P		P						
P	P		LV			P	P	S		P	P	P	P		
	S			S		P								P	
						P								P	
				P		P								P	
														P	
			S												
S	S		S			P									
						P	P		S						
S	P	S		P											
						P				P	P	P	P		
							S			P	P	P	P		
															P

SMALL SIGNAL FET Product Specifications

N & P-Channel Single JFETs

PART NUMBER	DEVICE	N or P	GEOMETRY (Section 4)	RESISTANCE Chnl Ω, Max.	RESISTANCE Gate Ω	NOISE VOLTAGE (nV/√Hz, MAX.) or (NF, dB, MAX.)	INPUT CAPACITANCE (pF, MAX.)	TRANS-CONDUCTANCE gfs (μmhos) Max.	TRANS-CONDUCTANCE gfs (μmhos) Min.	SATURATION CURRENT (mA) Max.	SATURATION CURRENT (mA) Min.	BREAKDOWN VOLTAGE (V, MAX.)	THRESHOLD VOLTAGE (V, MAX.)	LEAKAGE (nA, MAX.) Chnl	LEAKAGE (nA, MAX.) Gate	PACKAGE (TO-)
2N4117	LOW LEAKAGE	N	NT	–	–	–	3	210	70	0.09	0.03	40	1.8	–	0.01	72
2N4117A	LOW LEAKAGE	N	NT	–	–	–	3	210	70	0.09	0.03	40	1.8	–	0.001	72
2N4118	LOW LEAKAGE	N	NT	–	–	–	3	250	80	0.24	0.08	40	3.0	–	0.01	72
2N4118A	LOW LEAKAGE	N	NT	–	–	–	3	250	90	0.24	0.08	40	3.0	–	0.001	72
2N4119	LOW LEAKAGE	N	NT	–	–	–	3	330	100	0.6	0.2	40	6.0	–	0.01	72
2N4119A	LOW LEAKAGE	N	NT	–	–	–	3	330	100	0.6	0.2	40	6.0	–	0.001	72
PN4117	LOW LEAKAGE	N	NT	3K	–	–	–	210	70	0.09	0.03		−40		0.01	92
PN4117A	LOW LEAKAGE	N	NT	3K	–	–	–	210	70	0.09	0.03		−40		0.001	92
PN4118	LOW LEAKAGE	N	NT	3K	–	–	–	250	80	0.24	0.08		−40		0.01	92
PN4118A	LOW LEAKAGE	N	NT	3K	–	–	–	250	80	0.24	0.08		−40		0.001	92
PN4119	LOW LEAKAGE	N	NT	3K	–	–	–	330	100	0.6	0.2		−40		0.01	92
PN4119A	LOW LEAKAGE	N	NT	3K	–	–	–	330	100	0.6	0.2		−40		0.001	92
PN4120	LOW LEAKAGE	N	NT	3K	–	–	–	330	100	0.6	0.2		−40		–	92
FN4117	LOW LEAKAGE	N	NT	3K	–	–	–	210	70	0.09	0.03		−40		0.005	72
FN4117A	LOW LEAKAGE	N	NT	–	–	–	3	210	70	0.2	0.03	40	2.0		0.001	72
FN4118	LOW LEAKAGE	N	NT	3K	–	–	–	250	80	0.24	0.08		−40		0.005	72
FN4118A	LOW LEAKAGE	N	NT	–	–	–	3	250	80	0.4	0.08	40	2.0		0.001	72
FN4119	LOW LEAKAGE	N	NT	3K	–	–	–	330	100	0.6	0.2		−40		0.005	72
FN4119A	LOW LEAKAGE	N	NT	–	–	–	3	330	100	1.2	0.2	40	6.0		0.001	72
FN4392	LOW LEAKAGE	N	NC	14	60	–	–		–	100	25		40	0.1	0.1	18
FN4393	LOW LEAKAGE	N	NC	14	100	–	–		–	60	5.0		40	0.1	0.1	18
2N4220A	LOW NOISE	N	NRL	–	1M	2.5	6	4000	1000	3.0	0.5	30	4.0	–	0.1	72
2N4221 A	LOW NOISE	N	NRL	–	1M	2.5	6	5000	2000	6.0	2.0	30	6.0	–	0.1	72
2N4222	LOW NOISE	N	NRL	–	1M	2.5	6	6000	2500	15	5.0	30	8.0	–	0.1	72
2N4338	LOW NOISE	N	NP	–	1M	1.0	7	1800	600	0.6	0.2	50	1.0	–	0.1	18
2N4339	LOW NOISE	N	NP	–	1M	1.0	7	2400	800	1.5	0.5	50	1.8	–	0.1	18
2N4340	LOW NOISE	N	NP	–	1M	1.0	7	3000	1300	3.6	1.2	50	3.0	–	0.1	18
2N4341	LOW NOISE	N	NP	–	1M	1.0	7	4000	2000	9.0	3.0	50	6.0	–	0.1	18
2N4867	LOW NOISE	N	NS or NP	–	–	20	25	2000	700	1.2	0.4	40	2.0	–	0.25	72
2N4867A	LOW NOISE	N	NS or NP	–	–	10	25	2000	700	1.2	0.4	40	2.0	–	0.25	72
2N4868	LOW NOISE	N	NS or NP	–	–	20	25	3000	1000	3.0	1.0	40	3.0	–	0.25	72
2N4868A	LOW NOISE	N	NS or NP	–	–	10	25	3000	1000	3.0	1.0	40	3.0	–	0.25	72
2N4869	LOW NOISE	N	NS or NP	–	–	20	25	4000	1300	7.5	2.5	40	5.0	–	0.25	72
2N4869A	LOW NOISE	N	NS or NP	–	–	10	25	4000	1300	7.5	2.5	40	5.0	–	0.25	72
J230	LOW NOISE	N	NS or NP	–	–	30	–	2500	1000	3.0	0.7	40	3.0	–	0.25	92
J230-18	LOW NOISE	N	NS or NP	–	–	30	–	2500	1000	3.0	0.7	40	3.0	–	0.25	92
J231	LOW NOISE	N	NS or NP	–	–	30	–	3000	1500	6.0	2.0	40	5.0	–	0.25	92
J231-18	LOW NOISE	N	NS or NP	–	–	30	–	3000	1500	6.0	2.0	40	5.0	–	0.25	92
J232	LOW NOISE	N	NS or NP	–	–	30	–	4000	2500	10	5.0	40	6.0	–	0.25	92

SMALL SIGNAL FET Product Specifications (Cont'd)

N & P-Channel Single JFETs

Device: RF AMPLIFIERS

PART NUMBER	N or P	PACKAGE (TO-)	LEAKAGE (nA, MAX.) Gate	LEAKAGE (nA, MAX.) Chnl	THRESHOLD VOLTAGE (V, MAX.)	BREAKDOWN VOLTAGE (V, MAX.)	SATURATION CURRENT (mA) Min.	SATURATION CURRENT (mA) Max.	TRANS-CONDUCTANCE gfs (μmhos) Min.	TRANS-CONDUCTANCE gfs (μmhos) Max.	INPUT CAPACITANCE (pF, MAX.)	NOISE VOLTAGE (nV/√Hz, MAX.) or (NF, dB, MAX.)	RESISTANCE Gate Ω	RESISTANCE Chnl Ω, Max.	GEOMETRY (Section 4)
J232-18	N	92	0.25	–	6.0	40	5.0	10	2500	4000	–	30	–	–	NS
J270-18	P	92	0.2	–	2.0	30	2.0	15	6000	15000	–	–	–	–	PS
2N3819	N	92	2.0	–	8.0	25	2.0	20	2000	6500	8.0	–	–	–	NRL
2N3823	N	72	0.5	–	8.0	30	4.0	20	3500	6500	6	2.5	1K	–	NRL
2N4223	N	72	0.25	–	8.0	30	3.0	18	3000	7000	6	5.0	1K	–	NRL
2N4224	N	72	0.5	–	8.0	30	2.0	20	2000	7500	6	–	–	–	NRL
2N4416	N	72	0.1	–	6.0	30	5.0	15	4500	7500	4	2.0	1K	–	NH
2N4416A	N	72	0.1	–	6.0	35	5.0	15	4500	7500	4	2.0	1K	–	NH
2N5078	N	72	0.25	–	8.0	30	4.0	25	4500	10000	6	3.0	1K	–	–
2N5484	N	92	1.0	–	3.0	25	1.0	5.0	3000	6000	5	3.0	1K	–	NH
2N5485	N	92	1.0	–	4.0	25	4.0	10	3500	7000	5	2.0	1K	–	NH
2N5486	N	92	1.0	–	6.0	25	8.0	20	4000	8000	5	2.0	1K	–	NH
2N5668	N	92	2.0	–	4.0	25	1.0	5.0	1500	6500	7	2.5	1K	–	NH
2N5669	N	92	2.0	–	6.0	25	4.0	10	2000	6500	7	2.5	1K	–	NH
2N5670	N	92	2.0	–	8.0	25	8.0	20	3000	7500	7.0	2.5	1K	–	NH
J210	N	92	0.1	–	3.0	25	2.0	15	4000	12000	–	–	–	–	NZF
J211	N	92	0.1	–	4.5	25	7.0	20	7000	12000	–	–	–	–	NZF
J212	N	92	0.1	–	6.0	25	15	40	7000	12000	–	–	–	–	NZF
J270	P	92	0.2	–	2.0	30	2.0	15	6000	15000	–	–	–	–	PS
J271	P	92	0.2	–	4.5	30	6.0	50	8000	18000	–	–	–	–	PS
J300	N	92	0.5	–	6.0	25	6.0	30	4500	9000	5.5	–	–	–	NZF
J304	N	92	0.1	–	6.0	30	5.0	15	4500	7500	–	–	–	–	NH
J305	N	92	0.1	–	3.0	30	1.0	8.0	3000	–	–	–	–	–	NH
J308	N	92	1.0	–	6.5	25	12	60	8000	20000	7.5	–	–	–	NZA
J309	N	92	1.0	–	4.0	25	12	30	10000	20000	7.5	–	–	–	NZA
J310	N	92	1.0	–	6.5	25	24	60	8000	18000	7.5	–	–	–	NZA
PN4416	N	92	1.0	–	6.0	30	5.0	15	4500	7500	4.0	2.0	1K	–	NH
MPF102	N	92	2.0	–	7.5	25	2.0	20	2000	7500	7.0	–	–	–	NH
MPF108	N	92	1.0	–	8.0	25	1.5	24	2000	7500	6.5	2.5	1M	–	NH
MPF112	N	92	100	–	10	25	1.0	25	1000	7500	–	–	–	–	NH
U308	N	52	0.15	–	6.0	25	12	60	10000	20000	7.5	–	–	–	NZA
U309	N	52	0.15	–	4.0	25	12	30	10000	20000	7.5	–	–	–	NZA
U310	N	52	0.15	–	6.0	25	24	60	10000	18000	7.5	–	–	–	NZA
U311	N	72	0.15	–	6.0	25	20	60	10000	20000	7.5	–	–	–	NZA
U312	N	52	0.1	–	6.0	25	10	30	6000	10000	5.0	–	–	–	NZF

SMALL SIGNAL FET Product Specifications (Cont'd)

N & P-Channel Single JFETs

PART NUMBER	DEVICE	GEOMETRY (Section 4)	RESISTANCE Chnl Ω, Max.	RESISTANCE Gate Ω	NOISE VOLTAGE (nV/√Hz, MAX.) or (NF, dB, MAX.)	INPUT CAPACITANCE (pF, MAX.)	TRANS-CONDUCTANCE gfs (μmhos) Max.	TRANS-CONDUCTANCE gfs (μmhos) Min.	SATURATION CURRENT (mA) Max.	SATURATION CURRENT (mA) Min.	BREAKDOWN VOLTAGE (V, MAX.)	THRESHOLD VOLTAGE (V, MAX.)	LEAKAGE (nA, MAX.) Chnl	LEAKAGE (nA, MAX.) Gate	PACKAGE (TO-)	N or P
U1837	RF AMP	NH	—	1K	3.0	6.0	10000	4500	25	4.0	30	8.0	—	0.25	92	N
U1837-18	RF AMP	NH	—	1K	2.0	6.0	10000	4500	25	4.0	30	8.0	—	0.25	92	N
2N3824	SWITCHES & CHOPPERS	NRL	250	—	—	6.0	—	—	—	—	50	8.0	0.1	0.1	72	N
2N3966	SWITCHES & CHOPPERS	NH	220	—	—	6.0	—	—	—	2.0	30	6.0	1.0	0.1	72	N
2N3970	SWITCHES & CHOPPERS	NC	30	—	—	25	—	—	150	50	40	10	0.25	0.25	18	N
2N3971	SWITCHES & CHOPPERS	NC	60	—	—	25	—	—	75	25	40	5.0	0.25	0.25	18	N
2N3972	SWITCHES & CHOPPERS	NC	100	—	—	25	—	—	30	5.0	40	3.0	0.25	0.25	18	N
2N4091	SWITCHES & CHOPPERS	NC	30	—	—	16	—	—	—	30	40	10	0.2	0.2	18	N
2N4092	SWITCHES & CHOPPERS	NC	50	—	—	16	—	—	—	15	40	7.0	0.2	0.2	18	N
2N4093	SWITCHES & CHOPPERS	NC	80	—	—	16	—	—	—	8.0	40	5.0	0.2	0.2	18	N
2N4391	SWITCHES & CHOPPERS	NC	30	—	—	14	—	—	150	50	40	10	0.1	0.1	18	N
2N4392*	SWITCHES & CHOPPERS	NC	60	—	—	14	—	—	75	25	40	5.0	0.1	0.1	18	N
2N4393*	SWITCHES & CHOPPERS	NC	100	—	—	14	—	—	30	5.0	40	3.0	0.1	0.1	18	N
2N4856	SWITCHES & CHOPPERS	NC	25	—	—	18	—	—	—	50	40	10	0.25	0.25	18	N
2N4856A	SWITCHES & CHOPPERS	NC	25	—	—	10	—	—	—	50	40	10	0.25	0.25	18	N
2N4857	SWITCHES & CHOPPERS	NC	40	—	—	18	—	—	100	20	40	6.0	0.25	0.25	18	N
2N4857A	SWITCHES & CHOPPERS	NC	40	—	—	10	—	—	100	20	40	6.0	0.25	0.25	18	N
2N4858	SWITCHES & CHOPPERS	NC	60	—	—	18	—	—	80	8.0	40	4.0	0.25	0.25	18	N
2N4858A	SWITCHES & CHOPPERS	NC	60	—	—	10	—	—	80	8.0	40	4.0	0.25	0.25	18	N
2N4859	SWITCHES & CHOPPERS	NC	25	—	—	18	—	—	—	50	30	10	0.25	0.25	18	N
2N4859A	SWITCHES & CHOPPERS	NC	25	—	—	10	—	—	—	50	30	10	0.25	0.25	18	N
2N4860	SWITCHES & CHOPPERS	NC	40	—	—	18	—	—	100	20	30	6.0	0.25	0.25	18	N
2N4860A	SWITCHES & CHOPPERS	NC	40	—	—	10	—	—	100	20	30	6.0	0.25	0.25	18	N
2N4861	SWITCHES & CHOPPERS	NC	60	—	—	18	—	—	80	8.0	30	4.0	0.25	0.25	18	N
2N4861A	SWITCHES & CHOPPERS	NC	60	—	—	10	—	—	80	8.0	30	4.0	0.25	0.25	18	N
2N5018	SWITCHES & CHOPPERS	PS	75	—	—	45	—	—	—	10	30	10	10.0	2.0	18	P
2N5019	SWITCHES & CHOPPERS	PS	150	—	—	45	—	—	—	5.0	30	5.0	10.0	2.0	18	P
2N5114	SWITCHES & CHOPPERS	PS	75	—	—	25	—	—	90	30	30	10	0.5	0.5	18	P
2N5115	SWITCHES & CHOPPERS	PS	100	—	—	25	—	—	60	15	30	6.0	0.5	0.5	18	P
2N5116	SWITCHES & CHOPPERS	PS	150	—	—	25	—	—	25	5.0	30	4.0	0.5	0.5	18	P
2N5432	SWITCHES & CHOPPERS	NIP	5.0	—	—	30	—	—	—	150	25	10	0.2	0.2	52	N
2N5433	SWITCHES & CHOPPERS	NIP	7.0	—	—	30	—	—	—	100	25	9.0	0.2	0.2	52	N
2N5434	SWITCHES & CHOPPERS	NIP	10	—	—	30	—	—	—	30	25	4.0	0.2	0.2	52	N
2N5638	SWITCHES & CHOPPERS	NC	30	—	—	10	—	—	—	50	30	12	1.0	1.0	92	N
2N5639	SWITCHES & CHOPPERS	NC	60	—	—	10	—	—	—	25	30	8.0	1.0	1.0	92	N

*FN4392 and FN4393 available

SMALL SIGNAL FET Product Specifications (Cont'd)

N & P-Channel Single JFETs

DEVICE: SWITCHES & CHOPPERS

PART NUMBER	GEOMETRY (Section 4)	RESISTANCE Chnl Ω, Max.	RESISTANCE Gate Ω	NOISE VOLTAGE (nV/√Hz, MAX.) or (NF, dB, MAX.)	INPUT CAPACITANCE (pF, MAX.)	TRANSCONDUCTANCE gfs (μmhos) Max.	TRANSCONDUCTANCE gfs (μmhos) Min.	SATURATION CURRENT (mA) Max.	SATURATION CURRENT (mA) Min.	BREAKDOWN VOLTAGE (V, MAX.)	THRESHOLD VOLTAGE (V, MAX.)	LEAKAGE (nA, MAX.) Chnl	LEAKAGE (nA, MAX.) Gate	PACKAGE (TO-)	N or P
2N5640	NC	100	—	—	10	—	—	—	5.0	30	6.0	1.0	1.0	92	N
2N5653	NC	50	—	—	10	—	—	—	40	30	12	1.0	1.0	92	N
2N5654	NC	100	—	—	10	—	—	—	15	30	8.0	1.0	1.0	92	N
J105	NVA	3.0	—	—	—	—	—	—	500	25	10.0	3.0	3.0	92	N
J105-18	NVA	3.0	—	—	—	—	—	—	500	25	10	3.0	3.0	92	N
J106	NVA	6.0	—	—	—	—	—	—	200	25	6.0	3.0	3.0	92	N
J106-18	NVA	6.0	—	—	—	—	—	—	200	25	6.0	3.0	3.0	92	N
J107	NVA	8.0	—	—	—	—	—	—	100	25	4.5	3.0	3.0	92	N
J107-18	NVA	8.0	—	—	—	—	—	—	100	25	4.5	3.0	3.0	92	N
J108	NIP	8.0	—	—	—	—	—	—	80	25	10	3.0	3.0	92	N
J108-18	NIP	8.0	—	—	—	—	—	—	80	25	10	3.0	3.0	92	N
J109	NIP	12	—	—	—	—	—	—	40	25	6.0	3.0	3.0	92	N
J109-18	NIP	12	—	—	—	—	—	—	40	25	6.0	3.0	3.0	92	N
J110	NIP	18	—	—	—	—	—	—	10	25	4.0	3.0	3.0	92	N
J110-18	NIP	18	—	—	—	—	—	—	10	25	4.0	3.0	3.0	92	N
J111	NC	30	—	—	—	—	—	—	20	35	10	1.0	1.0	92	N
J111-18	NC	30	—	—	—	—	—	—	20	35	10	1.0	1.0	92	N
J112	NC	50	—	—	—	—	—	—	5.0	35	5.0	1.0	1.0	92	N
J112-18	NC	50	—	—	—	—	—	—	5.0	35	5.0	1.0	1.0	92	N
J113	NC	100	—	—	—	—	—	—	2.0	35	3.0	1.0	1.0	92	N
J113-18	NC	100	—	—	—	—	—	—	2.0	35	3.0	1.0	1.0	92	N
J174	PS	85	—	—	—	—	—	100	20	30	10	1.0	1.0	92	P
J174-18	PS	85	—	—	—	—	—	100	20	30	10	1.0	1.0	92	P
J175	PS	125	—	—	—	—	—	60	7.0	30	6.0	1.0	1.0	92	P
J175-18	PS	125	—	—	—	—	—	60	7.0	30	6.0	1.0	1.0	92	P
J176	PS	250	—	—	—	—	—	25	2.0	30	4.0	1.0	1.0	92	P
J176-18	PS	250	—	—	—	—	—	25	2.0	30	4.0	1.0	1.0	92	P
J177	PS	300	—	—	—	—	—	20	1.5	30	2.25	1.0	1.0	92	P
J177-18	PS	300	—	—	—	—	—	20	1.5	30	2.25	1.0	1.0	92	P
PN4391	NC	30	—	—	14	—	—	150	50	40	10	1.0	1.0	92	N
PN4391-18	NC	30	—	—	14	—	—	150	50	40	10	1.0	1.0	92	N
PN4392	NC	60	—	—	14	—	—	100	25	40	5.0	1.0	1.0	92	N
PN4392-18	NC	60	—	—	14	—	—	100	25	40	5.0	1.0	1.0	92	N
PN4393	NC	100	—	—	14	—	—	60	5.0	40	3.0	1.0	1.0	92	N
PN4393-18	NC	100	—	—	14	—	—	60	5.0	40	3.0	1.0	1.0	92	N
P1086	PS	75	—	—	45	—	—	—	10	30	10	10.0	2.0	92	P
P1086-18	PS	75	—	—	45	—	—	—	10	30	10	10.0	2.0	92	P

SMALL SIGNAL FET Product Specifications (Cont'd)

N & P-Channel Single JFETs

PART NUMBER	DEVICE	GEOMETRY (Section 4)	RESISTANCE Chnl Ω, Max.	RESISTANCE Gate Ω	NOISE VOLTAGE (nV/√Hz, MAX.) or (NF, dB, MAX.)	INPUT CAPACITANCE (pF, MAX.)	TRANS-CONDUCTANCE gfs (μmhos) Max.	TRANS-CONDUCTANCE gfs (μmhos) Min.	SATURATION CURRENT (mA) Max.	SATURATION CURRENT (mA) Min.	BREAKDOWN VOLTAGE (V, MAX.)	THRESHOLD VOLTAGE (V, MAX.)	LEAKAGE (nA, MAX.) Chnl	LEAKAGE (nA, MAX.) Gate	PACKAGE (TO-)	N or P
P1087	SWITCHES & CHOPPERS	PS	150	—	—	45	—	—	—	5.0	30	5.0	10.0	2.0	92	P
P1087-18		PS	150	—	—	45	—	—	—	5.0	30	5.0	10.0	2.0	92	P
SD210		DMCB-B	70	—	—	3.5	—	—	—	10	30	2.0	100	100	72	N
SD211		DMCB-A	70	—	—	3.5	—	—	—	10	30	2.0	100	100	72	N
SD212		DMCB-B	70	—	—	3.5	—	—	—	10	10	2.0	100	100	72	N
SD213		DMCB-A	70	—	—	3.5	—	—	—	10	10	2.0	100	100	72	N
SD214		DMCB-B	70	—	—	3.5	—	—	—	10	20	2.0	100	100	72	N
SD215		DMCB-A	70	—	—	3.5	—	—	—	10	20	2.0	100	100	72	N
U200		NC	150	—	—	30	—	—	25	3.0	30	3.0	1.0	1.0	18	N
U201		NC	75	—	—	30	—	—	75	15	30	5.0	1.0	1.0	18	N
U202		NC	50	—	—	30	—	—	150	30	30	10	1.0	1.0	18	N
U290		NVA	2.5	—	—	60	—	—	—	500	30	10	1.0	1.0	52	N
U291		NVA	7.0	—	—	60	—	—	—	200	30	4.5	1.0	1.0	52	N
U304		PS	85	—	—	27	—	—	90	30	30	10	0.5	0.5	18	P
U305		PS	110	—	—	27	—	—	60	15	30	6.0	0.5	0.5	18	P
U306		PS	175	—	—	27	—	—	25	5.0	30	4.0	0.5	0.5	18	P
U1897		NC	30	—	—	16	—	—	—	30	40	10	0.2	0.4	92	N
U1897-18		NC	30	—	—	16	—	—	—	30	40	10	0.2	0.4	92	N
U1898		NC	50	—	—	16	—	—	—	15	40	7.0	0.2	0.4	92	N
U1898-18		NC	50	—	—	16	—	—	—	15	40	7.0	0.2	0.4	92	N
U1899		NC	80	—	—	16	—	—	—	8.0	40	5.0	0.2	0.4	92	N
U1899-18		NC	80	—	—	16	—	—	—	8.0	40	5.0	0.2	0.4	92	N
2N2608	GENERAL PURPOSE	PC	—	1M	3	17	—	1000	4.5	0.9	30	4.0	—	10	18	P
2N2609		PD	—	1M	3	30	—	2500	10.0	2.0	30	4.0	—	30	18	P
2N2843		PC	—	1M	3	17	—	540	1.0	0.2	30	1.7	—	10	18	P
2N2844		PD	—	1M	3	30	—	1400	2.2	0.44	30	1.7	—	30	18	P
2N3329		PC	—	1M	3	20	2000	1000	3.0	1.0	20	5.0	—	10	72	P
2N3330		PC	—	1M	3	20	3000	1500	6.0	2.0	20	6.0	—	10	72	P
2N3331		PC	—	1M	4	20	4000	2000	15	5.0	20	8.0	—	10	72	P
2N3332		PC	—	1M	1	20	2200	1000	6.0	1.0	20	6.0	—	10	72	P
2N3368		NP	—	—	—	20	4000	1000	12	2.0	40	11.5	—	5.0	18	N
2N3369		NP	—	—	—	20	2500	600	2.5	0.5	40	6.5	—	5.0	18	N
2N3370		NP	—	—	—	20	2500	300	0.6	0.1	40	3.2	—	5.0	18	N
2N3382		PE	—	—	—	—	12500	4500	30	3.0	30	5.0	—	15	72	P
2N3384		PE	—	—	—	—	12500	7500	30	15.0	30	5.0	—	15	72	P
2N3386		PE	—	—	—	—	15000	7500	50	15.0	30	9.5	—	15	72	P

SMALL SIGNAL FET Product Specifications (Cont'd)

N & P-Channel Single JFETs

DEVICE: GENERAL PURPOSE

PART NUMBER	N or P	PACKAGE (TO-)	GEOMETRY (Section 4)	RESISTANCE Chnl Ω, Max.	RESISTANCE Gate Ω	NOISE VOLTAGE (nV/√Hz, MAX.) or (NF, dB, MAX.)	INPUT CAPACITANCE (pF, MAX.)	TRANS-CONDUCTANCE gfs (μmhos) Max.	TRANS-CONDUCTANCE gfs (μmhos) Min.	SATURATION CURRENT (mA) Max.	SATURATION CURRENT (mA) Min.	BREAKDOWN VOLTAGE (V, MAX.)	THRESHOLD VOLTAGE (V, MAX.)	LEAKAGE (nA, MAX.) Chnl	LEAKAGE (nA, MAX.) Gate
2N3821	N	72	NRL	–	–	200	6	4500	1500	2.5	0.5	50	4.0	–	0.1
2N3822	N	72	NRL	–	–	200	6	6500	3000	10	2.0	50	6.0	–	0.1
2N4220	N	72	NRL	–	–	–	6	4000	1000	3.0	0.5	30	4.0	–	0.1
2N4221	N	72	NRL	–	–	–	6	5000	2000	6.0	2.0	30	6.0	–	0.1
2N4222	N	72	NRL	–	–	–	6	6000	2500	15	5.0	30	8.0	–	0.1
2N5457	N	92	NRL	–	1M	3.0	7	5000	1000	5.0	1.0	25	6.0	–	1.0
2N5458	N	92	NRL	–	1M	3.0	7	5500	1500	9.0	2.0	25	7.0	–	1.0
2N5459	N	92	NRL	–	100M	3.0	7	6000	2000	16	4.0	25	8.0	–	1.0
J201	N	92	NP	–	–	–	5.0	–	500	1.0	0.2	40	1.5	–	0.1
J201-18	N	92	NP	–	–	–	5.0	–	500	1.00	0.2	40	1.5	–	0.1
J202	N	92	NP	–	–	–	5.0	–	1000	4.5	0.9	40	4.0	–	0.1
J202-18	N	92	NP	–	–	–	5.0	–	1000	4.5	0.9	40	4.0	–	0.1
J203	N	92	NP	–	–	–	5.0	–	1500	20	4.0	40	10	–	0.1
J203-18	N	92	NP	–	–	–	5.0	–	1500	20	4.0	40	10	–	0.1
J204	N	92	NP	–	–	–	5.0	–	–	3.0	1.2	25	2.0	–	0.1
J204-18	N	92	NP	–	–	–	5.0	–	–	3.0	1.2	25	2.0	–	0.1
J270	P	92	PS	–	–	–	–	18000	8000	50	6.0	30	4.5	–	0.2
J271-18	P	92	PS	–	–	–	–	18000	8000	50	6.0	30	4.5	–	0.2
PN4302	N	92	NP	–	1M	2.0	6	–	1000	5.0	0.5	30	4.0	–	1.0
PN4302-18	N	92	NP	–	1M	2.0	6.0	–	1000	5.0	0.5	30	4.0	–	1.0
PN4303	N	92	NP	–	1M	2.0	6	–	2000	10	4.0	30	6.0	–	1.0
PN4303-18	N	92	NP	–	1M	2.0	6.0	–	2000	10	4.0	30	6.0	–	1.0
PN4304	N	92	NP	–	1M	3.0	6	–	1000	15	0.5	30	10.0	–	1.0
PN4304-18	N	92	NP	–	1M	2.0	6.0	–	1000	15	0.5	30	10	–	1.0
PN5163	N	92	–	–	–	50.0	20	9000	2000	40.0	1.0	25	8.0	–	10
MPF109	N	92	NRL	–	1M	2.5	7.0	6000	800	24	0.5	25	8.0	–	1.0
MPF111	N	92	NRL	–	–	–	–	–	500	20	0.5	20	10	–	100

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SMALL SIGNAL FET Product Specifications (Cont'd)

N-Channel Dual JFETs

PART NUMBER	DEVICE	GEOMETRY (Section 4)	OUTPUT CONDUCTANCE gos (µmhos, MAX.)	THRESHOLD Temp Tracking µV/°C	THRESHOLD Static Match (mV, Max.)	NOISE VOLTAGE (nV/√Hz, MAX.) or (NF, dB, MAX.)	INPUT CAPACITANCE (pF, MAX.)	TRANS-CONDUCTANCE gfs (µmhos) Max.	TRANS-CONDUCTANCE gfs (µmhos) Min.	SATURATION CURRENT (mA) Max.	SATURATION CURRENT (mA) Min.	BREAKDOWN VOLTAGE (V, MAX.)	THRESHOLD VOLTAGE (V, MAX.)	LEAKAGE (nA, MAX.) Gate	PACKAGE (TO-)	N or P
2N5196	LOW LEAKAGE	NP-D	50	5.0	5.0	20	6.0	—	1000	7.0	0.7	50	4.0	0.025	71	N
2N5197	LOW LEAKAGE	NP-D	50	10	5.0	20	6.0	—	1000	7.0	0.7	50	4.0	0.025	71	N
2N5198	LOW LEAKAGE	NP-D	50	20	10	20	6.0	—	1000	7.0	0.7	50	4.0	0.025	71	N
2N5199	LOW LEAKAGE	NP-D	50	40	15	20	6.0	—	1000	7.0	0.7	50	4.0	0.025	71	N
2N5545	LOW LEAKAGE	NP-D	25	10	5.0	200	6.0	—	1500	8.0	0.5	50	4.5	0.1	71	N
2N5546	LOW LEAKAGE	NP-D	25	20	10	200	6.0	—	1500	8.0	0.5	50	4.5	0.1	71	N
2N5547	LOW LEAKAGE	NP-D	25	40	15	200	6.0	—	1500	8.0	0.5	50	4.5	0.1	71	N
2N5902	LOW LEAKAGE	NT	1.0	5.0	5.0	0.2	3.0	—	70	0.5	0.03	40	4.5	0.005	78	N
2N5903	LOW LEAKAGE	NT	1.0	10	5.0	0.2	3.0	—	70	0.5	0.03	40	4.5	0.005	78	N
2N5904	LOW LEAKAGE	NT	1.0	20	10	0.2	3.0	—	70	0.5	0.03	40	4.5	0.005	78	N
2N5905	LOW LEAKAGE	NT	1.0	40	15	0.2	3.0	—	70	0.5	0.03	40	4.5	0.005	78	N
2N5906	LOW LEAKAGE	NT	1.0	5.0	5.0	0.1	3.0	—	70	0.5	0.03	40	4.5	0.002	78	N
2N5907	LOW LEAKAGE	NT	1.0	10	5.0	0.1	3.0	—	70	0.5	0.03	40	4.5	0.002	78	N
2N5908	LOW LEAKAGE	NT	1.0	20	10	0.1	3.0	—	70	0.5	0.03	40	4.5	0.002	78	N
2N5909	LOW LEAKAGE	NT	1.0	20	15	0.1	3.0	—	70	0.5	0.03	40	4.5	0.002	78	N
U401	LOW LEAKAGE	NNR	2.0	10	5.0	20	8.0	—	2000	10	0.5	50	2.5	0.025	71	N
U402	LOW LEAKAGE	NNR	2.0	10	10	20	8.0	—	2000	10	0.5	50	2.5	0.025	71	N
U403	LOW LEAKAGE	NNR	2.0	25	10	20	8.0	—	2000	10	0.5	50	2.5	0.025	71	N
U404	LOW LEAKAGE	NNR	2.0	25	15	20	8.0	—	2000	10	0.5	50	2.5	0.025	71	N
U405	LOW LEAKAGE	NNR	2.0	40	20	20	8.0	—	2000	10	0.5	50	2.5	0.025	71	N
U406	LOW LEAKAGE	NNR	2.0	80	40	20	8.0	—	2000	10	0.5	50	2.5	0.025	71	N
U421	LOW LEAKAGE	NNT	0.5	10	10	10	3.0	1500	300	1.0	0.06	40	2.0	0.001	78	N
U422	LOW LEAKAGE	NNT	0.5	25	15	10	3.0	1500	300	1.0	0.06	40	2.0	0.001	78	N
U423	LOW LEAKAGE	NNT	0.5	40	25	10	3.0	1500	300	1.0	0.06	40	2.0	0.001	78	N
U424	LOW LEAKAGE	NNT	1.0	10	10	10	3.0	1500	300	1.8	0.06	40	3.0	0.003	78	N
U425	LOW LEAKAGE	NNT	1.0	25	15	10	3.0	1500	300	1.8	0.06	40	3.0	0.003	78	N
U426	LOW LEAKAGE	NNT	1.0	40	25	10	3.0	1500	300	1.8	0.06	40	3.0	0.003	78	N
U427	LOW LEAKAGE	NNT	3.0	40	25	—	3.0	—	250	1.8	0.06	40	2.0	0.005	78	N
U428	LOW LEAKAGE	NNT	5.0	80	40	—	3.0	—	250	1.8	0.06	40	3.0	0.005	78	N
2N5515	LOW NOISE	NS or NQP	1.0	5.0	5.0	30	25	—	1000	7.5	0.5	40	4.0	0.25	71	N
2N5516	LOW NOISE	NS or NQP	1.0	10	5.0	30	25	—	1000	7.5	0.5	40	4.0	0.25	71	N
2N5517	LOW NOISE	NS or NQP	1.0	20	10	30	25	—	1000	7.5	0.5	40	4.0	0.25	71	N
2N5518	LOW NOISE	NS or NQP	1.0	40	15	30	25	—	1000	7.5	0.5	40	4.0	0.25	71	N
2N5519	LOW NOISE	NS or NQP	1.0	80	15	30	25	—	1000	7.5	0.5	40	4.0	0.25	71	N
2N5520	LOW NOISE	NS or NQP	1.0	5.0	5.0	15	25	—	1000	7.5	0.5	40	4.0	0.25	71	N
2N5521	LOW NOISE	NS or NQP	1.0	10	5.0	15	25	—	1000	7.5	0.5	40	4.0	0.25	71	N
2N5522	LOW NOISE	NS or NQP	1.0	20	10	15	25	—	1000	7.5	0.5	40	4.0	0.25	71	N
2N5523	LOW NOISE	NS or NQP	1.0	40	15	15	25	—	1000	7.5	0.5	40	4.0	0.25	71	N
2N5524	LOW NOISE	NS or NQP	1.0	80	15	15	25	—	1000	7.5	0.5	40	4.0	0.25	71	N
U401	LOW NOISE	NNR	2.0	10	5.0	20	8.0	—	2000	10	0.5	50	2.5	0.025	71	N
U402	LOW NOISE	NNR	2.0	10	10	20	8.0	—	2000	10	0.5	50	2.5	0.025	71	N

N-Channel Dual JFETs

PART NUMBER	N or P	PACKAGE (TO-)	LEAKAGE (nA, MAX.) Gate	THRESHOLD VOLTAGE (V, MAX.)	BREAKDOWN VOLTAGE (V, MAX.)	SATURATION CURRENT (mA) Min.	SATURATION CURRENT (mA) Max.	TRANS-CONDUCTANCE gfs (μmhos) Min.	TRANS-CONDUCTANCE gfs (μmhos) Max.	INPUT CAPACITANCE (pF, MAX.)	NOISE VOLTAGE (nV/√Hz, MAX.) or (NF, dB, MAX.)	THRESHOLD Static Match (mV, Max.)	THRESHOLD Temp Tracking μV/°C	OUTPUT CONDUCTANCE gos (μmhos, MAX.)	GEOMETRY (Section 4)	DEVICE
U404	N	71	0.025	2.5	50	0.5	10	2000	–	8.0	20	15	25	2.0	NNR	LOW NOISE
U405	N	71	0.025	2.5	50	0.5	10	2000	–	8.0	20	20	40	2.0	NNR	
U406	N	71	0.025	2.5	50	0.5	10	2000	–	8.0	20	40	80	2.0	NNR	
2N5564	N	71	0.1	3.0	40	5.0	30	7500	–	12	50	5.0	10	45	NC	RF AMPLIFIER
2N5565	N	71	0.1	3.0	40	5.0	30	7500	–	12	50	10	25	45	NC	
2N5566	N	71	0.1	3.0	40	5.0	30	7500	–	12	50	20	50	45	NC	
2N5911	N	78	0.1	5.0	25	7.0	40	5000	–	3.0	20	10	20	100	NZF	
2N5912	N	78	0.1	5.0	25	7.0	40	5000	–	3.0	20	15	40	100	NZF	
U257	N	78	0.1	5.0	25	5.0	40	5000	–	5.0	30	100	–	150	NZF	
U430	N	99	0.15	4.0	25	12	30	10000	–	7.5	12	–	–	150	NZA	
U431	N	99	0.15	6.0	25	24	60	10000	–	7.5	10	–	–	150	NZA	
U440	N	71	0.50	6.0	25	6.0	30	4500	–	3.5	–	10	–	200	NZF	
U441	N	71	0.50	6.0	25	6.0	30	4500	–	3.5	–	20	–	200	NZF	
U443	N	78	.5	6	25	6.0	30	4500	9000	3.5	–	10	–	200	NZF	
U444	N	78	.5	6	25	6.0	30	4500	9000	3.5	–	20	–	200	NZF	
2N3921	N	71	1.0	3.0	50	1.0	10	1500	–	18	2.0	5.0	10	35	NNR or NRL-D	GENERAL PURPOSE
2N3922	N	71	1.0	3.0	50	1.0	10	1500	–	18	2.0	5.0	25	35	NNR or NRL-D	
2N3954	N	71	0.1	4.5	50	0.5	5.0	1000	–	4.0	0.5	5.0	10	35	NQP	
2N3954A	N	71	0.1	4.5	50	0.5	5.0	1000	–	4.0	0.5	5.0	5.0	35	NQP	
2N3955	N	71	0.1	4.5	50	0.5	5.0	1000	–	4.0	0.5	10	25	35	NQP	
2N3955A	N	71	0.1	4.5	50	0.5	5.0	1000	–	4.0	0.5	10	15	35	NQP	
2N3956	N	71	0.1	4.5	50	0.5	5.0	1000	–	4.0	0.5	15	50	35	NQP	
2N3957	N	71	0.1	4.5	50	0.5	5.0	1000	–	4.0	0.5	20	75	35	NQP	
2N3958	N	71	0.1	4.5	50	0.5	5.0	1000	–	4.0	0.5	25	100	35	NQP	
2N4084	N	71	1.0	3.0	50	1.0	10	1500	–	18	2	15	10	35	NNR or NRL-D	
2N4085	N	71	1.0	3.0	50	1.0	10	1500	–	18	2	15	25	35	NNR or NRL-D	
2N5045	N	71	0.25	4.5	50	0.5	8.0	1500	–	8.0	200	5.0	67	25	NNR or NRL-D	
2N5046	N	71	0.25	4.5	50	0.5	8.0	1500	–	8.0	200	10	133	25	NNR or NRL-D	
2N5047	N	71	0.25	4.5	50	0.5	8.0	1500	–	8.0	200	15	200	25	NNR or NRL-D	
2N5452	N	71	0.1	4.5	50	0.5	5.0	1000	–	4.0	20	5.0	5.0	1.0	NQP	
2N5453	N	71	0.1	4.5	50	0.5	5.0	1000	–	4.0	20	10	10	1.0	NQP	
2N5454	N	71	0.1	4.5	50	0.5	5.0	1000	–	4.0	20	15	25	1.0	NQP	
DN5564	N	71	.1	3.0	40	5	50	7500	12500	12	50	5	10	65	NC	
DN5565	N	71	.1	3.0	40	5	50	7500	12500	12	50	10	25	65	NC	
DN5566	N	71	.1	3.0	40	5	50	7500	12500	12	50	20	50	65	NC	
U231	N	71	0.1	4.5	50	0.5	5.0	1000	–	6.0	80	5.0	10	35	NP-D	
U232	N	71	0.1	4.5	50	0.5	5.0	1000	–	6.0	80	10	25	35	NP-D	
U233	N	71	0.1	4.5	50	0.5	5.0	1000	–	6.0	80	15	50	35	NP-D	
U234	N	71	0.1	4.5	50	0.5	5.0	1000	–	6.0	80	20	75	35	NP-D	
U235	N	71	0.1	4.5	50	0.5	5.0	1000	–	6.0	80	25	100	35	NP-D	
U410	N	71	0.2	3.5	40	0.5	6.0	1000	–	–	13	10	10	20	NQP	
U411	N	71	0.2	3.5	40	0.5	6.0	1000	–	–	13	20	25	20	NQP	
U412	N	71	0.2	3.5	40	0.5	6.0	1000	–	–	13	40	80	20	NQP	
DN5567	N	71	0.1	3.0	–40	5	60	–	–	7.0	–	20	–	–	NC	SWITCH

Product Specifications (Cont'd)

Low Leakage Diodes

Part Number	Package (TO-)	Diode	Reverse Current (pA, Max.)	Breakdown Voltage (Volts)		Forward Voltage Drop Volts (Max.)	Capacitance (pF, Max.)
				Min.	Max.		
DPAD1	78	Dual	1	45	120	1.5	0.8
DPAD2	72	Dual	2	45	120	1.5	0.8
DPAD5	72	Dual	5	45	120	1.5	0.8
DPAD10	72	Dual	10	35	–	1.5	2.0
DPAD20	72	Dual	20	35	–	1.5	2.0
DPAD50	72	Dual	50	35	–	1.5	2.0
DPAD100	72	Dual	100	35	–	1.5	2.0
JPAD2	92	Single	2	35	–	1.5	2.0
JPAD5	92	Single	5	35	–	1.5	2.0
JPAD10	92	Single1	10	35	–	1.5	2.0
JPAD20	92	Single	20	35	–	1.5	2.0
JPAD50	TO-92	Single	20	35	–	1.5	2.0
JPAD100	TO-92	Single	50	35	–	1.5	2.0
JPAD200	TO-92	Single	100	35	–	1.5	2.0
JPAD500	TO-92	Single	500	35	–	1.5	2.0
PAD1	18	Single	1	45	120	1.5	0.8
PAD2	18	Single	2	45	120	1.5	0.8
PAD5	18	Single	5	45	120	1.5	0.8
PAD10	18	Single	10	35	–	1.5	2.0
PAD20	18	Single	20	35	–	1.5	2.0
PAD50	18	Single	50	35	–	1.5	2.0
PAD100	18	Single	100	35	–	1.5	2.0

Voltage Controlled Resistors

Part Number	N or P	Package (TO-)	Breakdown Voltage (Volts, Min.)	Threshold Voltage (Volts)		Resistance (Channel Ω)		Geometry
				Min.	Max.	Min.	Max.	
VCR2N	N	18	15	3.5	7.0	20	60	NC
VCR3P	P	72	15	3.5	7.0	70	200	PE
VCR4N	N	18	15	3.5	7.0	200	600	NP
VCR5P	P	72	15	3.5	7.0	300	900	PC
VCR7N	N	72	15	2.5	5.0	4000	8000	NT
VCR11N	N	71	30	8.0	12.0	100	200	NS

P-Channel MOSFETs

Part Number	Package (TO-)	Operating Mode	Threshold Voltage (Volts, Max.)	Resistance Channel (Ω, Max.)	Leakage Channel On (mA)		Leakage Channel Off (nA, Max.)	Breakdown Voltage (Volts, Max.)	Input Capacitance (pF, Max.)	Reverse Capacitance (pF, Max.)	Geometry
					Min.	Max.					
3N163	72	ENH	5.0	250	5.0	30	–	40	2.5	0.7	MRA
3N164	72	ENH	5.0	300	3.0	30	–	30	2.5	0.7	MRA
MFE823	18	ENH	6.0	–	3.0	–	20	25	6.0	1.5	MRA

Product Specifications (Cont'd)

Current Regulator Diodes

Part Number	Package (TO-)	Forward Current (mA)	Forward Current Tolerance (%)	Limiting Voltage (Volts, Max.)	Peak Operating Voltage (Volts, Max.)	Dynamic Impedance (MΩ, Max.)	Forward Capacitance (pF, typ)	Geometry
CR022	18	0.22	10	1.00	100	13	–	NKL
CR024	18	0.24	10	1.00	100	10	–	NKL
CR027	18	0.27	10	1.00	100	9.0	–	NKL
CR030	18	0.30	10	1.00	100	8.0	–	NKL
CR033	18	0.33	10	1.00	100	6.6	–	NKL
CR039	18	0.39	10	1.05	100	4.1	–	NKL
CR043	18	0.43	10	1.05	100	3.3	–	NKL
CR047	18	0.47	10	1.10	100	2.7	–	NKL
CR056	18	0.56	10	1.20	100	1.9	–	NKL
CR062	18	0.62	10	1.30	100	1.55	–	NKL
CR068	18	0.68	10	1.15	100	1.35	–	NKM
CR075	18	0.75	10	1.20	100	1.15	–	NKM
CR082	18	0.82	10	1.25	100	1.00	–	NKM
CR091	18	0.91	10	1.29	100	0.88	–	NKM
CR100	18	1.00	10	1.35	100	0.80	–	NKM
CR110	18	1.10	10	1.40	100	0.70	–	NKM
CR120	18	1.20	10	1.45	100	0.64	–	NKM
CR130	18	1.30	10	1.50	100	0.58	–	NKM
CR140	18	1.40	10	1.55	100	0.54	–	NKM
CR150	18	1.50	10	1.60	100	0.51	–	NKM
CR160	18	1.60	10	1.65	100	0.475	–	NKO
CR180	18	1.80	10	1.75	100	0.42	–	NKO
CR200	18	2.00	10	1.85	100	0.395	–	NKO
CR220	18	2.20	10	1.95	100	0.37	–	NKO
CR240	18	2.40	10	2.00	100	0.345	–	NKO
CR270	18	2.70	10	2.15	100	0.32	–	NKO
CR300	18	3.00	10	2.25	100	0.30	–	NKO
CR330	18	3.30	10	2.35	100	0.28	–	NKO
CR360	18	3.60	10	2.50	100	0.265	–	NKO
CR390	18	3.90	10	2.60	100	0.255	–	NKO
CR430	18	4.30	10	2.75	100	0.245	–	NKO
CR470	18	4.70	10	2.90	100	0.235	–	NKO
CRR0240	18	.24	25	1.0	100	.9	–	NKL
CRR0360	18	.36	25	1.05	100	4.1	–	NKL
CRR0560	18	.56	25	1.30	100	1.15	–	NKL
CRR0800	18	.80	25	1.35	100	0.8	–	NKL
CRR1250	18	1.95	25	1.60	100	.54	–	NKM
CRR1950	18	1.95	25	1.95	100	.37	–	NKM
CRR2900	18	2.90	25	2.35	100	.28	–	NKO
CRR4300	18	4.30	25	3.00	100	0.5	–	NKO
J500	92	0.24	20	1.20	50	5.0	2	NCL
J501	92	0.33	20	1.30	50	3.0	2	NCL
J502	92	0.43	20	1.50	50	2.0	2	NCL
J503	92	0.56	20	1.70	50	1.4	2	NCL
J504	92	0.75	20	1.90	50	1.0	2	NCL
J505	92	1.00	20	2.10	50	0.6	2	NCL
J506	92	1.40	20	2.50	50	0.4	2	NCL
J507	92	1.80	20	2.80	50	0.25	2	NCL
J508	92	2.40	20	3.10	50	0.25	2	NCL
J509	92	3.00	20	3.50	50	0.20	2	NCL
J510	92	3.60	20	3.90	50	0.20	2	NCL
J511	92	4.70	20	4.20	50	0.15	2	NCL
J552	92	0.05	50	1.5	50	2.0	2	NKL
J553	92	(.18 - 0.75)	–	.75	50	10	–	NCL
J554	92	(06 -1.6)	–	.75	50	1.0	–	NCL
J555	92	(1.4 - 2.6)	–	.75	50	.88	–	NCL
J556	92	(2.4 - 3.8)	–	.75	50	.6	–	NCL
J557	92	(3.6 - 5.3)	–	1.5	50	.48	–	NCL
J9100	92	0.05	50	1.5	50	2.0	2	NCL
JR135V	92	0.200	–	0.9	135	2.0	–	VRMA
JR170V	92	0.200	–	0.9	170	2.0	–	VRMA
JR200V	92	0.200	–	0.9	200	2.0	–	VRMA
JR220V	92	0.200	–	0.9	220	2.0	–	VRMA
JR240V	92	0.200	–	0.9	240	2.0	–	VRMA

SMALL SIGNAL FETs Additional Product Options for European Customers

CECC 50 000

CECC 50 000 is a European system of continuous product assessment intended to produce electronic components of assessed quality to specifications and procedures which conform to internationally recognized standards. Components produced under the system are accepted by all participating countries without further testing being necessary.

At this time, member countries of the CECC are Belgium, Denmark, Germany, France, Ireland, Italy, the Netherlands, Norway, Sweden, Switzerland and the United Kingdom.

Under this assessment scheme, devices are manufactured on an approved line to nationally approved specifications written in accordance with CECC rules. The manufacturer must comply with defined standards relating to organization, facilities and quality control procedures.

Specific device types are individually qualified against a fixed detail specification which has been approved by the British Standards Institute acting as the national supervising agency on behalf of CECC.

The CECC 50 000 scheme is administered in the UK by the BSI, and UK generated specifications are prefixed with the letters BS.

A number of popular standard device types are now qualified and the following detail specifications are available:

Type Number	BS Specification
2N3970/1/2	BS CECC 50012-001
2N4091/2/3	BS CECC 50012-002
2N4391/2/3	BS CECC 50012-004
2N4856/7/8	BS CECC 50012-005
2N4859/60/61	BS CECC 50012-005
2N4856A/7A/8A	BS CECC 50012-006
2N4859A/60A/61A	BS CECC 50012-006
2N3821/2	BS CECC 50012-007
2N3824	BS CECC 50012-008
2N4220/1/2	BS CECC 50012-009
2N4220/1A/2A	BS CECC 50012-009

Each of the approved types is now available with additional screening options, including high temperature reverse bias burn-in, of either 48, 72 or 168 hours duration. Screening details are appended to the detail specification and conform to appendix VI of the European Standard CECC 50 0000 ISSUE 3.

Product is released with a BS CECC certificate of conformity and will have been submitted to:

1. Group A sample inspection (lot by lot)
   quality assessment tests, assuring product conforms to electrical specification.
2. Group B sample inspection (lot by lot)
   reliability tests, including package related tests and 168 hours electrical endurance, to identify potential early failures.
3. Group C sample inspection (periodic—3 monthly)
   long term reliability tests including 1000 hours of high temperature storage and electrical endurance.

Data from the inspection tests is available to the customer in the form of CTRs (certified test records).

Manufacturing of BS CECC product is carried out at the Siliconix UK facility located in Morriston, Swansea SA6 6NE, South Wales

In addition to BS CECC approved product, the Siliconix UK facility can provide internationally recognized high-reliability screening options on standard products. These include Mil-750B and custom screening options.

JAN, JANTX or JANTXV processing for certain JEDEC-registered FETs can also be supplied.

For additional information, enquiries may be directed to the nearest field sales office.

SMALL SIGNAL FET Process Option Flow

The Small Signal FET Process Option Flow Chart shows the standard screening options provided by Siliconix for Integrated Circuits

Column 2: Equivalent to MIL-STD-19500 JANTX flow.

Column 2A: Equivalent to MIL-STD-19500 JANTX flow with the exception of Preseal Inspection being a Siliconix internal specification versus MIL-STD-19500 M-2072 as in −2 flow.

Column 3: All metal can product is processed to one −3 flow.

Column 4: All plastic TO-92 product is processed to one −4 flow.

SMALL SIGNAL FET Process Option Flow Chart

-2 (JANTXV Equiv)	-2A (JANTX Equiv)	-3 (Hermetic Package)	-4 (Plastic Package)
Preseal Inspection Method 2072	Preseal Inspection Siliconix Visual	Preseal Inspection Siliconix Visual	Preseal Inspection Siliconix Visual
Stabilization Bake Method 1031 24 hour @ 200°C	Stabilization Bake Method 1031 24 hour @ 200°C	Stabilization Method 1031 24 hour @ 150°C	
Temperature Cycle Method 1051, Condition C 5 Cycles −65°C to +200°C @ Temperature Extremes	Temperature Cycle Method 1051, Condition C 5 Cycles −65°C to +200°C @ Temperature Extremes	LTPD = 20 Temperature Cycle Method 1051, Condition C 5 Cycles −65°C to +200°C @ Temperature Extremes	
Constant Acceleration Method 2006 Y1 Axis 30,000 G	Constant Acceleration Method 2006 Y1 Axis 30,000 G		
Fine Leak Method 1071, Condition H or G Maximum Leak Rate	Fine Leak Method 1071, Condition H or G Maximum Leak Rate	Fine Leak Method 1071, Condition H or G Maximum Leak Rate	
Gross Leak Method 1071, Condition C	Gross Leak Method 1071, Condition C	Gross Leak Method 1071, Condition C	
Electrical Test 100% to Static Parameters @ 25°C	Electrical Test 100% to Static Parameters @ 25°C	Electrical Test 100% to Static Parameters @ 25°C	Electrical Test 100% to Static Parameters @ 25°C
HTRB Burn-In Method 1039, Condition A 168 hour @ 150°C	HTRB Burn-In Method 1039, Condition A 168 hour @ 150°C		
Electrical Test 100% to Static Parameters @ 25°C	Electrical Test 100% to Static Parameters @ 25°C		
Quality Conformance 25°C Static LTPD = 5 −55°C Static LTPD = 5 150°C Static LTPD = 5 25°C 1 KHz Dynamic LTPD = 10 External Visual LTPD = 5	Quality Conformance 25°C Static AQL .65% 25°C 1 KHz Dynamic AQL 1.0% External Visual LTPD = 10	Quality Conformance 25°C Static AQL .65% 25°C 1 KHz Dynamic AQL 1.0% External Visual LTPD = 10	Quality Conformance 25°C Static AQL .65% External Visual LTPD = 10

NOTES:
Processing and test methods are MIL-STD-750 unless specified otherwise.

How to Use the SMALL SIGNAL FET Cross Reference

The following examples illustrate how the FET Cross Reference and Index should be used:

Case (1) Recommended replacement offered by Siliconix is identical to Industry Part Number.

Industry Part Number	Type and Classification	Recommended Replacement
2N4391	N JFET	2N4391

Case (2) Recommended replacement offered by Siliconix is not identical to Industry Part Number.

Industry Part Number	Type and Classification	Recommended Replacement
2N3457	N JFET	2N4338

The recommended replacement may be exact, tighter or looser on electrical characteristics, and may be a different package or pin-out. Data sheets for both parts should, if possible, be reviewed for a complete comparison. Send for *your* new November, 1982 Small Signal FET Design Catalog.

Type and classification abbreviations are described as follows:

BF (JFET Plastic)
CR (Current Limited)
CRR (Current Limiter)
D (Dual)
DN (Dual N-Channel Metal Can)
DPAD (Dual Pico Ampere Diode)
FN (N-Channel Metal Can)
ENH (Enhancement-Mode Normally-Off)
JPAD (Plastic Pico Ampere Diode)
JR (Plastic High Voltage Diode)
N (N-Channel)
P (P-Channel)
PAD (Pico Ampere Diode)
SD (N-Channel DMOS)
MOSPOWER

SMALL SIGNAL FET Cross Reference

Industry Part Number	Type and Classification	Recommended Replacement	Data Sheet Page	Geometry Page
1N5283	CL N JFET	CR022		
1N5284	CL N JFET	CR024		
1N5285	CL N JFET	CR027		
1N5286	CL N JFET	CR030		
1N5287	CL N JFET	CR033		
1N5288	CL N JFET	CR039		
1N5289	CL N JFET	CR043		
1N5290	CL N JFET	CR047		
1N5291	CL N JFET	CR056		
1N5292	CL N JFET	CR062		
1N5293	CL N JFET	CR068		
1N5294	CL N JFET	CR075		
1N5295	CL N JFET	CR082		
1N5296	CL N JFET	CR091		
1N5297	CL N JFET	CR100		
1N5298	CL N JFET	CR110		
1N5299	CL N JFET	CR120		
1N5300	CL N JFET	CR130		
1N5301	CL N JFET	CR140		
1N5302	CL N JFET	CR150		
1N5303	CL N JFET	CR160		
1N5304	CL N JFET	CR180		
1N5305	CL N JFET	CR200		
1N5306	CL N JFET	CR220		
1N5307	CL N JFET	CR240		
1N5308	CL N JFET	CR270		
1N5309	CL N JFET	CR300		
1N5310	CL N JFET	CR330		
1N5311	CL N JFET	CR360		
1N5312	CL N JFET	CR390		
1N5313	CL N JFET	CR430		
1N5314	CL N JFET	CR470		
2N2386	P JFET	2N2608		
2N2386A	P JFET	2N2609		
2N2497	P JFET	2N3329		
2N2498	P JFET	2N3330		
2N2499	P JFET	2N3331		
2N2500	P JFET	2N3332		
2N2606	P JFET	2N2608		
2N2606JAN	P JFET	2N2608JAN		
2N2607	P JFET	2N2608		
2N2607JAN	P JFET	2N2608JAN		
2N2608	P JFET	2N2608		
2N2608JAN	P JFET	2N2608JAN		
2N2609	P JFET	2N2609		
2N2609JAN	P JFET	2N2609JAN		
2N2841	P JFET	2N3329		
2N2842	P JFET	2N3329		
2N2843	P JFET	2N3329		
2N2844	P JFET	2N2608		
2N3066	N JFET	2N4340		
2N3067	N JFET	2N4338		
2N3068	N JFET	2N4338		
2N3069	N JFET	2N4341		
2N3070	N JFET	2N4339		

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Industry Part Number	Type and Classification	Recommended Replacement	Data Sheet Page	Geometry Page
2N3071	N JFET	2N4338		
2N3084	N JFET	2N4341		
2N3085	N JFET	2N4341		
2N3086	N JFET	2N4341		
2N3087	N JFET	2N4341		
2N3088	N JFET	2N4339		
2N3088A	N JFET	2N4339		
2N3089	N JFET	2N4339		
2N3089A	N JFET	2N4339		
2N3113	P JFET	2N3329		
2N3277	P JFET	2N2608		
2N3278	P JFET	2N2608		
2N3328	P JFET	2N3438		
2N3329	P JFET	2N3329		
2N3330	P JFET	2N3330		
2N3331	P JFET	2N3331		
2N3332	P JFET	2N3332		
2N3365	N JFET	2N4340		
2N3366	N JFET	2N4338		
2N3367	N JFET	2N4338		
2N3368	N JFET	2N4341		
2N3369	N JFET	2N4340		
2N3370	N JFET	2N4339		
2N3376	P JFET	2N3329		
2N3378	P JFET	2N3330		
2N3380	P JFET	2N3331		
2N3382	P JFET	2N3382		
2N3384	P JFET	2N3384		
2N3386	P JFET	2N3386		
2N3436	N JFET	2N4341		
2N3437	N JFET	2N4341		
2N3438	N JFET	2N4341		
2N3452	N JFET	2N4340		
2N3453	N JFET	2N4338		
2N3454	N JFET	2N4338		
2N3455	N JFET	2N4340		
2N3456	N JFET	2N4338		
2N3457	N JFET	2N4338		
2N3458	N JFET	2N4341		
2N3459	N JFET	2N4341		
2N3460	N JFET	2N4340		
2N3574	P JFET	2N3329		
2N3575	P JFET	2N3329		
2N3578	P JFET	2N2608		
2N3608	P MOS ENH	3N163		
2N3684	N JFET	2N4339		
2N3685	N JFET	2N4339		
2N3686	N JFET	2N4340		
2N3687	N JFET	2N4341		
2N3819	N JFET	2N3819		
2N3820	P JFET	J270		
2N3821	N JFET	2N3821		
2N3822	N JFET	2N3822		
2N3823	N JFET	2N3823		
2N3824	N JFET	2N3824		

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SMALL SIGNAL FET Cross Reference (Cont'd)

Industry Part Number	Type and Classification	Recommended Replacement	Data Sheet Page	Geometry Page
2N3909	P JFET	2N2608		
2N3909A	P JFET	2N3909		
2N3921	D N JFET	2N3921		
2N3922	D N JFET	2N3922		
2N3954	D N JFET	2N3954		
2N3954A	D N JFET	2N3954A		
2N3955	D N JFET	2N3955		
2N3955A	D N JFET	2N3955A		
2N3956	D N JFET	2N3956		
2N3957	D N JFET	2N3957		
2N3958	D N JFET	2N3958		
2N3966	N JFET	2N3966		
2N3967	N JFET	2N4221		
2N3967A	N JFET	2N4221		
2N3968	N JFET	2N4339		
2N3968A	N JFET	2N4339		
2N3969	N JFET	2N4339		
2N3969A	N JFET	2N3686		
2N3970	N JFET	2N3970		
2N3971	N JFET	2N3971		
2N3972	N JFET	2N3972		
2N3993	P JFET	2N3386		
2N3993A	P JFET	2N3386		
2N3994	P JFET	2N3382		
2N3994A	P JFET	2N3382		
2N4084	D N JFET	2N4084		
2N4085	D N JFET	2N4085		
2N4091	N JFET	2N4091		
2N4091A	N JFET	2N4091		
2N4092	N JFET	2N4092		
2N4092A	N JFET	2N4092		
2N4093	N JFET	2N4093		
2N4093A	N JFET	2N4093		
2N4117	N JFET	2N4117		
2N4117A	N JFET	2N4117A		
2N4118	N JFET	2N4118		
2N4118A	N JFET	2N4118A		
2N4119	N JFET	2N4119		
2N4119A	N JFET	2N4119A		
2N4120	P MOS ENH	3N163		
2N4139	N JFET	2N3822		
2N4220	N JFET	2N4220		
2N4220A	N JFET	2N4220A		
2N4221	N JFET	2N4221		
2N4221A	N JFET	2N4221A		
2N4222	N JFET	2N4222		
2N4222A	N JFET	2N4222A		
2N4223	N JFET	2N4223		
2N4224	N JFET	2N4224		
2N4267	P MOS ENH	3N163		
2N4302	N JFET	PN4302-18		
2N4303	N JFET	PN4303-18		
2N4304	N JFET	PN4304-18		
2N4338	N JFET	2N4338		
2N4339	N JFET	2N4339		

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Industry Part Number	Type and Classification	Recommended Replacement	Data Sheet Page	Geometry Page
2N4340	N JFET	2N4340		
2N4341	N JFET	2N4341		
2N4352	P MOS ENH	3N163		
2N4381	P JFET	2N2609		
2N4382	P JFET	2N5115		
2N4391	N JFET	2N4391		
2N4392	N JFET	2N4392		
2N4393	N JFET	2N4393		
2N4416	N JFET	2N4416		
2N4416A	N JFET	2N4416A		
2N4445	N JFET	2N5432		
2N4446	N JFET	2N5433		
2N4447	N JFET	2N5432		
2N4448	N JFET	2N5433		
2N4856	N JFET	2N4856		
2N4856A	N JFET	2N4856A		
2N4856JAN	N JFET	2N4856JAN		
2N4856JANTX	N JFET	2N4856JANTX		
2N4856JANTXV	N JFET	2N4856JANTXV		
2N4857	N JFET	2N4857		
2N4857A	N JFET	2N4857A		
2N4857JAN	N JFET	2N4857JAN		
2N4857JANTX	N JFET	2N4857JANTX		
2N4857JANTXV	N JFET	2N4857JANTXV		
2N4858	N JFET	2N4858		
2N4858A	N JFET	2N4858A		
2N4858JAN	N JFET	2N4858JAN		
2N4858JANTX	N JFET	2N4858JANTX		
2N4858JANTXV	N JFET	2N4858JANTXV		
2N4859	N JFET	2N4859		
2N4859A	N JFET	2N4859A		
2N4859JAN	N JFET	2N4859JAN		
2N4859JANTX	N JFET	2N4859JANTX		
2N4859JANTXV	N JFET	2N4859JANTXV		
2N4860	N JFET	2N4860		
2N4860A	N JFET	2N4860A		
2N4860JAN	N JFET	2N4860JAN		
2N4860JANTX	N JFET	2N4860JANTX		
2N4860JANTXV	N JFET	2N4860JANTXV		
2N4861	N JFET	2N4861		
2N4861A	N JFET	2N4861A		
2N4861JAN	N JFET	2N4861JAN		
2N4861JANTX	N JFET	2N4861JANTX		
2N4861JANTXV	N JFET	2N4861JANTXV		
2N4867	N JFET	2N4867		
2N4867A	N JFET	2N4867A		
2N4868	N JFET	2N4868		
2N4868A	N JFET	2N4868A		
2N4869	N JFET	2N4869		
2N4869A	N JFET	2N4869A		
2N4977	N JFET	2N5432		
2N4978	N JFET	2N5433		
2N4979	N JFET	2N5434		
2N5018	P JFET	2N5018		
2N5019	P JFET	2N5019		

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SMALL SIGNAL FET Cross Reference (Cont'd)

Industry Part Number	Type and Classification	Recommended Replacement	Data Sheet Page	Geometry Page
2N5020	P JFET	2N3329		
2N5021	P JFET	2N2608		
2N5033	P JFET	2N2608		
2N5045	D N JFET	2N5045		
2N5046	D N JFET	2N5046		
2N5047	D N JFET	2N5047		
2N5103	N JFET	2N4416		
2N5104	N JFET	2N4416		
2N5105	N JFET	2N4416		
2N5114	P JFET	2N5114		
2N5115	P JFET	2N5115		
2N5116	P JFET	2N5116		
2N5158	N JFET	2N5434		
2N5159	N JFET	2N5433		
2N5196	D N JFET	2N5196		
2N5197	D N JFET	2N5197		
2N5198	D N JFET	2N5198		
2N5199	D N JFET	2N5199		
2N5245	N JFET	PN4416		
2N5246	N JFET	J305-18		
2N5247	N JFE	J304-18		
2N5248	N JFET	2N5486		
2N5257	N JFET	2N5457		
2N5258	N JFET	2N5458		
2N5259	N JFET	2N5459		
2N5265	P JFET	2N2608		
2N5266	P JFET	2N2608		
2N5267	P JFET	2N2608		
2N5268	P JFET	2N2608		
2N5269	P JFET	2N3331		
2N5270	P JFET	2N3331		
2N5358	N JFET	2N4340		
2N5359	N JFET	2N4340		
2N5360	N JFET	2N4339		
2N5361	N JFET	2N4339		
2N5362	N JFET	2N4339		
2N5363	N JFET	2N4222A		
2N5364	N JFET	2N4224		
2N5391	N JFET	2N4867A		
2N5392	N JFET	2N4868A		
2N5393	N JFET	2N4869A		
2N5394	N JFET	2N4869A		
2N5395	N JFET	2N4869A		
2N5396	N JFET	2N4869A		
2N5397	N JFET	U310		
2N5398	N JFET	U312		
2N5432	N JFET	2N5432		
2N5433	N JFET	2N5433		
2N5434	N JFET	2N5434		
2N5452	D N JFET	2N5452		
2N5453	D N JFET	2N5453		
2N5454	D N JFET	2N5454		
2N5457	N JFET	2N5457		
2N5458	N JFET	2N5458		
2N5459	N JFET	2N5459		

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Industry Part Number	Type and Classification	Recommended Replacement	Data Sheet Page	Geometry Page
2N5484	N JFET	2N5484		
2N5485	N JFET	2N5485		
2N5486	N JFET	2N5486		
2N5515	D N JFET	2N5515		
2N5516	D N JFET	2N5516		
2N5517	D N JFET	2N5517		
2N5518	D N JFET	2N5518		
2N5519	D N JFET	2N5519		
2N5520	D N JFET	2N5520		
2N5521	D N JFET	2N5521		
2N5522	D N JFET	2N5522		
2N5523	D N JFET	2N5523		
2N5524	D N JFET	2N5524		
2N5545	D N JFET	2N5545		
2N5546	D N JFET	2N5546		
2N5547	D N JFET	2N5547		
2N5549	N JFET	2N4392		
2N5561	D N JFET	U401		
2N5562	D N JFET	U402		
2N5563	D N JFET	U404		
2N5564	D N JFET	2N5564		
2N5565	D N JFET	2N5565		
2N5566	D N JFET	2N5566		
2N5592	N JFET	2N3822		
2N5593	N JFET	2N3822		
2N5594	N JFET	2N3822		
2N5638	N JFET	2N5638		
2N5639	N JFET	2N5639		
2N5640	N JFET	2N5640		
2N5647	N JFET	2N4117A		
2N5648	N JFET	2N4117A		
2N5649	N JFET	2N4117A		
2N5797	P JFET	2N2608		
2N5798	P JFET	2N2608		
2N5799	P JFET	2N2608		
2N5800	P JFET	2N2608		
2N5801	N JFET	2N4393		
2N5802	N JFET	2N4393		
2N5803	N JFET	2N4392		
2N5902	D N JFET	2N5902		
2N5903	D N JFET	2N5903		
2N5904	D N JFET	2N5904		
2N5905	D N JFET	2N5905		
2N5906	D N JFET	2N5906		
2N5907	D N JFET	2N5907		
2N5908	D N JFET	2N5908		
2N5909	D N JFET	2N5909		
2N5911	D N JFET	2N5911		
2N5912	D N JFET	2N5912		
2N5949	N JFET	PN4416		
2N5950	N JFET	PN4416		
2N5951	N JFET	PN4416		
2N5952	N JFET	J305		
2N5953	N JFET	J305		
2N6451	N JFET	2N4393		
2N6452	N JFET	2N4393		

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SMALL SIGNAL FET Cross Reference (Cont'd)

Industry Part Number	Type and Classification	Recommended Replacement	Data Sheet Page	Geometry Page
2N6453	N JFET	2N4393	Refer to the 1982 Small Signal FET Design Catalog	
2N6454	N JFET	2N4393		
2N6483	D N JFET	U401		
2N6484	D N JFET	U402		
2N6585	D N JFET	U404		
2N6568	N JFET	U290		
2N6656	V MOS N ENH	2N6656		
2N6657	V MOS N ENH	2N6657		
2N6658	V MOS N ENH	2N6658		
2N6659	V MOS N ENH	2N6659		
2N6660	V MOS N ENH	2N6660		
2N6661	V MOS N ENH	2N6661		
3N145	P MOS ENH	3N163		
3N146	P MOS ENH	3N163		
3N155	P MOS ENH	3N163		
3N155A	P MOS ENH	3N163		
3N156	P MOS ENH	3N163		
3N156A	P MOS ENH	3N163		
3N157	P MOS ENH	3N163		
3N157A	P MOS ENH	3N163		
3N158	P MOS ENH	3N163		
3N158A	P MOS ENH	3N163		
3N163	P MOS ENH	3N163		
3N164	P MOS ENH	3N164		
3N174	P MOS ENH	3N163		
14T	N JFET	2N3819		
142T	N JFET	PN4392		
158T	N JFET	PN4302		
159T	N JFET	PN4416		
100S	N JFET	PN4304		
100U	N JFET	2N3684		
102M	N JFET	2N5486		
102S	N JFET	2N4302		
103M	N JFET	2N5457		
103S	N JFET	2N5459		
104M	N JFET	2N5458		
105M	N JFET	2N5459		
105U	N JFET	2N4222		
106M	N JFET	2N5485		
107M	N JFET	2N5486		
110U	N JFET	2N4339		
115U	N JFET			
120U	N JFET	2N4340		
125U	N JFET	2N4339		
130U	N JFET	2N4341		
135U	N JFET	2N4339		
155U	N JFET	2N4416		
182S	N JFET	2N4391		
183S	N JFET	2N3823		
197S	N JFET	2N4338		
198S	N JFET	2N4340		
199S	N JFET	2N4341		
200S	N JFET	2N4392		
200U	N JFET	2N3824		
201S	N JFET	2N4391		

Industry Part Number	Type and Classification	Recommended Replacement	Data Sheet Page	Geometry Page
202S	N JFET	2N4392	Refer to the 1982 Small Signal FET Design Catalog	
203S	N JFET	2N3821		
204S	N JFET	2N3821		
210U	N JFET	2N4416		
231S	D N JFET	2N3954		
232S	D N JFET	2N3955		
233S	D N JFET	2N3956		
234S	D N JFET	2N3957		
235S	D N JFET	2N3958		
241U	N JFET	2N4869		
250U	N JFET	2N4091		
251U	N JFET	2N4392		
703U	N JFET	2N4220		
704U	N JFET	2N4220		
705U	N JFET	2N4224		
707U	N JFET	2N4860		
714U	N JFET	2N3822		
734U	N JFET	2N4416		
734EU	N JFET	PN4416		
751U	N JFET	2N4340		
752U	N JFET	2N4340		
753U	N JFET	2N4341		
754U	N JFET	2N4340		
755U	N JFET	2N4341		
756U	N JFET	2N4340		
1277A	N JFET	2N3822		
1278A	N JFET	2N3821		
1279A	N JFET	2N3821		
1280A	N JFET	2N4224		
1281A	N JFET	2N3822		
1282A	N JFET	2N4341		
1283A	N JFET	2N4340		
1284A	N JFET	2N4222		
1285A	N JFET	2N3821		
1286A	N JFET	2N4220		
1325A	N JFET	2N4222		
1714A	N JFET	2N4340		
2000M	N JFET	2N3823		
2001M	N JFET	2N3823		
2078A	D N JFET	2N3955		
2079A	D N JFET	2N3955		
2080A	D N JFET	2N5546		
2081A	D N JFET	2N5546		
2093M	N JFET	2N3687		
2094M	N JFET	2N3686		
2095M	N JFET	2N3686		
2098A	D NJFET	2N5545		
2099A	D N JFET	2N5546		
2130U	D N JFET	2N5452		
2132U	D N JFET	2N3955		
2134U	D N JFET	2N3956		
2136U	D N JFET	2N3957		
2138U	D N JFET	2N3958		
2139U	D N JFET	2N3958		
2147U	D N JFET	2N3958		

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Industry Part Number	Type and Classification	Recommended Replacement	Data Sheet Page	Geometry Page
2148U	D N JFET	2N3958	Refer to the 1982 Small Signal FET Design Catalog	
2149U	D N JFET	2N3958		
A5T3821	N JFET	J305		
A5T3822	N JFET	J305		
A5T3823	N JFET	PN4416		
A5T3824	N JFET	J302-18		
A192	N JFET	2N4416		
AD830	D N JFET	U421		
AD831	D N JFET	U421		
AD832	D N JFET	U422		
AD833	D N JFET	U426		
AD833A	D N JFET	U423		
AD835	D N JFET	2N3921		
AD836	D N JFET	2N3921		
AD837	D N JFET	2N3922		
AD838	D N JFET	2N4085		
AD839	D N JFET	2N4085		
AD840	D N JFET	2N5196		
AD841	D N JFET	2N5197		
AD842	D N JFET	2N5199		
AD3954	D N JFET	2N3954		
AD3954A	D N JFET	2N3954A		
AD3955	D N JFET	2N3955		
AD3956	D N JFET	2N3956		
AD3957	D N JFET	2N3957		
AD3958	D N JFET	2N3958		
BC264	N JFET	PN4304		
BC264A	N JFET	PN4302		
BC264B	N JFET	PN4304		
BC264C	N JFET	PN4304		
BC264D	N JFET	PN4416		
BF244A/B/C*	N JFET	*Contact factory		
BF245A/B/C*	D N JFET	*Contact factory		
BFR45	D N JFET	2N4416		
BFS21	N JFET	2N5199		
BFS21A	D N JFET	2N5199		
BFS67	N JFET	2N3821		
BFS67P	N JFET	2N4303		
BFS68	N JFET	2N3823		
BFS68P	N JFET	PN4416		
BFS70	N JFET	2N3821		
BFS71	N JFET	2N3822		
BFS72	N JFET	2N3823		
BFS73	N JFET	2N3821		
BFS74	N JFET	2N4856		
BFS75	N JFET	2N4857		
BFS76	N JFET	2N4858		
BFS77	N JFET	2N4859		
BFS78	N JFET	2N4860		
BFS79	N JFET	2N4861		
BFS80	N JFET	2N4416A		
BFW10	N JFET	2N3823		
BFW11	N JFET	2N3822		
BFW54	N JFET	2N3822		
BFW55	N JFET	2N3822		
BFW56	N JFET	2N4869	Refer to the 1982 Small Signal FET Design Catalog	
BFW61	N JFET	2N4224		
BSV22	N JFET	2N4416		
BSV78	N JFET	2N4856A		
BSV80	N JFET	2N4858A		
C413N	N JFET	2N5434		
C673	N JFET	2N4341		
C674	N JFET	2N4341		
C680	N JFET	2N4338		
C680A	N JFET	2N4338		
C681	N JFET	2N4338		
C681A	N JFET	2N4338		
C682	N JFET	2N4339		
C682A	N JFET	2N4339		
C683	N JFET	2N4339		
C683A	N JFET	2N4339		
C684	N JFET	2N4220		
C684A	N JFET	2N4220		
C685	N JFET	2N4220		
C685A	N JFET	2N4220		
C6690	N JFET	2N4341		
C6691	N JFET	2N4341		
C6692	N JFET	2N4340		
CM600	N JFET	2N4092		
CM601	N JFET	2N4091		
CM602	N JFET	2N4091		
CM603	N JFET	2N4091		
CM640	N JFET	2N4093		
CM641	N JFET	2N4093		
CM642	N JFET	2N4093		
CM643	N JFET	2N4092		
CM644	N JFET	2N4092		
CM645	N JFET	2N4092		
CM646	N JFET	2N4092		
CM647	N JFET	2N4091		
CM650	N JFET	2N5432		
CM651	N JFET	2N5433		
CM652	N JFET	2N5432		
CM653	N JFET	2N5433		
CM697	N JFET	2N5434		
CM800	N JFET	2N5434		
CMX740	N JFET	U290		
CP640	N JFET	U296		
CP643	N JFET	2N5434		
CP650	N JFET	U322		
CP651	N JFET	U320		
CP652	N JFET	U322		
CP653	N JFET	U320		
CR022 Thru CR470 Referenced Under 1N Series				
CRR0240-4300	CL N FET	CRR0240-4300		
DN5564-66	D N JFET	DN5564-66		
DN5567	D N JFET	DN5567		
DPAD1	D PAD N JFET	DPAD1		
DPAD2	D PAD N JFET	DPAD2		
DPAD5	D PAD N JFET	DPAD5		

SMALL SIGNAL FET Cross Reference (Cont'd)

Industry Part Number	Type and Classification	Recommended Replacement	Data Sheet Page	Geometry Page
DPAD10	D PAD N JFET	DPAD10		
DPAD20	D PAD N JFET	DPAD20		
DPAD50	D PAD N JFET	DPAD50		
DPAD100	D PAD N JFET	DPAD100		
DU4339	D N JFET	U235		
DU4340	D N JFET	U235		
E100	N JFET	J203-18		
E101	N JFET	J201-18		
E102	N JFET	J202-18		
E103	N JFET	J105-18		
E105	N JFET	J105-18		
E106	N JFET	J106-18		
E107	N JFET	J107-18		
E108	N JFET	J108-18		
E109	N JFET	J109-18		
E110	N JFET	J110-18		
E111	N JFET	J111-18		
E112	N JFET	J112-18		
E113	N JFET	J113-18		
E114	N JFET	J114		
E174	P JFET	J174-18		
E175	P JFET	J175-18		
E176	P JFET	J176-18		
E177	P JFET	J177-18		
E201	N JFET	J201-18		
E202	N JFET	J202-18		
E203	N JFET	J203-18		
E204	N JFET	J204-18		
E210	N JFET	J210		
E211	N JFET	J211		
E212	N JFET	J212		
E230	N JFET	J230-18		
E231	N JFET	J231-18		
E232	N JFET	J232-18		
E270	P JFET	J270-18		
E271	P JFET	J271-18		
E300	N JFET	J300		
E304	N JFET	J304		
E305	N JFET	J305		
E308	N JFET	J308		
E309	N JFET	J309		
E310	N JFET	J310		
E400	D N JFET	U410		
E401	D N JFET	U411		
E402	D N JFET	U410		
E410	D N JFET	U410		
E411	D N JFET	U411		
E412	D N JFET	U412		
E413	D N JFET	U410		
E414	D N JFET	U411		
E415	D N JFET	U412		
E420	D N JFET	U440		
E421	D N JFET	U441		
E430	D N JFET	U430		
E431	D N JFET	U431		

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Industry Part Number	Type and Classification	Recommended Replacement	Data Sheet Page	Geometry Page
E500	CL N JFET	J500		
E501	CL N JFET	J501		
E502	CL N JFET	J502		
E503	CL N JFET	J503		
E504	CL N JFET	J504		
E505	CL N JFET	J505		
E506	CL N JFET	J506		
E507	CL N JFET	J507		
EPAD50	DD N JFET	JPAD50		
EPAD100	DD N JFET	JPAD100		
EPAD200	DD N JFET	JPAD200		
EPAD500	DD N JFET	JPAD500		
FE100	N JFET	2N3821		
FE100A	N JFET	2N3821		
FE102	N JFET	2N4119		
FE102A	N JFET	2N4119		
FE104	N JFET	2N4118		
FE104A	N JFET	2N4118		
FE200	N JFET	2N3821		
FE202	N JFET	2N3821		
FE204	N JFET	2N3821		
FE300	N JFET	2N3822		
FE302	N JFET	2N3821		
FE304	N JFET	2N3821		
FE0654A	N JFET	2N5486		
FE0654B	N JFET	2N5485		
FE3819	N JFET	2N3819		
FE5457	N JFET	2N5457		
FE5458	N JFET	2N5458		
FE5459	N JFET	2N5459		
FE5484	N JFET	2N5484		
FE5485	N JFET	2N5485		
FE5486	N JFET	2N5486		
FM3954	D N JFET	2N3954		
FM3954A	D N JFET	2N3954A		
FM3955	D N JFET	2N3955		
FM3955A	D N JFET	2N3955A		
FM3956	D N JFET	2N3956		
FM3957	D N JFET	2N3957		
FM3958	D N JFET	2N3958		
FN4117	N J FET	FN4117		
FN4117A	N J FET	FN4117A		
FN4118	N J FET	FN4118		
FN4118A	N J FET	FN4118A		
FN4119	N J FET	FN4119		
FN4119A	N J FET	FN4119A		
FN4392	N J FET	FN4392		
FN4393	N J FET	FN4393		
FT0654A	N JFET	2N5486		
FT0654B	N JFET	2N5486		
FT0654C	N JFET	2N4221		
FT0654D	N JFET	2N4221		
FT704	P MOS ENH	3N163		

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SMALL SIGNAL FET Cross Reference (Cont'd)

Industry Part Number	Type and Classification	Recommended Replacement	Data Sheet Page	Geometry Page
GET5457	N JFET	2N5457		
GET5458	N JFET	2N5458		
GET5459	N JFET	2N5459		
HDIG1030	P MOS ENH	3N163		
ID100	D PAD N JFET	DPAD1		
ID101	D PAD N JFET	DPAD10		
IMF3954	D N JFET	2N3954		
IMF3954A	D N JFET	2N3954A		
IMF3955	D N JFET	2N3955		
IMF3955A	D N JFET	2N3955A		
IMF3956	D N JFET	2N3956		
IMF3957	D N JFET	2N3957		
IMF3958	D N JFET	2N3958		
IMF6485	D N JFET	U405		
IT100	P JFET	2N5116		
IT101	P JFET	2N5114		
IT108	N JFET	2N5486		
IT109	N JFET	U310		
IT1700	P MOS ENH	3N163		
IT1702	P MOSENH	3N163		
ITE500	CL N JFET	J500		
ITE501	CL N JFET	J501		
ITE502	CL N JFET	J502		
ITE503	CL N JFET	J503		
ITE504	CL N JFET	J504		
ITE505	CL N JFET	J505		
ITE506	CL N JFET	J506		
ITE507	CL N JFET	J507		
ITE3066	N JFET	J202-18		
ITE3067	N JFET	J201-18		
ITE3068	N JFET	J201-18		
ITE4117	N JFET	2N4117		
ITE4118	N JFET	2N4118		
ITE4119	N JFET	2N4119		
ITE4338	N JFET	J201-18		
ITE4339	N JFET	J201-18		
ITE4340	N JFET	J202-18		
ITE4341	N JFET	J203-18		
ITE4391	N JFET	PN4391-18		
ITE4392	N JFET	PN4392-18		
ITE4393	N JFET	PN4393-18		
ITE4416	N JFET	PN4416		
ITE4867	N JFET	J230-18		
ITE4868	N JFET	J231-18		
ITE4869	N JFET	J232-18		
J105	N JFET	J105		
J105-18	N JFET	J105-18		
J106	N JFET	J106		
J106-18	N JFET	J106-18		
J107	N JFET	J107		
J107-18	N JFET	J107-18		
J108	N JFET	J108		
J108-18	N JFET	J108-18		
J109	N JFET	J109		
J109-18	N JFET	J109-18		

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Industry Part Number	Type and Classification	Recommended Replacement	Data Sheet Page	Geometry Page
J110	N JFET	J110		
J110-18	N JFET	J110-18		
J111	N JFET	J111		
J111-18	N JFET	J111-18		
J112	N JFET	J112		
J112-18	N JFET	J112-18		
J113	N JFET	J113		
J113-18	N JFET	J113-18		
J174	P JFET	J174		
J174-18	P JFET	J174-18		
J175	P JFET	J175		
J175-18	P JFET	J175-18		
J176	P JFET	J176		
J176-18	P JFET	J176-18		
J177	P JFET	J177		
J177-18	P JFET	J177-18		
J201	N JFET			
J201-18	N JFET			
J202	N JFET			
J202-18	N JFET			
J203	N JFET			
J203-18	N JFET			
J204	N JFET	J204		
J204-18	N JFET	J204-18		
J210	N JFET	J210		
J211	N JFET	J211		
J212	N JFET	J212		
J230	N JFET	J230		
J230-18	N JFET	J230-18		
J231	N JFET	J231		
J231-18	N JFET	J231-18		
J232	N JFET	J232		
J232-18	N JFET	J232-18		
J270	P JFET	J270		
J270-18	P JFET	J270-18		
J271	P JFET	J271		
J271-18	P JFET	J271-18		
J300	N JFET	J300		
J300A/B/C/D	N JFET	J300A/B/C/D		
J304	N JFET	J304		
J305	N JFET	J305		
J308	N JFET	J308		
J309	N JFET	J309		
J310	N JFET	J310		
J401	D N JFET	U401		
J402	D N JFET	U402		
J403	D N JFET	U403		
J404	D N JFET	U404		
J405	D N JFET	U405		
J406	D N JFET	U406		
J410	D N JFET	U410		
J411	D N JFET	U411		
J412	D N JFET	U412		
J500	CL N JFET	J500		
J501	CL N JFET	J501		

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Industry Part Number	Type and Classification	Recommended Replacement	Data Sheet Page	Geometry Page
J502	CL N JFET	J502		
J503	CL N JFET	J503		
J504	CL N JFET	J504		
J505	CL N JFET	J505		
J506	CL N JFET	J506		
J507	CL N JFET	J507		
J508	CL N JFET	J508		
J509	CL N JFET	J509		
J510	CL N JFET	J510		
J511	CL N JFET	J511		
J552	CL N JFET	J552		
J553	CL N JFET	J553		
J554	CL N JFET	J554		
J555	CL N JFET	J555		
J556	CL N JFET	J556		
J557	CL N JFET	J557		
JPAD5	PAD N JFET	JPAD5		
JPAD10	PAD N JFET	JPAD10		
JPAD20	PAD N JFET	JPAD20		
JPAD50	PAD N JFET	JPAD50		
JPAD100	PAD N JFET	JPAD100		
JPAD200	PAD NJFET	JPAD200		
JPAD500	PAD N JFET	JPAD500		
JR135V	CL N JFET	JR135V		
JR170V	CL N JFET	JR170V		
JR200V	CL N JFET	JR200V		
JR220V	CL N JFET	JR220V		
JR240V	CL N JFET	JR240V		
J1401	D N JFET	U401		
J1402	D N JFET	U402		
J1403	D N JFET	U403		
J1404	D N JFET	U404		
J1405	D N JFET	U405		
J1406	D N JFET	U406		
J9100	CL N JFET	J9100		
K210-18	N JFET	J210		
K211-18	N JFET	J211		
K212-18	N JFET	J212		
K300-18	N JFET	J210		
K304-18	N JFET	J304		
K305-18	N JFET	J305		
K308-18	N JFET	J308		
K309-18	N JFET	J309		
K310-18	N JFET	J310		
KE3684	N JFET	2N3684		
KE3685	N JFET	2N3685		
KE3686	N JFET	2N3686		
KE3687	N JFET	2N3687		
KE3823	N JFET	J304-18		
KE3970	N JFET	PN4391-18		
KE3971	N JFET	PN4392-18		
KE3972	N JFET	PN4393-18		
KE4091	N JFET	PN4391-18		
KE4092	N JFET	PN4392-18		
KE4093	N JFET	PN4393-18		
KE4220	N JFET	2N5457		
KE4221	N JFET	2N5457		
KE4222	N JFET	2N5459		
KE4223	N JFET	J304-18		
KE4224	N JFET	J304-18		
KE4391	N JFET	PN4391-18		
KE4392	N JFET	PN4392-18		
KE4393	N JFET	PN4393-18		
KE4416	N JFET	PN4416		
KE4856	N JFET	PN4391-18		
KE4857	N JFET	PN4392-18		
KE4858	N JFET	PN4393-18		
KE4859	N JFET	PN4391-18		
KE4860	N JFET	PN4392-18		
KE4861	N JFET	PN4393-18		
KE5103	N JFET	J305		
KE5104	N JFET	J304		
KE5105	N JFET	J306		
KK4416-18	N JFET	PN4416		
LDF603	N JFET	2N4221A		
LDF604	N JFET	2N4221A		
LDF605	N JFET	2N4221A		
M163	P MOS ENH	3N163		
M164	P MOS ENH	3N164		
MEM520	P MOS ENH	3N164		
MEM520C	P MOS ENH	3N164		
MEM561	P MOS ENH	3N163		
MEM561C	P MOS ENH	3N163		
MEM806	P MOS ENH	3N163		
MEM806A	P MOS ENH	3N163		
MFE823	P MOS ENH	MFE823		
MFE2000	N JFET	2N4416		
MFE2001	N JFET	2N4416		
MFE2004	N JFET	2N4093		
MFE2005	N JFET	2N4092		
MFE2006	N JFET	2N4091		
MFE2007	N JFET	2N4860		
MFE2008	N JFET	2N4859		
MFE2009	N JFET	2N4859		
MFE2010	N JFET	2N5434		
MFE2011	N JFET	2N5433		
MFE2012	N JFET	2N5432		
MFE2093	N JFET	2N3687		
MFE2094	N JFET	2N3686		
MFE2095	N JFET	2N3685		
MFE4007	P JFET	2N2608		
MFE4008	P JFET	2N2608		
MFE4009	P JFET	2N3329		
MFE4010	P JFET	2N3330		
MFE4011	P JFET	2N3330		
MFE4012	P JFET	2N3331		
MK10	N JFET	2N4416		
MMF1	D N JFET	2N3921		
MMF2	D N JFET	2N3921		
MMF3	D N JFET	2N3921		
MMF4	D N JFET	2N3921		
MMF5	D N JFET	2N3921		
MMF6	D N JFET	2N3921		
MMT3823	N JFET	2N3823		
MPF102	N JFET	MPF102		
MPF103	N JFET	2N5457		
MPF104	N JFET	2N5458		
MPF105	N JFET	2N5459		
MPF106	N JFET	2N5485		
MPF107	N JFET	2N5486		
MPF108	N JFET	MPF108		
MPF109	N JFET	MPF109		
MPF111	N JFET	MPF111		

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Industry Part Number	Type and Classification	Recommended Replacement	Data Sheet Page	Geometry Page
MPF112	N JFET	MPF112	Refer to the 1982 Small Signal FET Design Catalog	
MPF256	N JFET	J309		
MPF820	N JFET	U310		
MPF970	P JFET	J174		
MPF971	P JFET	J176		
MPF4391	N JFET	PN4391-18		
MPF4392	N JFET	PN4392-18		
MPF4393	N JFET	PN4393-18		
NF500	N JFET	2N4416		
NF501	N JFET	2N4416		
NF506	N JFET	2N4416		
NF510	N JFET	2N4393		
NF511	N JFET	2N4393		
NF520	N JFET	2N4339		
NF521	N JFET	2N4339		
NF522	N JFET	2N4339		
NF523	N JFET	2N4340		
NF530	N JFET	2N4341		
NF531	N JFET	2N4339		
NF532	N JFET	2N4341		
NF533	N JFET	2N4339		
NF580	N JFET	2N5432		
NF581	N JFET	2N5432		
NF582	N JFET	2N5433		
NF583	N JFET	2N5434		
NF584	N JFET	2N5433		
NF585	N JFET	2N4859		
NF4302	N JFET	2N4302		
NF4303	N JFET	2N4303		
NF4304	N JFET	2N4304		
NF4445	N JFET	2N5432		
NF4446	N JFET	2N5433		
NF4447	N JFET	2N5432		
NF4448	N JFET	2N5433		
NF5163	N JFET	2N5163		
NF5457	N JFET	2N5457		
NF5458	N JFET	2N5458		
NF5459	N JFET	2N5459		
NF5484	N JFET	2N5484		
NF5485	N JFET	2N5485		
NF5486	N JFET	2N5486		
NF5555	N JFET	2N5555		
NF5638	N JFET	2N5638		
NF5639	N JFET	2N5639		
NF5640	N JFET	2N5640		
NF5653	N JFET	2N5653		
NF5654	N JFET	2N5654		
PAD1	PAD N JFET	PAD1		
PAD2	PAD N JFET	PAD2		
PAD5	PAD N JFET	PAD5		
PAD10	PAD N JFET	PAD10		
PAD20	PAD N JFET	PAD20		
PAD50	PAD N JFET	PAD50		
PAD100	PAD N JFET	PAD100		
P1086	P JFET	P1086		
P1086-18	P JFET	P1086-18	Refer to the 1982 Small Signal FET Design Catalog	
P1087	P JFET	P1087		
P1087-18	P JFET	P1087-18		
PN4091	N JFET	PN4091		
PN4092	N JFET	PN4092		
PN4093	N JFET	PN4093		
PN4117	N JFET	PN4117		
PN4117A	N JFET	PN4117A		
PN4118	N JFET	PN4118		
PN4118A	N JFET	PN4118A		
PN4119	N JFET	PN4119		
PN4119A	N JFET	PN4119A		
PN4120	N JFET	PN4120		
PN4120A	N JFET	PN4120A		
PN4302	N JFET	PN4302		
PN4302-18	N JFET	PN4302-18		
PN4303	N JFET	PN4303		
PN4303-18	N JFET	PN4303-18		
PN4304	N JFET	PN4304		
PN4304-18	N JFET	PN4304-18		
PN4391	N JFET	PN4391		
PN4391-18	N JFET	PN4391-18		
PN4392	N JFET	PN4392		
PN4392-18	N JFET	PN4392-18		
PN4393	N JFET	PN4393		
PN4393-18	N JFET	PN4393-18		
PN4416	N JFET	PN4416		
PN5163	N JFET	PN5163		
PF510	P JFET	2N5018		
PF511	P JFET	2N5014		
SD210DE	D N JFET	SD210DE		
SD211DE	D N JFET	SD211DE		
SD212DE	D N JFET	SD212DE		
SD213DE	D N JFET	SD213DE		
SD214DE	D N JFET	SD214DE		
SD215DE	D N JFET	SD215DE		
SU2078	D N JFET	U425		
SU2079	D N JFET	U425		
SU2098	D N JFET	2N5197		
SU2098A	D N JFET	2N5197		
SU2098B	D N JFET	2N5196		
SU2099	D N JFET	2N5197		
SU2099A	D N JFET	2N5197		
SU2365	D N JFET	U401		
SU2365A	D N JFET	U401		
SU2366	D N JFET	U402		
SU2366A	D N JFET	U402		
SU2367	D N JFET	U403		
SU2367A	D N JFET	U403		
SU2368	D N JFET	U404		
SU2368A	D N JFET	U404		
SU2369	D N JFET	U405		
SU2369A	D N JFET	U405		
SU2410	D N JFET	U424		

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Industry Part Number	Type and Classification	Recommended Replacement	Data Sheet Page	Geometry Page
SU2411	D N JFET	U425		
SU2412	D N JFET	U426		
TD5902	D N JFET	2N5902		
TD5902	D N JFET	2N5902		
TD5902A	D N JFET	2N5902		
TD5903	D N JFET	2N5903		
TD5903A	D N JFET	2N5903		
TD5904	D N JFET	2N5904		
TD5904A	D N JFET	2N5904		
TD5905	D N JFET	2N5905		
TD5905A	D N JFET	2N5905		
TD5906	D N JFET	2N5906		
TD5906A	D N JFET	2N5906		
TD5907	D N JFET	2N5907		
TD5907A	D N JFET	2N5907		
TD5908	D N JFET	2N5908		
TD5908A	D N JFET	2N5908		
TD5909	D N JFET	2N5909		
TD5909A	D N JFET	2N5909		
TD5911	D N JFET	2N5911		
TD5911A	D N JFET	2N5911		
TD5912	D N JFET	2N5912		
TD5912A	D N JFET	2N5912		
TIS14	N JFET	2N4340		
TIS25	D N JFET	U401		
TIS26	D N JFET	U402		
TIS27	D N JFET	U404		
TIS41	N JFET	2N4859		
TIS58	N JFET	J305-18		
TIS59	D N JFET	U1837		
TIS73	N JFET	PN4391-18		
TIS74	N JFET	PN4392-18		
TIS75	N JFET	PN4393-18		
TIS88	N JFET	2N5486		
TIXS41	N JFET	2N4859		
TIXS42	N JFET	PN4393-18		
TN4117	N JFET	2N4117		
TN4117A	N JFET	2N4117A		
TN4118	N JFET	2N4118		
TN4118A	N JFET	2N4118A		
TN4119	N JFET	2N4119		
TN4119A	N JFET	2N4119A		
TN4338	N JFET	2N4338		
TN4339	N JFET	2N4339		
TN4340	N JFET	2N4340		
TN4341	N JFET	2N4341		
TP5114	P JFET	2N5114		
TP5115	P JFET	2N5115		
TP5116	P JFET	2N5116		
U110	P JFET	2N2608		
U112	P JFET	2N2608		
U133	P JFET	2N2608		
U146	P JFET	2N2608		
U147	P JFET	2N2608		
U148	P JFET	2N2608		

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Industry Part Number	Type and Classification	Recommended Replacement	Data Sheet Page	Geometry Page
U149	P JFET	2N2609		
U168	P JFET	2N2609		
U182	N JFET	2N4857		
U183	N JFET	2N3824		
U197	N JFET	2N4339		
U198	N JFET	2N4340		
U199	N JFET	2N4341		
U200	N JFET	U200		
U201	N JFET	U201		
U202	N JFET	U202		
U221	N JFET	2N4391		
U222	N JFET	2N4391		
U231	D N JFET	U231		
U232	D N JFET	U232		
U233	D N JFET	U233		
U234	D N JFET	U234		
U235	D N JFET	U235		
U240	N JFET	2N5432		
U241	N JFET	2N5433		
U242	N JFET	2N5432		
U243	N JFET	2N5433		
U248	D N JFET	2N5902		
U248A	D N JFET	2N5906		
U249	D N JFET	2N5903		
U249A	D N JFET	2N5907		
U250	D N JFET	2N5904		
U250A	D N JFET	2N5908		
U251	D N JFET	2N5905		
U251A	D N JFET	2N5909		
U254	N JFET	2N4859		
U255	N JFET	2N4860		
U256	N JFET	2N4861		
U257	D N JFET	U257		
U273	N JFET	2N4118A		
U273A	N JFET	2N4118A		
U274	N JFET	2N4119A		
U274A	N JFET	2N4119A		
U275	N JFET	2N4119A		
U275A	N JFET	2N4119A		
U280	D N JFET	U231		
U281	D N JFET	U231		
U282	D N JFET	U232		
U283	D N JFET	U232		
U284	D N JFET	U233		
U285	D N JFET	U234		
U290	N JFET	U290		
U291	N JFET	U291		
U295	N JFET	U295		
U296	N JFET	U296		
U300	P JFET	2N5114		
U301	P JFET	2N5115		
U304	P JFET	U304		
U305	P JFET	U305		
U306	P JFET	U306		
U308	N JFET	U308		

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Industry Part Number	Type and Classification	Recommended Replacement	Data Sheet Page	Geometry Page
U309	N JFET	U309	Refer to the 1982 Small Signal FET Design Catalog	
U310	N JFET	U310		
U311	N JFET	U311		
U320	N JFET	U290		
U321	N JFET	U291		
U322	N JFET	U290		
U401	D N JFET	U401		
U402	D N JFET	U402		
U403	D N JFET	U403		
U404	D N JFET	U404		
U405	D N JFET	U405		
U406	D N JFET	U406		
U410	D N JFET	U410		
U411	D N JFET	U411		
U412	D N JFET	U412		
U421	D N JFET	U421		
U422	D N JFET	U422		
U423	D N JFET	U423		
U424	D N JFET	U424		
U425	D N JFET	U425		
U426	D N JFET	U426		
U427	D N JFET	U427		
U428	D N JFET	U428		
U430	D N JFET	U430		
U431	D N JFET	U431		
U440	D N JFET	U440		
U441	D N JFET	U441		
U443	D N JFET	U443		
U444	D N JFET	U444		
U508	N JFET	CR030		
U1177	N JFET	2N4220A		
U1178	N JFET	2N3821		
U1179	N JFET	2N3821		
U1180	N JFET	2N4221A		
U1181	N JFET	2N4220A		
U1182	N JFET	2N3821		
U1277	N JFET	2N4339		
U1278	N JFET	2N4339		
U1279	N JFET	2N4340		
U1280	N JFET	2N4339		
U1281	N JFET	2N3822		
U1282	N JFET	2N4341		
U1283	N JFET	2N4340		
U1284	N JFET	2N4341		
U1285	N JFET	2N4220		
U1288	N JFET	2N4341		
U1287	N JFET	2N4092		
U1321	N JFET	2N3966		
U1322	N JFET	2N4221A		
U1323	N JFET	2N4221A		
U1324	N JFET	2N4220A		
U1325	N JFET	2N4222		
U1420	N JFET	2N3821		

Industry Part Number	Type and Classification	Recommended Replacement	Data Sheet Page	Geometry Page
U1421	N JFET	2N3822	Refer to the 1982 Small Signal FET Design Catalog	
U1422	N JFET	2N3822		
U1714	N JFET	2N4340		
U1837E	N JFET	U1837		
U1897	N JFET	U1897		
U1897-18	N JFET	U1897-18		
U1897E	N JFET	U1897-18		
U1898	N JFET	U1898		
U1898-18	N JFET	U1898-18		
U1898E	N JFET	U1898-18		
U1899	N JFET	U1899		
U1899-18	N JFET	U1899-18		
U1899E	N JFT	U1899-18		
U1994E	N JFET	U1994		
U2047E	N JFET	PN4416		
U3000	N JFET	2N4341		
U3001	N JFET	2N4339		
U3002	N JFET	2N4338		
U3010	N JFET	2N4341		
U3011	N JFET	2N4340		
U3012	N JFET	2N4338		
UC20	N JFET	2N4341		
UC40	P JFET	2N2608		
UC41	P JFET	2N2608		
UC100	N JFET	2N4339		
UC110	N JFET	2N4339		
UC115	N JFET	2N4340		
UC120	N JFET	2N3686		
UC130	N JFET	2N4341		
UC155	N JFET	2N4416		
UC200	N JFET	2N3824		
UC201	N JFET	2N3824		
UC210	N JFET	2N4416		
UC220	N JFET	2N3822		
UC240	N JFET	2N4869		
UC241	N JFET	2N4869		
UC250	N JFET	2N4091		
UC251	N JFET	2N4392		
UC300	P JFET	2N2608		
UC310	P JFET	2N2843		
UC320	P JFET	2N2843		
UC330	P JFET	2N2843		
UC340	P JFET	2N2843		
UC400	P JFET	2N3331		
UC401	P JFET	2N5116		
UC410	P JFET	2N3330		
UC420	P JFET	2N3329		
UC450	P JFET	2N5114		
UC451	P JFET	2N5116		
UC588	N JFET	2N4417		
UC703	N JFET	2N4220		
UC704	N JFET	2N4220		
UC705	N JFET	2N4224		

SMALL SIGNAL FET Cross Reference (Cont'd)

Industry Part Number	Type and Classification	Recommended Replacement	Data Sheet Page	Geometry Page
UC707	N JFET	2N4860	Refer to the 1982 Small Signal FET Design Catalog	
UC714	N JFET	2N3822		
UC714E	N JFET	J203-18		
UC734	N JFET	2N4416		
UC734E	N JFET	PN4416		
UC751	N JFET	2N4340		
UC752	N JFET	2N4340		
UC753	N JFET	2N4341		
UC754	N JFET	2N4340		
UC755	N JFET	2N4341		
UC756	N JFET	2N4340		
UC805	P JFET	2N3331		
UC807	N JFET	2N4860		
UC814	P JFET	2N3331		
UC851	P JFET	2N2608		
UC853	P JFET	2N2608		
UC854	P JFET	2N2608		
UC855	P JFET	2N2609		
UC1700	P MOS ENH	3N163		
UC1764	P MOS ENH	3N163		
UC2130	D N JFET	2N5452	Refer to the 1982 Small Signal FET Design Catalog	
UC2132	D N JFET	2N3955		
UC2134	D N JFET	2N3956		
UC2136	D N JFET	2N3957		
UC2138	D N JFET	2N3958		
UC2139	D N JFET	2N3958		
UC2147	D N JFET	2N3958		
UC2148	D N JFET	2N3958		
UC2149	D N JFET	2N3958		
VCR2N	N JFET	VCR2N		
VCR3P	P JFET	VCR3P		
VCR4N	N JFET	VCR4N		
VCR5P	P JFET	VCR5P		
VCR6P	P JFET	2N5116		
VCR7N	N JFET	VCR7N		
VCR11N	N JFET	VCR11N		
WK5457	N JFET	2N5457		
WK5458	N JFET	2N5458		
WK5459	N JFET	2N5459		

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Analog Switches Selector Guide

Application	Feature of Application	Important Parameters	Major Tradeoffs	Suggested Switches
Battery Operated or Battery Back-Up Supply	1) Low Power	Low Supply Current		**CMOS DG304-DG308, DG304A, DG307A, DG309** DG300-DG303, DG381-DG390, DG300A-DG303A, DG381A-DG390A
	2) Minimum Number of Power Supplies	Only One or Two Supplies Needed		**CMOS DG300-DG308A, DG300A-DG307A, DG309** (Can Also Be Used As Single Supply) CMOS DG200, DG201, DG211, DG200A, DG201A, DG202, DG212 (For MUX: DG506-DG509, DG506A-DG509A, DG528, DG529)
	3) Low Standby Power	Low Standby Current		**CMOS DG304-DG308A, DG211, DG304A-DG307A, DG309, DG212**
Audio	1) Low Signal Distortion	Low $r_{DS(on)}$; Constant $r_{DS(on)}$	JFET is Constant, $r_{DS(on)}$; Signal Range Limited Toward Negative Supply; CMOS Slight $r_{DS(on)}$ Variation, Full Signal Range	**JFET DG180-DG191** CMOS DG300-DG308A, DG381-DG390, DG300A-DG307A, DG309, DG381A-DG390A, DG5040-DG5045 DG243 (Make-Before-Break)
	2) Low Noise (Channel)	Low $r_{DS(on)}$		CMOS DG300-DG308A, DG381-DG390, DG300A-DG307A, DG309, DG381A-DG390A, DG5040-DG5045, DG243 JFET DG180-DG191
	3) Wide Signal Range	±15V Signal Range		**CMOS DG300-DG308, DG381-DG390, DG300A-DG307A, DG309, DG381A-DG390A, DG5040-DG5045, DG243** CMOS DG200, DG200A, DG201, DG201A, DG202, DG211, DG212 (MUX: DG506-DG509, DG506A-DG509A, DG528, DG529)
		Signal Range is From the Positive Supply to Above the Negative Supply	Higher $r_{DS(on)}$ (Must Stay Above Negative Supply By 5V to 7.5V)	**JFET (75Ω) DG182, DG185, DG188, DG191** (10Ω, 30Ω) Remainder of DG181-DG190 Family
	4) Large Dynamic Range	Wide Signal Range and Low Thermocouple Noise		**CMOS DG304-DG308A, DG304A-DG307A, DG309** DG300-DG303, DG381-DG390, DG211, DG300A-DG303A, DG381A-DG390A, DG212
Video (High Frequency)	1) High OFF Impedance, Small Feedthrough of Signal	High OFF Isolation	Higher $r_{DS(on)}$	**JFET (30Ω, 75Ω) DG181, DG182, DG184, DG185, DG187, DG188, DG190, DG191** CMOS DG200, DG201, DG211, DG200A, DG201A, DG202, DG212 CMOS DG300-DG308A, DG381-DG390, DG300A-DG307A, DG309, DG381A-DG390A, DG5040-DG5045, DG243
	2) Good Impedance Matching, Minimum Signal Drop Across Switch	Low $r_{DS(on)}$	Lower OFF Isolation	**JFET (10Ω) DG180, DG183, DG186, DG189** (30Ω) DG181, DG184, DG187, DG190 CMOS DG300-DG308A, DG211 DG300A-DG307A, DG309, DG212

Bold Print = Recommended for the application

Analog Switches Selector Guide (Cont'd)

Application	Feature of Application	Important Parameters	Major Tradeoffs	Suggested Switches
Sample and Hold	1) Low Droop Rate	Low Leakage	Higher ON Resistance	**CMOS DG300A-DG307A, DG300, DG309 DG381A-DG390A** **CMOS DG300-DG308A, DG381-DG390, DG5040-DG5045** JFET DG180-DG191 CMOS DG200, DG201, DG211, DG200A, DG201A, DG202, DG212
	2) Low Sample to Hold Offset	Low Charge Coupling	Higher ON Resistance	**CMOS DG200A, DG201A, DG202, DG212** **CMOS DG200, DG201, DG211** JFET DG181, DG182 (30Ω, 75Ω) DG184, DG185, DG187, DG188, DG190, DG191 CMOS DG300-DG308A, DG300A-DG307A, DG309
	3) Fast Acquisition Speed	Low ON Resistance	Higher Leakage Higher Charge Coupling	**JFET (10Ω) DG180, DG183, DG186, DG189** (30Ω, 75Ω) Remainder of DG181-DG191 Family CMOS DG300-DG307, DG381-DG390, DG300A-DG307A CMOS DG200, DG201, DG211, DG212 CMOS DG381A-DG390A, DG200A, DG201A, DG202
Switching to High Impedance Inputs	1) Low Error Voltage	Low Leakage		**CMOS DG300A-DG307A, DG381A-DG390A** **CMOS DG300-DG307, DG381-DG390, DG5040-DG5045, DG200-DG201, DG211, DG200A, DG201A, DG212**
	2) Low Switching Transient Error Voltage	Low Charge Coupling		**CMOS DG200A, DG201A, DG202, DG212** **CMOS DG200, DG201, DG211** DG300-DG307, DG381-DG390, DG300A-DG307A, DG381A-DG390A
Low Cost	1) Best Performance for Lowest Cost	Monolithic Good Switch Performance		**CMOS DG211, DG212, DG303, DG309, DG308A, DG300-DG307, DG5040-DG5045** DG200, DG201, DG381-DG390, DG200A, DG201A, DG202, DG300A-DG307A, DG243, DG381A-DG390A
Military System	1) Hi-Rel Specified			**BS9000** **JM38510/XXXXX**
Differential Signal Switching	1) Good Matching of Switch Parameters	Monolithic Switch		**CMOS DG300, DG302, DG303, DG304, DG243, DG306, DG307, DG308A, DG381, DG384, DG390, DG309** CMOS DG200, DG201, DG211, DG5040-DG5045, DG300A, DG302A, DG303A, DG304A, DG306A, DG307A, DG309, DG381A, DG384A, DG390A, DG200A, DG207A, DG202, DG212
	2) Low Thermo-couple Offset Voltage	Drain and Source of FET Switch in Close Proximity on *Small Chip*	JFET Switches Not Monolithic	**JFET DG183, DG184, DG185.**
		Low Power Dissi-pation on Switch Driver		**CMOS DG304, DG306, DG307, DG308A DG304A, DG309** DG300-DG303, DG300A-DG303A, DG306A, DG307A, DG381-DG390, DG381A-DG390A, DG309

Bold Print = Recommended for the application

Analog Switches Selector Guide (Cont'd)

Application	Feature of Application	Important Parameters	Major Tradeoffs	Suggested Switches
Small Signal (<1 V)	1) Low Noise (Channel)	Low $r_{DS(on)}$	Higher Leakages	**JFET (10Ω) DG180, DG183, DG186, DG189** (30Ω, 75Ω) Remainder of DG181-DG191 Family
	2) Low Charge Coupling			**CMOS DG300A-DG307A, DG309, DG381A-DG390A, DG212, DG308A** CMOS DG300-DG308, DG381-DG390, DG211
	3) High Impedance Inputs of Load	Low Leakage	Higher $r_{DS(on)}$	**CMOS DG300-DG308A, DG381-DG390, DG211, DG5040-DG5045, DG243, DG309** DG200-DG201 JFET DG181, DG182, DG184, DG185, DG187, DG188, DG190, DG191 CMOS DG300A-DG307A, DG309, DG381A-DG390A, DG212
	4) Low Thermocouple Offset Voltage	Low Power Switch		**CMOS DG304-DG307, DG304A-DG307A, DG381A-DG390A** DG300-DG303, DG381-DG390, DG300A-DG303A
		Drain and Source of FET Switch in Close Proximity on *Small Chip*		**JFET DG180-DG190 Family**
Multiplexing	1) Break-Before-Make Switching	t_{on} is Greater Than t_{off}		**CMOS DG506, DG506A, DG507, DG507A, DG508, DG508A, DG509, DG509A, DG528, DG529 (Latchable)**
	2) Binary Controlled Logic Inputs	Binary Decoding Stage on Chip		PMOS DG501, DG503
	3) Differential Multiplexing	Dual Switching Action		CMOS DG507, DG509, DG507A, DG509A, DG529
	4) D/A Conversion	Binary Weighted ON Resistance and Channel Resistance to Minimize Error		NMOS DG515, DG516

Bold Print = Recommended for the application

Analog Switches

Basic Part No. (Note 1)	Switch Type	Analog Voltage Range (V) (Note 4)	$r_{DS(on)}$ Max (Ω) (Note 4)	$I_{D(off)}$ (nA)	Switching Time (μsec) t_{ON}	Switching Time (μsec) t_{OFF}	Logic Levels (V) V_{INL}	Logic Levels (V) V_{INH}	Opt. Supply Voltage (V) (+) Sup. V+	Opt. Supply Voltage (V) (−) Sup. V−	Logic Sup. V_L	Ref. Sup. V_R	Comments	Switch Configuration
						SINGLE CHANNEL SPST								
DG5040	Plus 40 CMOS	+15 to −15	50	1	1.0	0.5	0.8	2	15	−15	5	—	TTL Compatible	1 SPST Switch per Package
						TWO CHANNEL SPST								
DG180	N-JFET	+10 to −12.5	10	10	0.3	0.25	0.8	2.0	10	−20	5	0	Break-Before-Make	
		+10 to −7.5	10	10	0.3	0.26	0.8	2.0	15	−15	5	0	15 V Supplies	
DG181	N-JFET	+10 to −12.5	30	1	0.15	0.13	0.8	2.0	10	−20	5	0	Break-Before-Make	
		+10 to −7.5	30	1	0.15	0.13	0.8	2.0	15	−15	5	0	15 V Supplies JAN/11101	
DG182	N-JFET	+10 to −15	75	1	0.25	0.13	0.8	2.0	10	−20	5	0	Break-Before-Make	
		+10 to −10	75	1	0.25	0.13	0.8	2.0	15	−15	5	0	15 V Supplies JAN/11102	2 SPST Switches per Package
DG200	CMOS	+15 to −15	70	2	1.0	0.5	0.8	2.4	15	−15	—	(Note 3)	JAN/12303	
DG200A	Plus 40 CMOS	+15 to −15	70	2	1.0	0.5	0.8	2.4	15	−15	—	—	TTL In	
DG281	N-JFET	+15 to −15	300	0.2	0.15	0.13	0.8	2.0	15	−15	5	0	Low Charge Injection	
DG300	CMOS	+15 to −15	50	1	0.3	0.25	0.8	4.0	15	−15	—	—	Low Power, TTL In JAN/11601	
DG300A	Plus 40 CMOS	+15 to −15	50	1	0.3	0.25	0.8	4.0	15	−15	—	—	Low Power, TTL In	
DG304	CMOS	+15 to −15	50	1	0.25	0.15	3.5	11.0	15	−15	—	—	Low Power, CMOS In JAN/11605	
DG304A	Plus 40 CMOS	+15 to −15	50	1	0.25	0.15	3.5	11.0	15	−15	—	—	Low Power, CMOS In	
DG381	CMOS	+15 to −15	50	1	0.3	0.25	0.8	4.0	15	−15	—	—	Low Power, DG181 Pin Out	
DG381A	Plus 40 CMOS	+15 to −15	50	1	0.3	0.25	0.8	4.0	15	−15	—	—	Low Power, DG181 Pin Out	
DG5041	Plus 40 CMOS	+15 to −15	50	1	1.0	0.5	0.8	2.0	15	−15	5	—	TTL Compatible	
						FOUR CHANNEL SPST								
DG201	CMOS	+15 to −15	175	1	1.0	0.5	0.8	2.4	15	−15	—	(Note 3)	JAN/12304	4 SPST Switches per Package
DG201A	Plus 40 CMOS	+15 to −15	175	1	1.0	0.5	0.8	2.4	15	−15	—	—	TTL In	
DG202	Plus 40 CMOS	+15 to −15	175	1	1.0	0.5	0.8	2.4	15	−15	—	—	TTL In	
DG211	Plus 40 CMOS	+15 to −15	175	5	0.5	0.4	0.8	2.4	15	−15	5	—	Low Cost, TTL In	
DG212	Plus 40 CMOS	+15 to −15	175	5	0.6	0.45	0.8	2.4	15	−15	5	—	Low Cost, TTL In	
DG308A	Plus 40 CMOS	+15 to −15	100	1	0.2	0.15	3.5	11.0	15	−15	—	—	Low Cost CMOS In	
DG309	Plus 40 CMOS	+15 to −15	100	5	0.2	0.15	3.5	11.0	15	−15	—	—	Low Cost CMOS In	
						ONE CHANNEL SPDT								
DG186	N-JFET	+10 to −12.5	10	10	0.3	0.25	0.8	2.0	10	−20	5	0	Break-Before-Make	
	N-JFET	+15 to −7.5	10	10	0.3	0.25	0.8	2.0	15	−15	5	0	15 V Supplies	
DG187	N-JFET	+10 to −12.5	30	1	0.15	0.13	0.8	2.0	10	−20	5	0	Break-Before-Make	
	N-JFET	+15 to −7.5	30	1	0.15	0.13	0.8	2.0	15	−15	5	0	15 V Supplies JAN/11105	
DG188	N-JFET	+10 to −15	75	1	0.25	0.13	0.8	2.0	10	−20	5	0	Break-Before-Make	1 SPST Switch per Package
	N-JFET	+15 to −10	75	1	0.25	0.13	0.8	2.0	15	−15	5	0	15 V Supplies JAN/11106	
DG287	N-JFET	+15 to −7.5	300	0.2	0.15	0.13	0.8	2.0	15	−15	5	0	Break-Before-Make	
DG301	CMOS	+15 to −15	50	1	0.3	0.25	0.8	4.0	15	−15	—	—	Low Power, TTL In JAN/11602	
DG301A	Plus 40 CMOS	+15 to −15	50	1	0.3	0.25	0.8	4.0	15	−15	—	—	Low Power, TTL In	
DG305	CMOS	+15 to −15	50	1	0.25	0.15	3.5	11.0	15	−15	—	—	Low Power, CMOS In JAN/11605	
DG305A	Plus 40 CMOS	+15 to −15	50	1	0.25	0.15	3.5	11.0	15	−15	—	—	Low Power, CMOS In	
DG387	CMOS	+15 to −15	50	1	0.3	0.25	0.8	4.0	15	−15	—	—	Low Power, DG187 Pin Out	
DG387A	Plus 40 CMOS	+15 to −15	50	1	0.3	0.25	0.8	4.0	15	−15	—	—	Low Power, DG187 Pin Out	
DG5042	Plus 40 CMOS	+15 to −15	50	1	1.0	0.5	0.8	4.0	15	−15	5	—	TTL Compatible	

NOTES:

1. The devices shown in **boldface** are recommended parts for new designs.
2. The appropriate switching characteristic for multiplexers is $t_{TRANSITION}$, not t_{ON}, t_{OFF}.
3. V_{REF} = 1.5 V is used when supply voltages < ± 15 V are used. Not needed when supply voltages of ± 15 are used.
4. Analog voltage range is a function of supply voltages. Where a FET switch is PMOS or CMOS, r_{DS} is also a function of Supply Voltage and Analog Voltage. See individual data sheets for more detail. Values shown are for temperature suffix A.
5. Device normally operates with resistor to + 10 V.

Analog Switches (Cont'd)

Basic Part No. (Note 1)	Switch Type	Analog Voltage Range (V) (Note 4)	$r_{DS(on)}$ Max (Ω) (Note 4)	$I_{D(off)}$ (nA)	Switching Time (μsec) t_{ON}	t_{OFF}	Logic Levels (V) V_{INL}	V_{INH}	Opt. Supply Voltage (V) (+) Sup. V+	(−) Sup. V−	Logic Sup. V_L	Ref. Sup. V_R	Comments	Switch Configuration
TWO CHANNEL SPDT														
DG189	N-JFET	+10 to −12.5	10	10	0.3	0.25	0.8	2.0	10	−20	5	0	Break-Before-Make	2 SPDT Switches per Package
	N-JFET	+15 to −7.5	10	10	0.3	0.25	0.8	2.0	15	−15	5	0	15 V Supplies	
DG190	N-JFET	+10 to −12.5	30	1	0.15	0.13	0.8	2.0	10	−20	5	0	Break-Before-Make JAN/11107	
	N-JFET	+15 to −7.5	30	1	0.15	0.13	0.8	2.0	15	−15	5	0	15 V Supplies	
DG191	N-JFET	+10 to −15	75	1	0.25	0.13	0.8	2.0	10	−20	5	0	Break-Before-Make JAN/11108	
	N-JFET	+15 to −10	75	1	0.25	0.13	0.8	2.0	15	−15	5	0	15 V Supplies	
DG243	Plus 40 CMOS	+15 to −15	50	1	0.5	1.0	0.8	2.0	15	−15	5	—	Make-Before-Break (DG191 Pin Out)	
DG290	N-JFET	+15 to −7.5	300	0.2	0.15	0.13	0.8	2.0	15	−15	5	0	Break-Before-Make	
DG303	CMOS	+15 to −15	50	1	0.3	0.25	0.8	4.0	15	−15	—	—	Low Power, TTL In JAN/11604	
DG303A	Plus 40 CMOS	+15 to −15	50	1	0.3	0.25	0.8	4.0	15	−15	—	—	Low Power, TTL In	
DG307	CMOS	+15 to −15	50	1	0.25	0.15	3.5	11.0	15	−15	—	—	Low Power, CMOS In JAN/11608	
DG307A	Plus 40 CMOS	+15 to −15	50	1	0.25	0.15	3.5	11.0	15	−15	—	—	Low Power, CMOS In	
DG390	CMOS	+15 to −15	50	1	0.3	0.25	0.8	4.0	15	−15	—	—	Low Power, DG190 Pin Out	
DG390A	Plus 40 CMOS	+15 to −15	50	1	0.3	0.25	0.8	4.0	15	−15	—	—	Low Power, DG190 Pin Out	
DG5043	Plus 40 CMOS	+15 to −15	50	1	1.0	0.5	0.8	2.0	15	−15	5	—		
ONE CHANNEL DPST														
DG5044	Plus 40 CMOS	+15 to −15	50	1	1.0	0.5	0.8	2	15	−15	5	—	TTL Compatible	1 DPST Switch per Package
TWO CHANNEL DPST														
DG183	N-JFET	+10 to −12.5	10	10	0.3	0.25	0.8	2.0	10	−20	5	0	Break-Before-Make	2 DPST Switches per Package
	N-JFET	+15 to −7.5	10	10	0.3	0.25	0.8	2.0	15	−15	5	0	15 V Supplies	
DG184	N-JFET	+10 to −12.5	30	1	0.15	0.13	0.8	2.0	10	−20	5	0	Break-Before-Make	
	N-JFET	+15 to −7.5	30	1	0.15	0.13	0.8	2.0	15	−15	5	0	15 V Supplies	
DG185	N-JFET	+10 to −15	75	1	0.25	0.13	0.8	2.0	10	−20	5	0	Break-Before-Make	
	N-JFET	+15 to −10	75	1	0.25	0.13	0.8	2.0	15	−15	5	0	15 V Supplies	
DG284	N-JFET	+15 to −7.5	300	0.2	0.15	0.13	0.8	2.0	15	−15	5	0	Break-Before-Make	
DG302	CMOS	+15 to −15	50	1	0.3	0.25	0.8	4.0	15	−15	—	—	Low Power, TTL In	
DG302A	Plus 40 CMOS	+15 to −15	50	1	0.3	0.25	0.8	4.0	15	−15	—	—	Low Power, TTL In	
DG306	CMOS	+15 to −15	50	1	0.25	0.15	3.5	11.0	15	−15	—	—	Low Power, CMOS In	
DG306A	Plus 40 CMOS	+15 to −15	50	1	0.25	0.15	3.5	11.0	15	−15	—	—	Low Power, CMOS In	
DG384	CMOS	+15 to −15	50	1	0.3	0.25	0.8	4.0	15	−15	—	—	Low Power, DG184 Pin Out	
DG384A	Plus 40 CMOS	+15 to −15	50	1	0.3	0.25	0.8	4.0	15	−15	—	—	Low Power, DG184 Pin Out	
DG5045	Plus 40 CMOS	+15 to −15	50	1	1.0	0.5	0.8	2.0	15	−15	5	—		

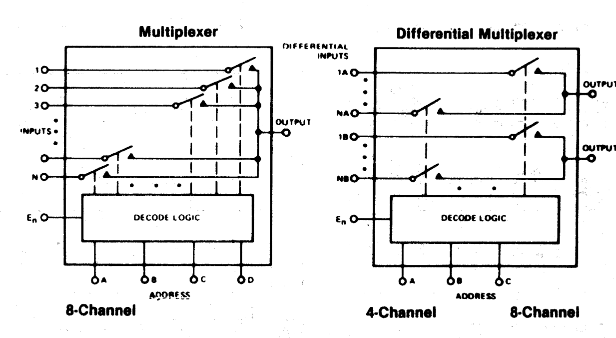
NOTES:

1. The devices shown in **boldface** are recommended parts for new designs.
2. The appropriate switching characteristic for multiplexers is $t_{TRANSITION}$, not t_{ON}, t_{OFF}.
3. V_{REF} = 1.5 V is used when supply voltages < ± 15 V are used. Not needed when supply voltages of ± 15 are used.
4. Analog voltage range is a function of supply voltages. Where a FET switch is PMOS or CMOS, r_{DS} is also a function of Supply Voltage and Analog Voltage. See individual data sheets for more detail. Values shown are for temperature suffix A.
5. Device normally operates with resistor to + 10 V.

Multiplexers with Input Latches

Basic Part No.	Process Type	Analog Voltage Range (V) (Note 4)	$r_{DS(on)}$ Max (Ω) (Note 4)	$I_{D(off)}$ (nA)	Transition Time (μsec) (Note 2)	Logic Levels (V) V_{INL}	Logic Levels (V) V_{INH}	Supply Voltage (V) (+) Sup. V+	Supply Voltage (V) (−) Sup. V−	Comments
EIGHT CHANNEL MUX + ENABLE										
DG501	PMOS	+5 to −5	150-240	8	1.5	0.6	3.5	5	−20	Logic Pullup Resistors
DG503	PMOS	+10 to −10	150-800	8	1.5	0.6	8.5	10	−20	
DG508A	Plus 40 CMOS	+10 to −15	400	10	1.0	0.8	2.4	15	−15	Break-Before-Make
DG528	Plus 40 CMOS	+15 to −15	400	10	1.0	0.8	2.4	+15	−15	Latches On Inputs
SIXTEEN CHANNEL MUX + ENABLE										
DG506A	Plus 40 CMOS	+15 to −15	400	10	1.0	0.8	2.4	15	−15	Break-Before-Make
FOUR CHANNEL DIFFERENTIAL MUX + ENABLE										
DG509A	Plus 40 CMOS	+15 to −15	400	10	1.0	0.8	2.4	15	−15	Break-Before-Make
DG529	Plus 40 CMOS	+15 to −15	400	10	1.0	0.8	2.4	15	−15	Latches On Inputs
EIGHT CHANNEL DIFFERENTIAL MUX + ENABLE										
DG507A	Plus 40 CMOS	+15 to −15	400	5	1.0	0.8	2.4	+15	−15	Break-Before-Make

Switch Configurations



NOTES:
1. The devices shown in **boldface** are recommended parts for new designs.
2. The appropriate switching characteristic for multiplexers is $t_{TRANSITION}$, not t_{ON}, t_{OFF}.
3. V_{REF} = 1.5 V is used when supply voltages < ± 15 V are used. Not needed when supply voltages of ± 15 are used.
4. Analog voltage range is a function of supply voltages. Where a FET switch is PMOS or CMOS, r_{DS} is also a function of Supply Voltage and Analog Voltage. See individual data sheets for more detail. Values shown are for temperature suffix A.
5. Device normally operates with resistor to + 10 V.

Analog Switches Product Information

Drivers and Gates

Basic Part No. (Notes 1 & 2)	Switch Type	$r_{DS(on)}$ Max. (Ω) (Note 3)	Analog Voltage Range (p-p V) (Note 3)	Switching Time (μs) t_{ON}	t_{OFF}	Logic Input for ON Switch	Logic Levels (V) V_{INL}	V_{INH}	Opt. Sup. Voltage (V) (+) Sup. V_1	(−) Sup. V_2	Logic Sup. V_L	Comments
One Channel SPST												
DG5040	CMOS Plus-40	50	30	1.0	0.5	1	0.8	2.0	15	-15	5	
Two Channel SPST												
DGM111	PMOS	75-200	20	0.3	1.0	0	0.5	4.6	10	-20	5	
DG133	N-JFET	30	20	0.6	1.6	1	0.8	2.5	12	-18	—	See DG181
DG134	N-JFET	80	20	0.6	1.6	1	0.8	2.5	12	-18	—	See DG182
DG141	N-JFET	10	20	1.0	2.5	1	0.8	2.5	12	-18	—	See DG180
DG151	N-JFET	15	15	1.0	2.5	1	0.8	2.5	15	-15	—	See DG180
DG152	N-JFET	50	15	0.8	1.6	1	0.8	2.5	15	-15	—	See DG181
SG180	N-JFET	10	20	0.3	0.25	0	0.8	2.0	10	-20	5	Break-Before-Make
		10	15	0.3	0.25	0	0.8	2.0	15	-15	5	15V Supplies
***DG181**	N-JFET	30	20	0.15	0.13	0	0.8	2.0	10	-20	5	Break-Before-Make
		30	15	0.15	0.13	0	0.8	2.0	15	-15	5	15V Supplies
***DG182**	N-JFET	75	20	0.25	0.13	0	0.8	2.0	10	-20	5	Break-Before-Make
		75	20	0.25	0.13	0	0.8	2.0	15	-15	5	15V Supplies
DG200	CMOS	70	30	1.0	0.5	0	0.8	2.4	15	-15	—	
***DG200A**	CMOS Plus-40	70	30	1.0	0.5	0	0.8	2.4	15	-15	—	
DG281	N-JFET	300	20	0.15	0.13	0	0.8	2.0	15	-15	5	Break-Before-Make
***DG300**	CMOS	50	30	0.300	0.250	1	0.8	4.0	15	-15	—	
***DG381**	CMOS	50	30	0.300	0.250	0	0.8	4.0	15	-15	—	
***DG304**	CMOS	50	30	0.250	0.150	1	3.5	11.0	15	-15	—	CMOS compatible
***DG5041**	CMOS Plus-40	50	30	1.0	0.5	1	0.8	2.0	15	-15	5	Break-Before-Make
Four Channel SPST												
***DG172**	PMOS	150-450	20	0.3	0.75	0	0.8	2.0	10	-20	5	
DG201	CMOS	175	30	1.0	0.5	0	0.8	2.4	15	-15	—	
***DG201A**	CMOS Plus-40	175	30	0.6	0.45	0	0.8	2.4	15	-15	—	
***DG202**	CMOS Plus-40	175	30	0.6	0.45	1	0.8	2.4	15	-15	—	
***DG211**	CMOS Plus-40	175	30	1.0	0.5	0	0.8	2.4	15	-15	5	
***DG212**	CMOS Plus-40	175	30	1.0	0.5	1	0.8	2.4	15	-15	5	
***DG308A**	CMOS Plus-40	100	30	0.2	0.15	1	3.5	11.0	15	-15	—	Single Supply Operation
***DG309**	CMOS Plus-40	100	30	0.2	0.15	0	3.5	11.0	15	-15	—	Single Supply Operation
Five Channel SPST												
DG125	PMOS	100-450	20	0.3	2.0	0	0.5	4.6	10	-20	5	
One Channel SPDT												
DG143	N-JFET	80	20	0.8	1.6	(Note 4)	2.0	3.0	12	-18	—	See DG188
DG144	N-JFET	30	20	0.8	1.6	(Note 4)	2.0	3.0	12	-18	—	See DG187
DG146	N-JFET	10	20	1.0	2.5	(Note 4)	2.0	3.0	12	-18	—	See DG186
DG161	N-JFET	15	15	1.0	2.5	(Note 4)	2.0	3.0	15	-15	—	See DG186
DG162	N-JFET	50	15	0.8	1.6	(Note 4)	2.0	3.0	15	-15	—	See DG187
DG186	N-JFET	10	20	0.3	0.25	(Note 5)	0.8	2.0	10	-20	5	Break-Before-Make
	N-JEFT	10	15	0.3	0.25	(Note 5)	0.8	2.0	15	-15	5	15V Supplies
***DG187**	N-JFET	30	20	0.15	0.13	(Note 5)	0.8	2.0	10	-20	5	Break-Before-Make
	N-JFET	30	15	0.15	0.13	(Note 5)	0.8	2.0	15	-15	5	15V Supplies
***DG188**	N-JFET	75	20	0.25	0.13	(Note 5)	0.8	2.0	10	-20	5	Break-Before-Make
	N-JFET	75	20	0.25	0.13	(Note 5)	0.8	2.0	15	-15	5	15V Supplies
DG287	N-JFET	300	20	0.15	0.13	(Note 5)	0.8	2.0	15	-15	5	Break-Before-Make

*Devices recommended for new designs are indicated in **bold face** type.

Analog Switches Product Information (Cont'd)

Drivers and Gates (Cont'd)

Basic Part No. (Notes 1 & 2)	Switch Type	$r_{DS(on)}$ Max. (Ω) (Note 3)	Analog Voltage Range (p-p V) (Note 3)	Switching Time (μs) t_{ON}	t_{OFF}	Logic Input for ON Switch	Logic Levels (V) V_{INL}	V_{INH}	Opt. Sup. Voltage (V) (+) Sup. V_1	(−) Sup. V_2	Logic Sup. V_l	Comments
One Channel SPDT (Cont'd)												
***DG301**	CMOS	50	30	0.300	0.250	(Note 5)	0.8	4.0	15	−15	—	
***DG387**	CMOS	50	30	0.300	0.250	(Note 5)	0.8	4.0	15	−15	—	
***DG305**	CMOS	50	30	0.250	0.150	(Note 5)	3.5	11.0	15	−15	—	CMOS compatible
SI3002	PMOS	100-400	20	1.0	1.5	(Note 5)	0.8	2.0	10	−20	—	Same as HAD30021XX
***DG5042**	CMOS Plus-40	50	30	1.0	0.5	(Note 5)	0.8	2.0	15	−15	5	Break-Before-Make
Two Channel SPDT												
DG189	N-JFET	10	20	0.3	0.25	(Note 5)	0.8	2.0	10	−20	5	Break-Before-Make
	N-JFET	10	15	0.3	0.25	(Note 5)	0.8	2.0	15	−15	5	15V Supplies
***DG190**	N-JFET	30	20	0.15	0.13	(Note 5)	0.8	2.0	10	−20	5	Break-Before-Make
	N-JFET	30	15	0.15	0.13	(Note 5)	0.8	2.0	15	−15	5	15V Supplies
***DG191**	N-JFET	75	20	0.25	0.13	(Note 5)	0.8	2.0	10	−20	5	Break-Before-Make
	N-JFET	75	20	0.25	0.13	(Note 5)	0.8	2.0	15	−15	5	15V Supplies
***DG243**	CMOS Plus-40	50	30	1.0	0.5	(Note 5)	0.8	2.0	15	−15	5	Make-Before-Break
DG290	N-JFET	300	20	0.15	0.13	(Note 5)	0.8	2.0	15	−15	5	Break-Before-Make
***DG303**	CMOS	50	30	0.300	0.250	(Note 5)	0.8	4.0	15	−15	—	
***DG390**	CMOS	50	30	0.300	0.250	(Note 5)	0.8	4.0	15	−15	—	
***DG307**	CMOS	50	30	0.250	0.150	(Note 5)	3.5	11.0	15	−15	—	CMOS compatible
***DG5043**	CMOS Plus-40	50	30	1.0	0.5	(Note 5)	0.8	2.0	15	−15	5	Break-Before-Make
One Channel DPST												
***DG5044**	CMOS Plus-40	50	30	1.0	0.5	(Note 5)	0.8	2.0	15	−15	5	Break-Before-Make
Two Channel DPST												
DG126	N-JFET	80	20	0.6	1.6	1	0.8	2.5	12	−18	—	See DG185
DG129	N-JFET	30	20	0.6	1.6	1	0.8	2.5	12	−18	—	See DG184
DG140	N-JFET	10	20	1.0	2.5	1	0.8	2.5	12	−18	—	See DG183
DG153	N-JFET	15	15	1.0	2.5	1	0.8	2.5	15	−15	—	See DG183
DG154	N-JFET	50	15	0.6	1.6	1	0.8	2.5	15	−15	—	See DG185
DG183	N-JFET	10	20	0.3	0.25	1	0.8	2.0	10	−20	5	Break-Before-Make
	N-JFET	10	15	0.3	0.25	1	0.8	2.0	15	−15	5	15V Supplies
***DG184**	N-JFET	30	20	0.15	0.13	1	0.8	2.0	10	−20	5	Break-Before-Make
	N-JFET	30	15	0.15	0.13	1	0.8	2.0	15	−15	5	15V Supplies
***DG185**	N-JFET	75	20	0.25	0.13	1	0.8	2.0	10	−20	5	Break-Before-Make
	N-JFET	75	20	0.25	0.13	1	0.8	2.0	15	−15	5	15V Supplies
DG284	N-JFET	300	20	0.15	0.13	1	0.8	2.0	15	−15	5	Break-Before-Make
***DG302**	CMOS	50	30	0.300	0.250	1	0.8	4.0	15	−15	—	
***DG384**	CMOS	50	30	0.300	0.250	1	0.8	4.0	15	−15	—	
***DG306**	CMOS	50	30	0.250	0.150	1	3.5	11.0	15	−15	—	CMOS compatible
***DG5045**	CMOS Plus-40	50	30	1.0	0.5	1	0.8	2.0	15	−15	5	Break-Before-Make
One Channel DPDT												
DG139	N-JFET	30	20	0.8	1.6	(Note 4)	2.0	3.0	12	−18	—	See DG191
DG142	N-JFET	80	20	0.8	1.6	(Note 4)	2.0	3.0	12	−18	—	See DG190
DG145	N-JFET	10	20	1.0	2.5	(Note 4)	2.0	3.0	12	−18	—	See DG189
DG163	N-JFET	15	15	1.0	2.5	(Note 4)	2.0	3.0	15	−15	—	See DG189
DG164	N-JFET	50	15	0.8	1.6	(Note 4)	2.0	3.0	15	−15	—	See DG191
Eight Channel MUX + Enable												
DG501	PMOS	150-250	10	1.5	(Note 8)	(Note 7)	0.6	3.5	5	−20	—	Logic Pullup Resistors
DG503	PMOS	150-800	20	1.5	(Note 8)	(Note 7)	0.6	8.5	10	−20	—	
DG508	CMOS	400	30	1.0	(Note 8)	(Note 7)	0.8	2.4	15	−15	—	

*Devices recommended for new designs are indicated in **bold face** type.

Analog Switches Product Information (Cont'd)

Drivers and Gates (Cont'd)

Basic Part No. (Notes 1 & 2)	Switch Type	$r_{DS(on)}$ Max. (Ω) (Note 3)	Analog Voltage Range (p-pV) (Note 3)	Switching Time (μs) t_{ON}	t_{OFF}	Logic Input for ON Switch	Logic Levels (V) V_{INL}	V_{INH}	Opt. Sup. Voltage (V) (+) Sup. V_1	(−) Sup. V_2	Logic Sup. V_I	Comments
Eight Channel MUX + Enable (Cont'd)												
*DG508A	CMOS Plus-40	400	30	1.0	(Note 8)	(Note 7)	0.8	2.4	15	-15	—	
*DG528	CMOS Plus-40	400	30	1.0	(Note 8)	(Note 7)	0.8	2.4	15	-15	—	With Input Latches
SI3705	PMOS	150-400	10	1.5	(Note 8)	(Note 7)	0.6	3.5	5	-20	—	See DG501/No Pullup Resistors
Sixteen Channel MUX + Enable												
DG506	CMOS	400	30	1.0	(Note 8)	(Note 7)	0.8	2.4	15	-15	—	Break-Before-Make
*DG506A	CMOS Plus-40	400	30	1.0	(Note 8)	(Note 7)	0.8	2.4	15	-15	—	
Four Channel Differential MUX												
DG509	CMOS	400	30	1.0	(Note 8)	(Note 7)	0.8	2.4	15	-15	—	Break-Before-Make
*DG509A	CMOS Plus-40	400	30	1.0	(Note 8)	(Note 7)	0.8	2.4	15	-15	—	
*DG529	CMOS Plus-40	400	30	1.0	(Note 8)	(Note 7)	0.8	2.4	15	-15	—	With Input Latches
Eight Channel Differential MUX + Enable												
DG507	CMOS	400	30	1.0	(Note 8)	(Note 7)	0.8	2.4	15	-15	—	Break-Before-Make
*DG507A	CMOS Plus-40	400	30	1.0	(Note 8)	(Note 7)	0.8	2.4	15	-15	—	
Four Channel SPDT D/A Converter Summing Node Switches												
DG515	NMOS	See Comments	—	0.120	0.170	(Note 5)	0.5	7.5	8.0	0	—	$R_1 = 6.25Ω$, $R_2 = 12.5Ω$, $R_3 = 25Ω$, $R_4 = 50Ω$
Ten Channel SPDT D/A Converter Summing Node Switches												
DG516	NMOS	See Comments	—	0.120	0.170	(Note 5)	0.5	7.5	8.0	0	—	$R_1 = 100Ω$, $R_2 = 200Ω$ $R_3 = 400Ω$, $R_4 = 800Ω$ $R_5 = 1600Ω$ $R_{6-10} = 3200Ω$

Multiple FET Switches

Siliconix P-Channel MOSFET & DMOS Switches are available for such applications as sequential switching (commutation), signal processing, modulation, and A-to-D conversion. The MOSFET is normally OFF. These devices are also available with Siliconix drivers in a single package.

Basic Part Number (Note 2)	Circuit Function: Sources	Drains	Gates	Switch Type	Pull Up On Gate	r_{DS} Max. (V) @ $V_S = +10V$	@ $V_S = -10V$	BV_{DSS}	$I_{S(off)}$ (nA)	$V_{GS(th)}$ Min.	Max.	C_{gs} Typ. (pF)	C_{ds} Typ. (pF)	C_{sb} Typ. (pF)
G115	6	1	6	SP6T	Yes	100	450	-30	0.5	-1.5	-4.0	0.9	0.4	2
G118	6	1	8	SP6T	No	100	450	-30	0.5	-1.5	-4.0	0.9	0.4	2
G119	6	2	3	DP3T	Yes	100	450	-30	0.5	-1.5	-4.0	1.8	0.4	2
G122	4	2	2	DPDT	Yes	100	450	-30	0.5	-1.5	-4.0	1.8	0.4	2
G123	4	2	4	2×SPDT	Yes	100	450	-30	0.5	-1.5	-4.0	1.8	0.4	2
*SD5000	4	4	4	4×SPST	No	50		20	10.0	0.1	2.0	3.5	0.5	4
*SD5001	4	4	4	4×SPST	No	50		10	10.0	0.1	2.0	3.5	0.5	4
*SD5002	4	4	4	4×SPST	No	50		15	10.0	0.1	2.0	3.5	0.5	4
*SD5200	4	4	4	4×SPST	No	80		30	1000	0.5	2.0	3.5	0.5	4

*Devices recommended for new designs are indicated in **bold face** type.

Drivers for MOS FET Switches

These drivers were designed to function as a level shifter and buffer between low level logic and the control gate of FET analog switches. Output voltage ratings are as high as 50V.

Basic Part Number (Note 2)	INPUTS	OUTPUTS	Function and Uses	ON Level $V_{(OUT)}ON-V_2$ at Rated Current(s)	OFF Level $V_{(OUT)}OFF$ at Rated Current or $I_{(OUT)}(OFF)$ at Rated Voltage	Input Logic for V_{OUT} (low)	V_{INL} (V)	V_{INH} (V) (I_{INH}) (mA)	Optimum Supply Voltage (V) V_1	V_2	V_L	V_R	Switching Time (μs) t_{ON}	t_{OFF}
D125	6	6	Six Separate MOSFET-Drivers	0.4V@5mA	0.1μA@10V	0	0.5	4.6	(Note 9)	-20	5	—	0.5	1.2
D129	7	4	Four Channel (BV = 50) MOSFET-Driver with Decode	0.7V@10mA	0.1μA@10V	1	0.7	2.2	(Note 9)	-20	—	—	0.25	0.8
													t_d+	t_d-
***D169**	2	4	Dual High-Speed Drivers with Complementary Outputs designed to drive high-capacity loads.	1.2V@1mA 3.0V@40mA	1.1V@1mA 2.5V@40mA	Output & Complement Available	0.8 0.8	2.0 2.0	15 15	-15 -15	5 5	0 0	0.17 0.17	0.20 0.20

NOTES:

(1) *Devices recommended for new designs are indicated in **bold face** type.
(2) See pages 7-26 through 7-28 for package and temperature designations for most products.
(3) Analog voltage range is a function of supply voltages. Where a FET switch is PMOS or CMOS, r_{DS} is also a function of Supply Voltage and Analog Voltage. See individual data sheets for more detail.
(4) Input reference voltage of 2.5V is required (see data sheets).
(5) See data sheet for switch state of differential switches.
(6) Current Driven Device—I_{INH} = 1mA.
(7) For truth table see data sheet.
(8) The appropriate switching characteristic for multiplexers is $t_{TRANSITION}$, not t_{ON}, t_{OFF}.
(9) Device normally operates with resistor—to +10V.
(10) (C_L = 35pF).

LSI/Linear Product Information

A/D Converters

3½-Digit High Performance	**LD110/LD111A** 16-pin plastic DIPs	±3½-Digit A/D Converter Accuracy 0.02% ±1 count Auto zero Auto polarity 10μV resolution Typical T.C. of 5 ppm/°C A usable 20mV scale	Three voltage ranges: 1.999V, 199.9mV & 19.99mV Sampling rate up to 40 samples/s Differential input capability Over-range & under-range signals TTL compatible
4½-Digit	**LD120/121A** 16- & 18- pin plastic DIP respectively	±4½-Digit A/D Converter Accuracy 0.005% ±1 count Auto zero Auto polarity TTL compatible Internal clock Linear to 28,500 counts	Two voltage ranges: 2.0V & 200.00mV 1 to 5 samples/s 25% inter-digit blanking MUX BCD outputs 0.5 count stability on 2.0V range Monolithic design
4½-Digit	**LD122/LD121A** 16- & 18- pin plastic DIP respectively	±4½-Digit A/D Converter Accuracy 0.005% ±1 count 1μV resolution for 20 mV FS Auto zero Auto polarity TTL compatibility Internal clock Linear to 28,500 counts	MUX BCD outputs Two over-range outputs, under-range, blink inhibit and convert-on-command capability Interfaces to external circuitry and microprocessors

Micropower Linears

Triple Op Amp	**L144** 14-pin plastic, ceramic, flat-pack & Dice	±1.5 to ±18V supply Programmable supply current Internally compensated 0.4V/μs slew rate	80dB gain with 20kΩ load Drives large capacitive loads ±30V differential input Monolithic construction
Quad Comparator	**L161** 16-pin plastic, ceramic, flat-pack & Dice	±1.5 to ±18V supply Single supply operation Programmable supply current 3V/μs slew rate	Gain greater than 20V/mV Sensing near ground ±30V differential input CMOS Logic compatible

Telecommunications Products

Loop Disconnect Dialer (pulse dialer)	**DF320** 18-lead ceramic, plastic & CERDIP		Operation from 2.5V to 5V supply Low standby power dissipation; 3μW Low dynamic power consump-ion; 600μW On-chip oscillator for 3.579545 MHz crystal Redial capability Hold capability delays impulsing Post-impulsing pause of 33 ms Mask during impulsing and inter-digit pause Selectable make-break ratio 10, 16, 20, 932 Hz impulsing rates Inter-digital pause of 800 ms

LSI/Linear Product Information (Cont'd)

Loop Disconnect Dialer (pulse dialer) (Cont'd)	**DF320A**		Same as DF320, except post-impulsing pause of 500ms
	DF322		Same as DF320, except mask during impulsing only
	DF328 16-lead plastic		Same as DF320, except 10, 932Hz impulsing rates No hold capability during impulsing

Interface

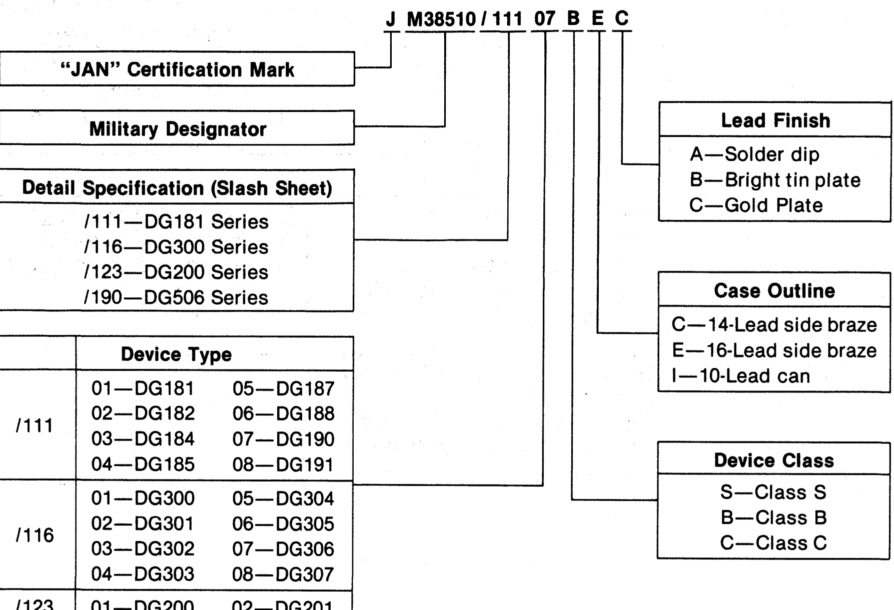
Four-digit MUX'd BCD to LCD Display Driver	**DF412** 40-pin plastic	Decodes MUX BCD to LCD 4-Digit drive capability Low power consumption TTL, DTL, CMOS compatible Can be ganged to drive more than 4 digits	7-segment LCD drive signals Drives large LCDs easily Can be clocked using an external oscillator Internal oscillator available
Dual High-Voltage Driver	**D169** 14-pin DIP	Designed to drive MOSPOWER Accepts TTL input High output drive; up to 36V Complementary outputs on each channel	

Analog Switches

JAN 38510

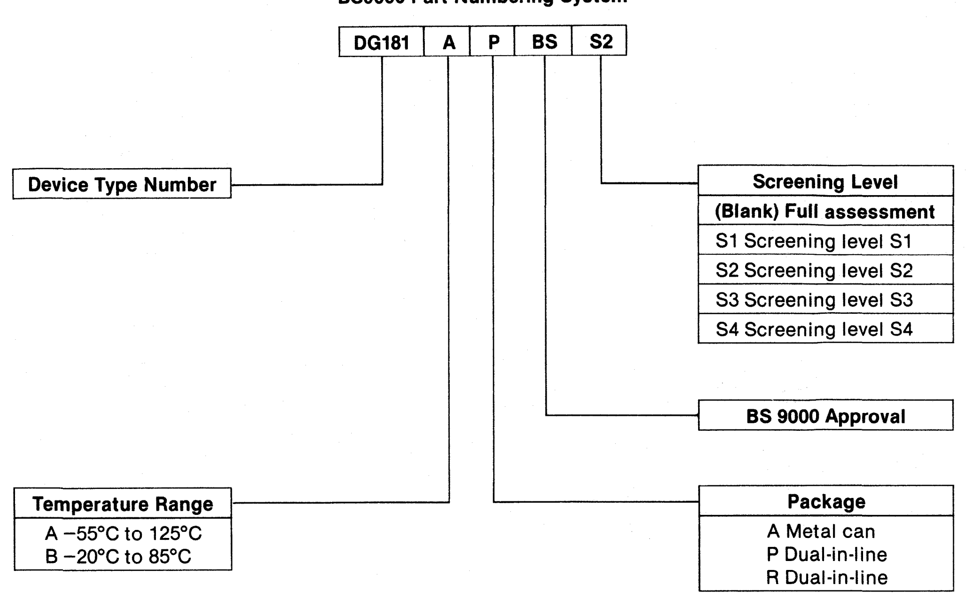
Several Siliconix Analog Switches are available fully certified on the QPL (Qualified Parts List) published monthly by Defense Electronics Supply Center (DESC). The QPL numbers follow this format: JM38510/XXXXX. Refer to the current Siliconix Price List for available part types and order numbers.

JAN Part Numbering System



Part Number	Order Part Number	Generic Part Number
JM38510/11101BCC	SJM181BCC	DG181AP/883
JM38510/11101BIC	SJM181BIC	DG181AA/883
JM38510/11102BCC	SJM182BCC	DG182AP/883
JM38510/11102BIC	SJM182BIC	DG182AA/883
JM38510/11103BEC	SJM183BEC	DG184AP/883
JM38510/11104BEC	SJM185BEC	DG185AP/883
JM38510/11105BCC	SJM187BCC	DG187AP/883
JM38510/11105BIC	SJM187BIC	DG187AA/883
JM38510/11106BCC	SJM188BCC	DG188AP/883
JM38510/11106BIC	SJM188BIC	DG188AA/883
JM38510/11107BEC	SJM190BEC	DG190AP/883
JM38510/11108BEC	SJM191BEC	DG191AP/883
JM38510/11601BCC	SJM300BCC	DG300AP/883
JM38510/11601BIC	SJM300BIC	DG300AA/883
JM38510/11602BCC	SJM301BCC	DG301AP/883
JM38510/11602BIC	SJM301BIC	DG301AA/883
JM38510/11603BCC	SJM302BCC	DG302AP/883
JM38510/11604BCC	SJM303BCC	DG303AP/883
JM38510/11605BCC	SJM304BCC	DG304AP/883
JM38510/11605BIC	SJM304BIC	DG304AA/883
JM38510/11606BCC	SJM305BCC	DG305AP/883
JM38510/11606BIC	SJM305BIC	DG305AA/883
JM38510/11607BCC	SJM306BCC	DG306AP/883
JM38510/11608BCC	SJM307BCC	DG307AP/883
JM38510/12303BCC	SJM200BCC	DG200AP/883
JM38510/12303BIC	SJM200BIC	DG200AA/883
JM38510/12304BEC	SJM201BEC	DG201AP/883

Analog Switches BS9000



Approved Parts		Awaiting Approval*
Generic Part No.	Generic Part No.	Generic Part No.
DG126/ /BS	DG180/ /BS	DG281/ /BS
DG129/ /BS	DG181/ /BS	DG284/ /BS
DG133/ /BS	DG182/ /BS	DG287/ /BS
DG134/ /BS	DG183/ /BS	DG290/ /BS
DG139/ /BS	DG184/ /BS	DG300/ /BS
DG140/ /BS	DG185/ /BS	DG301/ /BS
DG141/ /BS	DG186/ /BS	DG302/ /BS
DG142/ /BS	DG187/ /BS	DG303/ /BS
DG143/ /BS	DG188/ /BS	DG304/ /BS
DG144/ /BS	DG189/ /BS	DG305/ /BS
DG145/ /BS	DG190/ /BS	DG306/ /BS
DG146/ /BS	DG191/ /BS	DG307/ /BS
DG151/ /BS	DG200/ /BS	DG308/ /BS
DG152/ /BS	DG201/ /BS	DG381/ /BS
DG153/ /BS	DG501/ /BS	DG384/ /BS
DG154/ /BS	DG503/ /BS	DG387/ /BS
DG161/ /BS	DG506/ /BS	DG390 /BS
DG162/ /BS	DG507/ /BS	
DG163/ /BS	DG508/ /BS	
DG164/ /BS	DG509/ /BS	
	SI3705/ /BS	

*Contact one of the Silixonix sales offices for latest information.

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Process Option Flow

The Process Option Flow Chart shows the standard screening options provided by Siliconix for Integrated Circuits

Column 1: Denotes the screening process for MIL-883, Class B. To order a part screened to this option, add a "/883" following the package suffix letter. If Group B or C Quality Conformance is also required, call out as a separate line item. Parts in this classification are carried in inventory.

Column 2: Is the screening procedure for military grade standard products ("A" temperature suffix).

Column 3: Is the normal screening procedure for industrial and commercial grade products (B and C temperature suffixes). An industrial and commercial grade product (B and C temperature range) may be given a 160 hour burn-in at 125°C by adding a Dash 4 (—4) following the package suffix letter.

Process Option Flow Chart

/883 MIL-STD-883B METHOD 5004 Class B

- Preseal Inspection, Method 2010, Condition B — /883
- Stabilization Bake, Method 1008, Cond. C, 150°C, 24 Hours — /883
- Temperature Cycle, Method 1010, Cond. C, −65°C to +150°C, 10 Cycles — /883
- Centrifuge, Method 2001, Cond. E, 30,000G Y1 Axis — /883
- Hermeticity (Fine Leak), Method 1014, Cond. A or B, $\leq 5 \times 10^{-8}$ cc/sec — /883
- Hermeticity (Gross Leak), Method 1014, Cond. C — /883
- Electrical Test, Per Data Sheet, at 25°C — Siliconix
- Burn-In, Method 1015, 125°C, 160 Hours — /883
- Electrical Test, Per Data Sheet, 100% at 25°C, −55°C and 125°C — Siliconix
- Quality Conformance, Group A*, Method 5005 — /883
- External Visual, Method 2009**, 100% — /883

STANDARD PRODUCT (A Temperature Suffix)

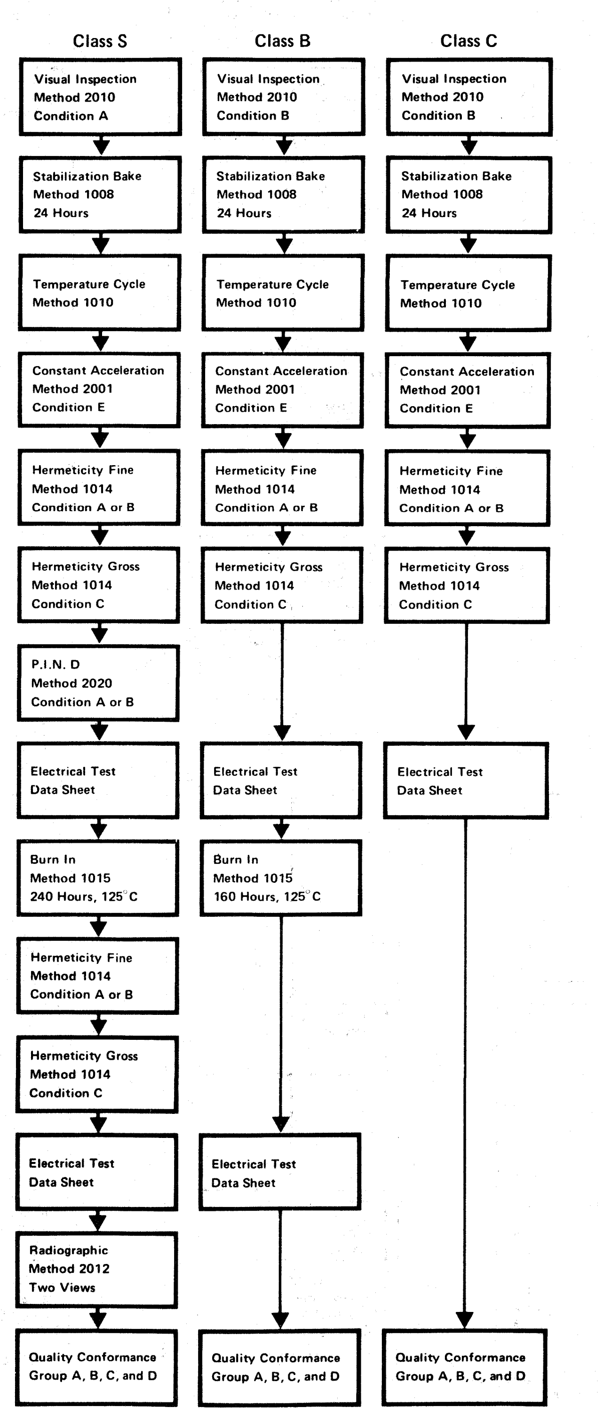
- Preseal Inspection, Method 2010, Condition B — /883
- Stabilization Bake, Method 1008, Cond. C, 150°C, 24 Hours — /883
- Temperature Cycle, Method 1010, Cond. C, −65°C to +150°C, 10 Cycles — /883
- Centrifuge, Method 2001, Cond. E, 30,000G Y1 Axis — /883
- Hermeticity (Fine Leak), Method 1014, Cond. A or B, $<5 \times 10^{-8}$ cc/sec — /883
- Hermeticity (Gross Leak), Method 1014, Cond. C — /883
- Final Electrical Test, 100% Per Data Sheet — Siliconix
- Quality Conformance, Electrical Test, Per Data Sheet, 1.5% AQL — Siliconix
- External Visual, Method 2009**, 2.5% AQL — /883

INDUSTRIAL/COMMERCIAL (B-C Temperature Suffix) and −4 (Burned-in)

- Preseal Inspection, Siliconix Industrial Specifications — Siliconix
- Hermeticity (Gross Leak), (Non-Plastic Only), Method 1014, Cond. C — /883
- Burn-In, 125°C, 160 Hours, (−4 Only) — Siliconix
- Final Electrical Test, 100% Per Data Sheet — Siliconix
- Quality Conformance, Electrical Test, Per Data Sheet, 1.5% AQL — Siliconix
- External Visual, 2.5% AQL — Siliconix

*Group B and C tests done to customer order on /883 parts
**Physical Dimensions Excluded
The latest revision of MIL-STD-883 is applicable

JM38510/883 Process Option Flow Chart



BS9000 Series Process Option Flow Chart

CATEGORY S1 SCREENING LEVEL A	CATEGORY S2 SCREENING LEVEL B	CATEGORY S3 SCREENING LEVEL C	CATEGORY S4 SCREENING LEVEL D	FULL ASSESSMENT LEVEL
Pre-Cap Inspection BS9400 1.2.10 Level A	Pre-Cap Inspection BS9400 1.2.10 Level B	Pre-Cap Inspection BS9400 1.2.10 Level B		
High Temperature Storage BS9400 1.2.6.3 150 C for 24 Hours	High Temperature Storage BS9400 1.2.6.3 150 C for 24 Hours	High Temperature Storage BS9400 1.2.6.3 150 C for 24 Hours		
Rapid Change of Temperature Liquid Immersion BS9400 1.2.6.19				
Rapid Change of Temperature BS9400 1.2.6.13 10 Cycles -65 C to 150 C	Rapid Change of Temperature BS9400 1.2.6.13 10 Cycles -65 C to 150 C	Rapid Change of Temperature BS9400 1.2.6.13 10 Cycles -65 C to 150 C		
Shock at 14 700 m/s^2 BS9400 1.2.6.6				
Acceleration Steady State BS9400 1.2.6.9 296 000 m/s^2 in Directions Y1, Y2	Acceleration Steady State BS9400 1.2.6.9 296 000 m/s^2 in Direction Y1	Acceleration Steady State BS9400 1.2.6.9 296 000 m/s^2 in Direction Y1		
Fine and Gross Leak Tests BS9400 1.2.6.14 (1), (2)	Fine and Gross Leak Tests BS9400 1.2.6.14 (1), (2)	Fine and Gross Leak Tests BS9400 1.2.6.14 (1), (2)		
Electrical Tests at 25 C as Subgroup A3 (a) of the Specification	Electrical Tests at 25 C as Subgroup A3 (a) of the Specification	Electrical Tests at 25 C as Subgroup A3 (a) of the Specification	Electrical Tests at 25 C as Subgroup A3 (a) of the Specification	
Burn-in Screen BS9400 1.2.7.2.1 240 Hour Minimum at 125 C	Burn-in Screen BS9400 1.2.7.2.1 168 Hour Minimum at 125 C		Burn-in Screen BS9400 1.2.7.2.1 168 Hour Minimum at 125 C	
Electrical Tests at 25 C as Subgroup A3 (a) of the Specification				
Burn-in Screen Reverse Bias BS9400 1.2.7.2.1 72 Hours Minimum at 150 C				
Final Electrical Tests at 25 C as Subgroup A3 (a) of the Specification	Final Electrical Tests at 25 C as Subgroup A3 (a) of the Specification	Final Electrical Tests at 25 C as Subgroup A3 (a) of the Specification	Final Electrical Tests at 25 C as Subgroup A3 (a) of the Specification	Final Electrical Tests at 25 C as Subgroup A3 (a) of the Specification
Radiographic Tests				
Groups A, B, C and D Inspection	Groups A, B, C and D Inspection	Groups A, B, C and D Inspection	Groups A, B, C and D Inspection	Groups A, B, C and D Inspection

INSPECTION REQUIREMENTS: All tests to be conducted at $T_{amb} = 25°C$ unless otherwise specified. Samples submitted to tests marked 'D' shall not be accepted for release under BS9000 (see 2.6.5 of BS9000 Part I).

Flow chart for 100% screening test procedures (see also Inspection Requirements). Production batches containing greater than 10% defective units subsequent to Burn-in will not be issued for release.

The following acceptance/rejection criteria apply to the electrical tests after Burn-in for screening levels A, B and D.

(a) Lots exhibiting greater than 20% defectives shall be rejected.
(b) Lots exhibiting less than 10% defectives shall be accepted.
(c) Lots exhibiting between 10% and 20% defectives (inclusive) shall have the defectives removed and the remainder of the lot subjected to an identical Burn-in. If such a Lot then exhibits greater than 5% defectives is shall be rejected.

Radiographic tests. Each device shall be examined, for extraneous matter and assembly defects, in the X and Y directions.

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	AN71-1	A High Resolution CMRR Test Method
F	AN72-1	FETs in Balanced Mixers
A	AN72-2	FETs as Analog Switches
F	AN73-1	FETs as Voltage-Controlled Resistors
A	AN73-2	IC Multiplexer Increases Analog Switching Speeds
A	AN73-3	Switching High-Frequency Signals With FET Integrated Circuits
	AN73-4	Junction FETs in Active Double-Balanced Mixers
A	*AN73-5	Driver Circuits for the JFET Analog Switch
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	AN74-3	Designing Junction FET Input Op Amps
F	*AN74-4	Audio-Frequency Noise Characteristics of Junction FETs
A	*AN75-1	CMOS Analog Switches—A Powerful Design Tool
	AN76-1	Measuring High Frequency S-Parameters on the Dual Gate MOSFET
A	*AN76-6	DG300 Series Analog Switch Applications
AIC	*AN76-7	Function/Application of the L161 Micropower Comparator
AIC	*AN77-1	Function/Application of the LD120/LD121 4½ Digit A/D Converter Set in Measurement Systems
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M	*AN79-1	A 500KHz Switching Inverter for 12V Systems
M	*AN79-3	Dynamic Input Characteristics of a VMOS Power Switch
M	*AN79-4	Driving VMOS FETs
	AN79-5	Using the VN64GA High Current, High Power VMOS Power FET
M	*AN79-6	Using Power MOSFET Transistors to Interface from IC Logic to High Power Loads
	AN79-7	Applications of the VN10KM VMOS Power FET

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M	*AN80-1	A Key to the Advance of Switching Power Supplies
M	*AN80-2	Meet the VMOS FET Model
M	AN80-3	Ultralinear Broadband Amplifier
M	*AN80-4	Enjoy VHF Power Amplifier Design
M	AN80-6	AGC for the VMOS RF Power Amplifier
AIC	AN80-8	Function/Application of the LD122/LD121A ±4½ Digit A/D Converter Set in Measurement Systems
AIC	AN81-1	Microprocessor Interface Techniques As Applied to the Siliconix A/D Converter Family
AIC	AN81-2	Introduction to Quantized Feedback
F	*AN81-3	Composite Op Amp for High Performance
	AN82-1	Solving the Stepper Motor Interface Problems
		Design Aids
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AIC	*DA77-2	Design Aid of the LD120/LD121 4½ Digit DVM
	DA78-4	Build a Smoke Detector With the SM110 IC
M	*DA80-1	A Low Cost Regulator for Microprocessor Applications
	DA81-1	Logic Interfacing Made Easy with the DG308
	DA81-2	Logic Interfacing Made Easy with the DG308
		Design Ideas
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	DI71-4	Wideband Mixer-Preamplifier Using FETs
	DI71-5	A FET Frequency Doubler
	DI71-6	Using FETs in Selective VHF Amplifiers
	DI71-8	Using JFETs in Ultra-Wideband UHF Amplifiers
F	DI71-9	Wideband UHF Amplifier with High Performance FETs
F	*DI73-2	High Performance FETs in Low-Noise VHF Oscillators
	DI80-1	A 5 Watt, Parallel-Mode Crystal Oscillator
		Technical Articles
	TA70-1	High Frequency Junction FET Characterization and Application
F	*TA70-2	FET Biasing
A	*TA73-1	Multiplexer Adds Efficiency to 32-Channel Telephone System
A	TA73-2	Designing with Monolithic FET Switches
	TA76-1	VMOS Power FETs in Your Next Broadband Driver

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M	*TA82-2	MOSPOWER Semiconductor
M	*TA82-3	Bipolar and MOS Transistors: Emerging Partners for the 1980s

Catalogs

Analog Switch & IC Product Data Book
Analog Switches and Their Applications ($7.95 charge)
Small Signal FET Design Catalog
MOSPOWER Design Catalog
OEM Pricing with Cross Reference
RF MOSPOWER Short Form Catalog
Siliconix Short Form Selector Guide

Key

Catalogs

AIC = Analog Switch & IC Product Data Book
A = Analog Switches and Their Applications
F = Small Signal FET Design Catalog
M = MOSPOWER Design Catalog
*Available in bound catalog only.

Reprints & Reports

- Siliconix, Inc. Annual Report.
- Designing a VMOS 250 Watt Off-Line Inverter. David C. Hoffman, *Powercon* 3/78
- Designing with CODECs: Know Your A's and μ's. Thomas J. Mroz, *EDN* 5/76
- Log Data under μ Control, Gary Grandbois, *Electronic Design* 5/76
- Higher Power Ratings Extend VMOS FETs' Dominion, Arthur D. Evans, David C. Hoffman, Edwin S. Oxner, Walter Heinzer and Lee Shaeffer. *Electronics* 6/78
- CODEC has On-Chip Signaling for Phone Applications, Walter Heinzer and Steve Bolger, *Electronics* 6/7/79
- A Microprocessor Controlled VMOS Power Supply, David C. Hoffman
- Control Analog Signals with Voltage, Stephen Moore, *Electronic Design,* 1978
- Exploit VMOS FETs' Advantages to Drive Bipolar Power Transistors, F. Michael Barlage, *Powercon* 5/78
- Rely on IC Analog Switches for Fast Small-Signal Control, *EDN*, August 5, 20, Sept. 5, 1980
- Composite Op Amp Outperforms FET-Input ICs, *EDN*, May 27, 1981

Books

Designing with Field-Effect Transistors, Edited by Arthur D. Evans. Available at your technical bookstore or write to Suite 26-1; McGraw-Hill Book Co., 1221 Avenue of the Americas, New York, NY 10020.

Power FETs and Their Applications, by Edwin S. Oxner. Available at your technical bookstore or write to: Mail Order Billing, Prentice-Hall, Inc., Tappan Road, Old Tappan, NJ 07675.

MOSPOWER

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Twx: 810-866-0328

FLORIDA, Orlando (32807)
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(305)275-1132
Twx: 810-850-0103

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Twx: 810-459-1624

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21730 Nordhoff St.
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Twx: 910-595-2638

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Twx: 910-340-6364

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CALIFORNIA, Sunnyvale (94086)
Hamilton/Avnet, #03
1175 Bordeaux Avenue
(408) 743-3300
Twx: 910-339-9332

CALIFORNIA, Tustin (92680)
Anthem Electronics, Inc.
2661 Dow Avenue
(714)730-8000
Twx: 910-595-1585

CALIFORNIA, Woodland Hills (91367)
Hamilton/Avnet, #71
21050 Erwin Street
(213) 883-0000

COLORADO, Englewood (80111)
Hamilton/Avnet, #06
8765 E. Orchard Rd., Suite 708
(303)740-1000
Twx: 910-931-0510

COLORADO, Thornton (80241)
Wyle Distribution Group
451 E. 124th Ave.
(303)457-9953
Twx: 910-936-0770

COLORADO, Wheatridge (80033)
Bell Industries
8155 W. 48th Ave.
(303)424-1985
Twx: 910-938-0393

CONNECTICUT, Danbury (06810)
Hamilton/Avnet, #21
Commerce Drive, Commerce Park
(203)797-2800
Twx: 710-460-0594

CONNECTICUT, Wallingford (06492)
Marshall Industries
Village Lane
Barnes Industrial Park
(203)265-3822
Twx: 710-465-0747

FLORIDA, Ft. Lauderdale (33309)
Hamilton/Avnet, #17
6801 N.W. 15th Way
(305) 971-2900
Twx: 510-956-3097

FLORIDA, Orlando (32809)
Pioneer Elec.
6220 S. Orange Blossom Trail, Ste. 412
(305)859-3600
Twx: 810-850-0177

FLORIDA, St. Petersburg (33702)
Hamilton/Avnet, #25
3197 Tech Drive No.
(813)576-3930
Twx: 810-863-0374

FLORIDA, Winter Park (32789)
Milgray Electronics
185 Lee Avenue
(305) 647-5747

GEORGIA, Norcross (30092)
Hamilton/Avnet #15
5825 Peachtree Corners E-D
(404) 447-7500
Twx: 810-766-0432

GEORGIA, Norcross (30093)
Marshall Industries
4364B Shakelford Rd.
(404)923-5750
Twx: 810-766-3969

ILLINOIS, Bensenville (60106)
Hamilton/Avnet, #10
1130 Thorndale Ave.
(312) 860-7780
Twx: 910-227-0060

ILLINOIS, Elk Grove Village (60007)
Pioneer/Chicago
1551 Carmen Drive
(312)437-9680
Twx: 910-222-1834

ILLINOIS, Elk Grove Village (60007)
GBL/Goold Electronics
610 Bonnie Lane
(312) 593-3222

INDIANA, Carmel (46032)
Hamilton/Avnet, #28
485 Gradle Drive
(317)844-9333
Twx: 810-260-3966

INDIANA, Indianapolis (46250)
Pioneer/Indiana
6408 Castleplace Drive
(317)849-7300
Twx: 810-260-1794

KANSAS, Overland Park (66215)
Hamilton/Avnet
9219 Quivira Rd.
(913)888-8900
Twx: 910-743-0005

MARYLAND, Columbia (21045)
Hamilton/Avnet, #12
6822 Oak Hall Lane
(301)995-3500(MD)
(301)621-5410(DC)
Twx: 710-862-1861

MARYLAND, Gaithersburg (20760)
Pioneer/Washington
9100 Gaither Rd.
(301)948-0710
Twx: 710-828-0545

MARYLAND, Gaithersburg (20760)
Marshall Industries
16760 Oakmont Ave.
(301)840-9450
Twx: 710-828-0223

MASSACHUSETTS, Burlington (01803)
Milgray Electronics
79 Terrace Hall Ave.
(617)272-6800
Twx: 510-225-3673

MASSACHUSETTS, Burlington (01803)
Marshall Industries
1 Wilshire Road
(617)272-8200
Twx: 710-332-6359

MASSACHUSETTS, Woburn (01801)
Hamilton/Avnet, #18
50 Tower Office Park
(617)953-9700
Twx: 710-393-0382

MICHIGAN, Grand Rapids (49508)
Hamilton/Avnet #67
2215 20th St., S.E. A5

MICHIGAN, Livonia (48150)
Hamilton/Avnet, #66
32487 Schoolcraft
(313)522-4700
Twx: 810-242-8775

MICHIGAN, Livonia (48150)
Pioneer/Michigan
13485 Stamford
(313)525-1800
Twx: 810-242-3271

MINNESOTA, Minneapolis (55435)
Industrial Components
5229 Edina Industrial Blvd.
(612)831-2666
Twx: 910-576-3153

MINNESOTA, Minnetonka (55343)
Hamilton/Avnet
10300 Bren Rd. East
(612)932-0600
Twx: 910-576-2729

MINNESOTA, Minnetonka (55343)
Pioneer/Twin Cities
10203 Bren Rd. East
(612)935-5444

MISSOURI, Earth City (63045)
Hamilton/Avnet #05
13743 Shoreline Ct.
(314) 344-1200
Twx: 910-762-0606

NEW JERSEY, Cherry Hill (08003)
Hamilton/Avnet, #14
One Keystone Ave.
(609)424-0100
Twx: 710-940-0262

NEW JERSEY, Clifton (07015)
Marshall Industries
1111 Paulison Ave.
(201)340-1900
Twx: 710-989-7052

NEW JERSEY, Fairfield (07006)
Hamilton/Avnet, #19
10 Industrial Rd.
(201)575-3390
Twx: 710-734-4388

NEW JERSEY, Mt. Laurel (08057)
Marshall Industries
102 Gaither Dr., Unit 2
(609)234-9100 NJ (215)627-1920 PA
Twx: 710-941-1361

NEW MEXICO, Albuquerque (87123)
Alliance Electronics
11030 Cochiti S.E.
(505) 292-3360
Twx: 910-989-1151

NEW MEXICO, Albuquerque (87123)
Bell Industries
11728 Linn NE
(505)292-2700
Twx: 910-989-0625

NEW MEXICO, Albuquerque (87119)
Hamilton/Avnet, #22
2524 Baylor Dr., SE
(505)765-1500
Twx: 910-989-0614

NEW YORK, Buffalo (14202)
Summit Distributors, Inc.
916 Main Street
(716) 884-3450
Twx: 710-522-1692

NEW YORK, East Syracuse (13057)
Hamilton/Avnet, #8
1600 Corporate Circle
(315)437-2642
Twx: 710-541-1560

NEW YORK, Endwell (13760)
Marshall Industries
10 Hooper Road
(607)754-1570
Twx: 510-252-0194

NEW YORK, Freeport (11520)
Milgray Electronics, Inc.
191 Hanse Ave.
(516)546-5600
Twx: 516-546-5600

NEW YORK, Hauppauge (11787)
Harvey Military/Components Plus
40 Oser Ave.
(516)231-9200
Twx: 510-227-9869

NEW YORK, Hauppauge (11787)
Marshall Industries
275 Oser Avenue
(516) 273-2424
Twx: 510-224-6109

NEW YORK, Melville (11747)
Hamilton/Avnet, #20
5 Hub Drive
(516)454-6000
Twx: 510-224-6166

NEW YORK, Portchester (10573)
Zeus Components, Inc.
100 Midlin Ave.
(914) 937-7400
Twx: 710-567-1248

NEW YORK, Rochester (14623)
Hamilton/Avnet, #61
333 Metro Park
(716)475-9130
Twx: 510-253-5470

NEW YORK, Rochester (14623)
Marshall Industries
1260 Scottsville Rd.
(716)235-7620
Twx: 510-253-5470

NORTH CAROLINA, Greensboro (27406)
Pioneer/NC
103 Industrial Ave.
(919)273-4441
Twx: 510-925-1114

Worldwide Sales Offices (Cont'd)

U.S. Distributors (Cont'd)

NORTH CAROLINA, Raleigh (27609)
Hamilton/Avnet
2803 Industrial Dr.
(919)829-8030
Twx: 510-928-1836

OHIO, Cleveland (44105)
Pioneer/Cleveland
4800 E. 131st Street
(216)587-3600
Twx: 810-422-2210

OHIO, Dayton (45459)
Hamilton/Avnet, #64
954 Senate Dr.
(513)433-0610
Twx: 810-450-2531

OHIO, Dayton (45424)
Pioneer/Dayton
4433 Interpoint Blvd.
(513)236-9900
Twx: 810-459-1622

OHIO, Warrensville Heights (44128)
Hamilton/Avnet, #62
4588 Emery Industrial Parkway
(216)831-3500
Twx: 810-427-9452

OKLAHOMA, Tulsa (74129)
Quality Components
9934 E. 21st St. South
(918)664-8812

OREGON, Lake Oswego (97034)
Hamilton/Avnet, #27
6024 SW Jean Road, Bldg. C, Ste. 10
(503)635-8836
Twx: 910-455-8179

PENNSYLVANIA, Horsham (19044)
Pioneer Elec.
261 Gibraltar Rd.
(215)674-4000
Twx: 510-665-6778

PENNSYLVANIA, Pittsburgh (15238)
Pioneer/Pittsburgh
259 Kappa Dr.
(412)782-2300
Twx: 710-795-3122

TEXAS, Addison (75001)
Quality Components
4257 Kellway Circle
(214)387-4949
Twx: 910-860-5459

TEXAS, Austin (78758)
Hamilton/Avnet, #26
2401 Rutland Dr.
(512)837-8911
Twx: 910-874-1319

TEXAS, Austin (78758)
Harrison Equipment Co., Inc.
8910-A1 Research Blvd.
(512) 458-3555

TEXAS, Austin (78758)
Quality Components
2427 Rutland Drive
(512)835-0220
Twx: 910-874-1377

TEXAS, Dallas (75234)
Harrison Equipment Co., Inc.
14282 Gillis Rd.
(214) 239-2750

TEXAS, Dallas (75240)
Zeus Components
14001 Goldmark
(214) 783-7010

TEXAS, Houston (77063)
Hamilton/Avnet, #11
8750 Westpark
(713)780-1771
Twx: 910-881-5523

TEXAS, Houston (77036)
Quality Components
6126 Westline
(713)772-7100

TEXAS, Irving (75062)
Hamilton/Avnet, #16
2111 W. Walnut Hill Lane
(214)659-4151
Twx: 910-860-5929

TEXAS, Stafford (77477)
Harrison Equipment Co., Inc.
11100 W. Airport Blvd.
(713) 879-2771

UTAH, Salt Lake City (84119)
Hamilton/Avnet, #09
1585 West 2100 South
(801)972-2800
Twx: 910-925-4018

WASHINGTON, Bellevue (98000)
Hamilton/Avnet, #07
14212 NE 21st St.
(206)453-5844
Twx: 910-443-2464

WASHINGTON, Bellevue (98005)
Wyle Distribution Group
1750 - 132nd Ave. NE
(206)453-8300
Twx: 910-443-2526

WISCONSIN, Milwaukee (53214)
Marsh Electronics, Inc.
1563 So. 101st St.
(414)475-6000
Twx: 910-262-3321

WISCONSIN, New Berlin (53151)
Hamilton/Avnet, #57
2975 Moorland Rd.
(414)784-4510
Twx: 910-262-1182

European Distributors/Representatives

AUSTRIA
Ing. Ernst Steiner
Hummelgasse 14
A-1130 Vienna
Tel: 0222/827474
Tlx: 135026

BELGIUM
J.P. Lemaire
Rampe Gauloise 1-A
1020 Brussels
Tel: (02) 478 4847
Tlx: 24610

CYPRESS
For the distributor's address, contact our Siliconix sales office in France

DENMARK
Ditz Schweitzer A.S.
Vallensbaekvej 41
Dk-2600 Glostrup
Tel: (02) 45-30-44
Tlx: 33257

FINLAND
Oy Findip AB
Teollisuustie 7, P.O.B. 34
SF 02700 Kauniainen
Tel: 358-0-5052255
Tlx: 12-3129

FRANCE
Almex
48 Rue de L'Aubepine
92160 Antony Cedex
Tel: 666-21-12
Tlx: 250067

Alrodis
40 Rue Villon
69008 Lyon
Tel: (78)00.87.12
Tlx: 380636

Composants S.A.
Avenue Gustave Eiffel
B.P. 81
33605 Pessac Cedex
Tel: (56)36.4040
Tlx: 550696F

Composants S.A.
55 Avenue Louis Brequet
31400 Toulouse
Tel: (61) 20.82.38

Composants S.A.
183 Route de Paris
86000 Poitiers
Tel: (49)88.60.50
Twx: 791525F

A. Baltzinger
18-26 Route du Gen de Gaulle
B.P. 63
67042 Strasbourg Cedex
Tel: (88) 331852
Tlx: 870952F

Composants S.A.
57 Rue Manoir de Servigne
Z1, Route de Lorient
B.P. 3209
35013 Rennes Cedex
Tel: (99) 54.01.53
Tlx: 740311

Sanelec Electronique
7 Rue de la Couture
Z1, de la Pilaterie
59700 Marcq-en-Baroeuil
Tel: (20)98-92-13
Tlx: 160 143F

SCAIB
80 Rue d'Arcueil
94523 Rungis Cedex
Tel: 687-23-13
Tlx: 204 674F

GERMANY
Ditronic GmbH
IM Asemwald 48
7000 Stuttgart 70
Tel: (0711)724844, 722079
Tlx: 07-255638

Ing. Büro K.H. Dreyer
Flensburger Strasse 3
2380 Schleswig
Tel: (04621)24055
Tlx: 02-21334

Ing. Büro K.H. Dreyer
Albert Schweitzer - Ring 36
2000 Hamburg 70
Tel: (040)669027
Tlx: 2164484

EBV Elektronik GmbH
Oberweg 6
D-8025 Unterhaching
Tel: 089-61105-1
Tlx: 05-24535

EBV Elektronik GmbH
Alexanderstrasse 42
7000 Stuttgart 1
Tel: (0711)247481
Tlx: 07-22271

EBV Elektronik GmbH
Ostrasse 129
4000 Dusseldorf
Tel: (0211)84846/7
Tlx: 08-587267

EBV Elektronik GmbH
Kiebitzrain 18
3006 Burgwedel 1/Hannover
Tel: (05139)5038
Tlx: 09-23694

EBV Elektronik GmbH
Schenckstr 99
6000 Frankfurt M.90
Tel: 0611/785037
Tlx: 04-13590

Ing. Büro Rainer König
Königsbergerstrasse 16A
1000 Berlin 45
Tel: 030 772 8009
Tlx: 184 707

Ultratronik GmbH
Münchner Strasse 6
8031 Oberalting-Seefeld
Tel: (08152)7773
Tlx: 05-26459

GREECE
General Electronics, Ltd.
209 Thevon St.
Nikaia, Piraeus
Tel: (1) 491 35 95 or
(1) 491 10 56
Tlx: 212949 GELT GR

General Electronics Ltd.
6 Skoufa St.
Athens 136
Tel: (1) 490 69 98
Tlx: 219250 RETE GR

HOLLAND
Koning en Hartman Elektrotechniek BV
Postbus 43220, 30 Koperwerf
2504 A E The Hague
Koperwerf 30
Tel: 070-210101
Tlx: 31528

ITALY
Dott Ing Giuseppe DeMico S.P.A.
Via Vittorio
Veneto 8, 20060 Cassina
De Pecchi, Milano
Tel: (02) 9520551
Tlx: 330869

NORWAY
A. S. Kjell Bakke
Øvre Raelingsvei 20
P.O. Box 27
N-2001 Lillesstrøm
Tel: (02) 83 02 20
Tlx: 19407

PORTUGAL
Telectra S.A.R.L.
Rua Rodrigo da Fonseca 103
1000 Lisbon
Tel: 68.60.72
Tlx: 42827

Worldwide Sales Offices (Cont'd)

European Distributors/Representatives (Cont'd)

SOUTH AFRICA
Electrolink (PTY) Ltd.
P.O. Box 1020
Cape Town 8000
Tel: 215 350
Tlx: 572 732

SPAIN
Comercial Española Componentes S. A.
Calle Arzobispo
Morcillo 24 Oficina 5
Madrid 34
Tel: 733 7054/55
Tlx: 47010

Redis Logar SA
Casanova 56
Barcelona 11
Tel: 2549048

Rediś Logar SA
Lopez de Hoyos,
78 DPDO, Madrid 2
Tel: 4113561
Tlx: 23967

SWEDEN
Komponentbolaget NAXAB
Box 4115
S-171 04 Solna
Tel: 08.985140
Tlx: 17912 KOMP

SWITZERLAND
Abelec A.G.
CH-8116 Würenlos
Landstrasse 78
Tel: 01-730-0455
Tlx: 59834

UNITED KINGDOM
Abercorn Electronics Ltd.
Abercorn House, 3 Pittville St.
Edinburgh, Scotland
Tel: 031 669 6479

Bartec Ltd.
Foundry Road, Horsham
West Sussex RH13 5PX
Tel: 0403-51881
Tlx: 877222

Dage Eurosem Ltd.
Rabans Lane
Aylesbury
Bucks HP19 3RG
Tel: 0296-32881
Tlx: 83518

Hartech Ltd.
Forum House, Stirling Road
Chichester PO19 2EN
West Sussex
Tel: 0243-773511
Tlx: 86230

Macro-Marketing Ltd.
Burnham Lane,
Slough, Berks
Tel: (06286)4422
Tlx: 847945

Semiconductor Specialists (UK) Ltd.
Carroll House
159 High Street
West Drayton
Middlesex UB7 7XB
Tel: (08954)45522/46415
Tlx: 21958

YOGOSLAVIA
Contact: Belram S. A.
83 Avenue des Mimosas
1150 Brussels, Belgium
Tel: 734.33.32 734.26.19
Tlx: 21790

Canadian Distributors/Representatives

DISTRIBUTORS

BRITISH COLUMBIA
Burnaby (V5G 4J7)
RAE Industrial Elec. Ltd.
3455 Gardner Court
(604) 291-8866
Tlx: 04-356533
Twx: 610-929-3065

ONTARIO, Mississauga (L4V 1M5)
Hamilton/Avnet, #59
6845 Rexwood Dr.
(416) 677-7432
Twx: 610-492-8867

ONTARIO, Ottawa (K2C 3P2)
Future Elec.
Baxter Centre
1050 Baxter Rd.
(613) 820-8313

ONTARIO, Nepean (K2E 7L5)
Hamilton/Avnet, #60
2110 Colonade Road
(613) 226-1700
Tlx: 0534971

ONTARIO, Downsview (M3H 5S9)
Future Electronics
4800 Dufferin St.
(416) 663-5563

QUEBEC, Pointe Claire (H9R 5C7)
Future Elec.
237 Hymus Blvd.
(514) 694-7710
Twx: 610-421-3251

QUEBEC, St. Laurent (H4S 1M2)
Hamilton/Avnet, #65
2670 Sabourin St.
(514) 331-6443
Twx: 610-421-3731

REPRESENTATIVES

ISLINGTON, ONTARIO M9B 6E3
Pipe Thompson, Ltd.
5468 Dundas St., West Suite 206
(416) 236-2355
Twx: 610-492-4367

NORTH GOWER, ONTARIO K0A 2T0
Pipe Thompson, Ltd.
Rural Route #2
(613) 258-4067
Twx: 610-492-4367

Worldwide Sales Offices (Cont'd)

Other International Distributors/Representatives

AUSTRALIA
STC Cannon Components PTY. LTD.
248 Wickham Road - P.O. Box 62
Moorabbin, Victoria 3189
Tel: Melbourne 555-1566
Tlx: Melbourne AA 30877
Cable: CANNONLEC - MELBOURNE

BRAZIL
Cosele Comercio e Servicos
Electronicos Ltda.
Rua Da Consolacao, 867
01310 Sao Paulo
Tel: 255-1733
Tlx: 1130869-CSEL-BR

INDIA
Zenith Electronics
541 Panchratna
Mama Parmanand Marg
Bombay 400004
Tel: 384214
Tlx: 011-3152

Authorized U.S. Agent:
Fegu Electronics Inc.
3308 Middlefield Rd.
Palo Alto, CA 94306
Tel: (415)493-1788
Tlx: 345599

ISRAEL
Telsys Ltd.
12, Kehilat Venetsia St.
Tel Aviv
Tel: 482126-7-8
Tlx: 032392

JAPAN
Teijin Advanced Products Corp.
1-1 Uchisaiwai-cho, 2-Chome
Chiyoda-Ku, Tokyo, 100
Tel: (03)506-4670
Tlx: J-23548

KOREA
Exim Co. Ltd.
155-12 Yumri-Dong,
Mapo-Ku
Seoul
Tel: 715-4933
Tlx: BROXIM K25253

LATIN AMERICA
Intectra Inc.
2629 Terminal Blvd.
Mt. View, CA 94043
Tel: (415)967-8818
Tlx: 345545 Intectra MNTV
Cable: INTECTRA

MALAYSIA
Carter Semiconductor
(M.) SDN. Berhad*
Jalan Lapangan Terbang
Ipon, Perak
Tel: 513400
Tlx: MA44050
Cable: CARXISTOR IPOH

NEW ZEALAND
S.T.C. Auckland
10 Margot St.
Epsom, Auckland 3
Tel: 500-019
Tlx: NZ21888

PHILIPPINES
Alexan Commercial
812 Elcano St.
P.O. Box 4459, Manila
Tel: 405923
Tlx: 27484

Dynetics, Inc.
FTI Complex,
Taguig, Metro Manila

Stanford Microsystems, Inc.
FCI Building
416 Dasmarinas 4 St.
Manila

SINGAPORE & MALAYSIA
Carter Semiconductor PTE. Ltd.
807, 8th Floor Front Block
Orchard Road, Orchard Towers
Tel: 235 6653
Tlx: RS 36443

Reliability Singapore PTE Ltd.
26, Kallang Place
Blk 7, Unit 3F
Singapore 12

SOUTH AFRICA
ElectroLink (Pty) Ltd.
P.O. Box 1020
Cape Town 8000
Tel: 215-350
Tlx: 572-7320

TAIWAN
Don Business Corp. 3 FL
354 Chang Chung Rd.
Taipei
Tel: 571-2911
Tlx: 25641 DONBC
Cable: "DONBC" TAIPEI

THAILAND
Choakchai Electronic Supplies
128/22 Thanon Atsadang
Bangkok 2
Tel: 221-0432-221-5384
Cable: SAHAPIPHAT

VENEZUELA
P. Benavides S.R.L.
Avilanas a Rio Edificio
Rio Caribe, Local 9
Caracas
Tel: 52 92 97
Tlx: 21801 PBTH

Worldwide Sales Office Updates